

STEPS FORWARD IN THE DIGITAL RF CONTROL SYSTEM AT LNS

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Abstract

The present radio frequency control system is changing under the influence of the new digital devices from the commercial broadcast industries. Since the introduction of the direct digital synthesized (DDS) as a new RF generator for the superconducting cyclotron in 2002, several measures aimed at improving the quality of the RF control system have been adopted in the digital field. Experimental results on RF digital prototypes of generators, turn-on, protections, phase and amplitude loops have been achieved. At the moment, a hybrid digital and analog RF control system is running at LNS. The status of these digital additions in the general frame of the present RF control system, will be given in this report.

RF CONTROL SYSTEM OVERVIEW

Currently, the radio frequency control system of the superconducting cyclotron has its roots in the analog rather than in the digital system introduced at the beginning of our cyclotron activity [1]. The system has been modified and all the technical improvements have been successfully tested during the beam cyclotron time in the last few years. The main functional blocks of the control system are: generators, turn-on, phase-amplitude-tuning loops, electromechanical driving devices. We are working in two parallel ways: a semi-conservative one, which partially grafts the new seeds of the digital technique in the mainframe of the present RF control system; the other more progressive, as well as experimental way, is targeted towards a full Digital-based RF control system. The most important digital upgrade concerns the RF generator.

RF generator

The present RF generator is an evolution of the first RF source based on the direct digital synthesis technique introduced in 2002 [2]. The same DDS technique has been adopted to generate four sinusoidal waves: the first three for the RF cavities, plus an auxiliary channel is available. The initial amplitude and phase are set by a personal computer, without any phase shifters or linear attenuators. The core of the system is based on the commercial microchip, the AD9854, providing a 48 bit frequency resolution together with a frequency system clock of 300 MHz giving a resolution of 1 μ Hz, 0.02° in phase, 27 mV in amplitude with a maximum frequency output of up to 120 MHz. The four electronic boards, DDS1÷4 host this integrated circuit. The reference 300 MHz system clock is generated from a 50 MHz precision high stable \pm 5ppb quartz oscillator. The reference clock through a well-balanced distribution network reaches each board so allowing for perfect synchronization. An

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external clock can be used to lock the generator to another oscillator. The stability output signals can always be checked by -20dB coupling ports. The personal computer is connected to the four DDS, through a customized electronic board interface via the parallel port. The block diagram of Figure 1 shows the main components of this new multi RF source generator.

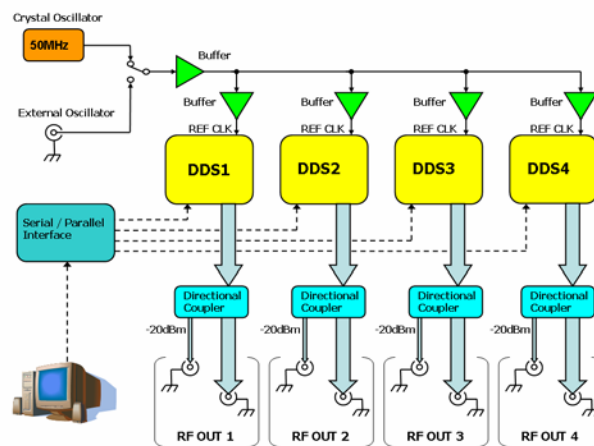


Figure 1: Block diagram of the DDS generator.

All the components in the above block diagram are placed inside a 3-unit standard cabinet. Great attention has been adopted in the shielding and grounding assembling technique to increase the RF output quality.



Figure 2: the DDS generator

Figure 2 shows the four DDS boards, the PC interface, the \pm 5ppb quartz oscillator inside the cabinet. The in-house software written in Visual Basic© programming language allows users to fully operate the DDS via a menu-driven control panel in a Windows© environment as displayed on the PC monitor. Moreover, this software

calculates the exact value of the frequency word according to the maximum resolution of the DDS itself. This virtual tool calculator avoids any shift in phase between the output RF channels. The control panel displays the frequency word in decimal, hexadecimal, or binary at the same time. The least significant bit of the string shows if the RF outputs are in phase or out of phase. Figure 3 shows the control panel in detail.

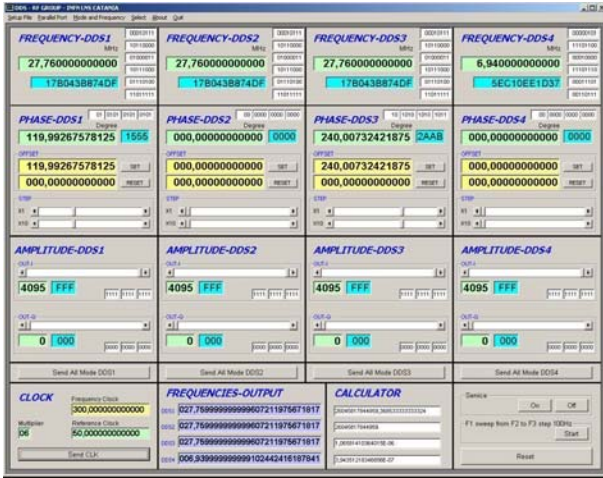


Figure 3: DDS control panel

The control panel displays four DDS output channels. The frequency, phase, amplitude can be changed independently for each channel. The clock, together with the multiplication factor, can be adjusted too. The on-line tool calculator to see the deviation phase is shown in the central bottom side. The display in Figure 2 shows a real frequency cyclotron of 27.76 MHz for the DDS1-2-3 and a sub-harmonic $\frac{1}{4}$ for the DDS4. The four DDS sinusoidal waveforms are shown in be Figure 4.

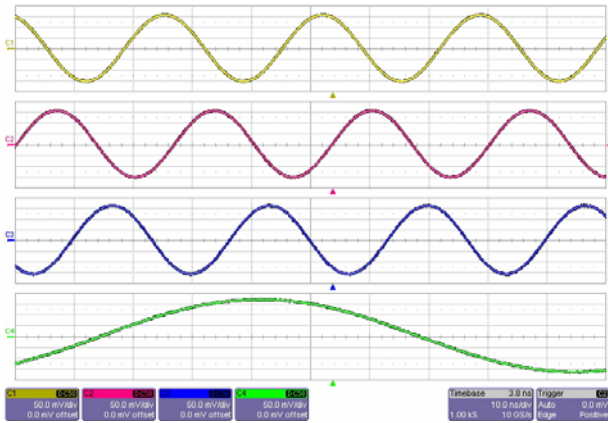


Figure 4: the 3 cavities and chopper sine waves.

The outputs 1-2-3 supply the three cavities of the cyclotron while the output 4 drives a chopper system along the acceleration beam line. The cyclotron harmonic 2 imposes a phase difference between the three DDS outputs for the RF cavities equal to 120° , the final phase stability is well below $\pm 0.1^\circ$. The acceleration of the beam of $^{129}\text{Xe}^{+31}$ at 30 MeV/amu was performed

successfully on April 2007. This is the best acceptance test of any modifications or upgrades of the RF controls.

Uncertainties and limits of the DDS system

The DDS technique uses digital data processing blocks as a means to generate an output signal, tunable in frequency, amplitude and phase, referenced to a precision clock source. In essence, the reference clock frequency is “divided down” in a DDS architecture by the scaling factor set forth in a programmable binary tuning word. In our case the tuning word is 48 bits long, which provides a remarkably high resolution of the output frequency. Equation (1) defines the system clock frequency, whilst equation (2) shows the minimum frequency step.

$$f_{\text{systemclock}} = K_{\text{factor}} \cdot f_{\text{clock}} \quad (1)$$

$$f_{\text{step}} = \frac{f_{\text{systemclock}}}{2^{48}} \quad (2)$$

In our case the frequency system is equal to 300 MHz, while the frequency step is about 1.065814104 μHz .

Formula (3) gives the normalized frequency of the system according to the following division factor:

$$N_{\text{word}} = \frac{f_0}{f_{\text{step}}} \quad (3)$$

this normalized factor is the tuning word of the DDS system, where f_0 is the frequency written on the control panel. The DDS electronic architecture takes into account only the integer part of the fraction, between 1 and 2^{48} . In this case there will be a difference between the set f_0 and the output frequency generated by the DDS.

$$f_{\text{output}} = \text{Int}[N_{\text{word}}] \cdot f_{\text{step}} \quad (4)$$

If we substitute f_{step} from the equation (2) in (4), we get :

$$f_{\text{output}} = \text{Int}[N_{\text{word}}] \cdot \frac{K_{\text{factor}} \cdot f_{\text{clock}}}{2^{48}} \quad (5)$$

the integer N_{word} determines a bit truncation inside a DDS, meaning the generated frequency is lower than the real one:

$$\begin{aligned} f_{\text{output}} &\leq f_0 & \Delta f &= f_0 - f_{\text{output}} \\ 0 &\leq \Delta f < f_{\text{step}} & 0 &\leq \Delta f < \frac{f_{\text{systemclock}}}{2^{48}} \\ 0 &\leq \Delta f < \frac{K_{\text{factor}} \cdot f_{\text{clock}}}{2^{\text{bit}}} & & \end{aligned} \quad (6)$$

$$f_{\text{output}} = 27,759999999999607211975671817 \text{ MHz}$$

$$\Delta f = f_0 - f_{\text{output}} = 0,394351218346856 \mu\text{Hz}$$

If $f_0=27.76$ MHz, then formula (6) gives the uncertainty between the set frequency and the generated DDS one.

The same clock for the DDS boards means equal Δf for each output signals. The amplitude and phase resolutions are related to the bit conversion only. 14 bit for the phase and 12 bit for the amplitude give $\Delta\Phi=2\pi/2^{14}$ and $\Delta V=V_{\max}/2^{12}$, $\Delta\Phi=0.02197265625^\circ$ and $\Delta V\approx 27\text{mV}$.

The sliding shorts driving movement system

Another digital step in the mainframe of the RF control system is the new driving electromechanical system for the sliding shorts of the cavities. A new control console panel has been developed. It adopts the same software environment of the DDS generator. The console sets and reads the position of the sliding shorts for all the $\frac{1}{2}\lambda$ length of the RF cavities in the frequency range of 15÷48 MHz. A new mechanic design together with six miniaturized DC motors has been installed to improve the movement of the short circuits of the cyclotron. A minimum resolution step up to 0.1mm has been achieved. Figure 5 shows the new mechanic plus a DC motor.



Figure 5: the new mechanic and the DC motor.

Full DDS-based RF control system

A more progressive and radical approach was conceived in the total DDS-based control system. The system includes RF generators, phase and amplitude loops, turn-on, protections for the cyclotron cavities [3].

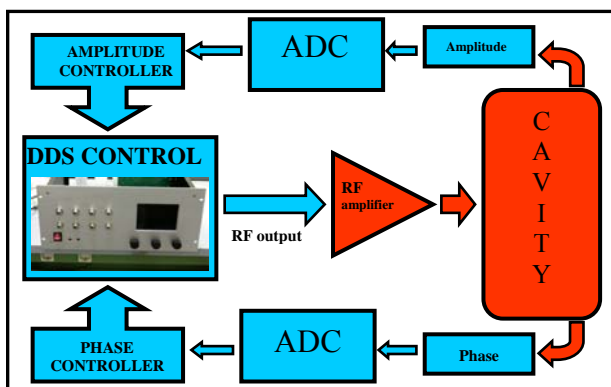


Figure 6: the complete DDS control RF system

The DDS output drives the power amplifier directly, while the input is connected to a cavity pick-up, as shown in Figure 6. The feedback cavity signal is digitalized, compared with a reference and processed by a μ computer. The test was performed with an RF power of about 20 kW at the frequency of 22.09 MHz. Further positive tests on

the turn-on system and protections were done, too. All the multipactoring levels were avoided and the automatic restart procedure was also perfectly tested. Although the first DDS closed loop test was positive, it is nowhere near the performance, under -85dBc , of a classic analog loop. The residual modulation of the Dee voltage of -66dBc and -62dBc , respectively at 50Hz and 100Hz has been measured at closed loop on the DDS control system.

FPGA PI controller error amplifier

A parallel approach of the Proportional-Integral controllers is necessary for low level RF systems [4]. It can cancel steady-state error both in amplitude and phase loops. The advantage of digital PI control implementation over a traditional one is increasing system flexibility. For digital implementation, an alternative is to use Field Programmable Gate Array as a technical platform. A prototype and the relative software codes have been developed. The test showed the same performance as the analog loop one, with the addition of more flexibility.

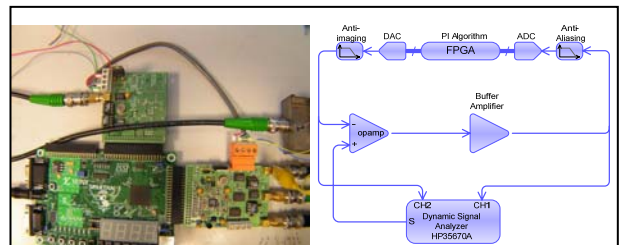


Figure 7: hardware test board and block diagram set-up.

The hardware test bench includes an ADC board, a DAC board and an off- shelf Spartan-3 FPGA evaluation board. The summing point was placed on the ADC board both for convenience and noise reduction. A simplified 10-baseT interface was integrated in the DAC board as an aid method for first stage test activities. The test boards and the block diagram are shown in Figure 7.

Conclusion

In our opinion the way forward is to develop a hybrid analog and digital system exploiting the DDS technology together with FPGA platforms, given the proven benefit of its high-level efficiency, flexibility and integration in the creation of a low-level radio frequency system.

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