SIGNAL PROCESSING FOR HIGH PRECISION PHASE MEASUREMENTS*

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Abstract

High precision phase measurement is important for many areas of accelerator operation. In a heterodyne digital receiver, one source of phase error is the thermal variation of the input stage. We have developed a technique to calibrate this drift. A CW calibration signal is sent through the same components together with the RF signal to measure and compensate the component drift. At intermediate frequency (IF), we use FPGA based digital signal processing to measure and reconstruct the RF signal after applying appropriate correction. Using this technique, we can measure the phase of a 2856 MHz signal with an accuracy of 15 milli-degrees. We describe how this approach is applied to the femtosecond timing distribution system.

INTRODUCTION

We developed a high precision phase measurement technique by using a live calibration signal to compensate for the thermal effect on the input stage of heterodyne receiver. This technique can be applied in a timing system, a low-level RF controller, and potentially other accelerator subsystems. We used this technique in a femto-second timing distribution system and achieved ~20 fs timing jitter and drift between two RF receivers[1].

A simplified block diagram of the femtosecond timing distribution system is given in Figure 1.

An RF signal is distributed as a phase reference over the fiber link. At each end station, a receiver reconstructs the RF signal and maintains the jitter between two end stations at the tens-of-fs level.

At the transmitter side, we amplitude modulate the RF source onto the carrier light, which is from a CW laser in our case. The modulated light is transmitted through a single-mode fiber link to the end station. The phase delay variation of the signal on the fiber is measured by a frequency shifted Michelson interferometer.

At the receiver side, the RF signal is detected by a photodiode. As soon as the RF signal is peeled off from the light and enters components, including cables, mixers, etc., the thermal variation effect becomes significant.

We measure the RF signal phase by downconverting it to IF, then digitize the IF signal, and process it with an FPGA based signal process board. The LLRF4 board we are using was developed for the SNS low level RF system[2]. We describe the signal processing for the phase measurement in this paper.

A CW double sideband suppressed carrier (DSB-SC) signal is added onto the RF signal as a common mode

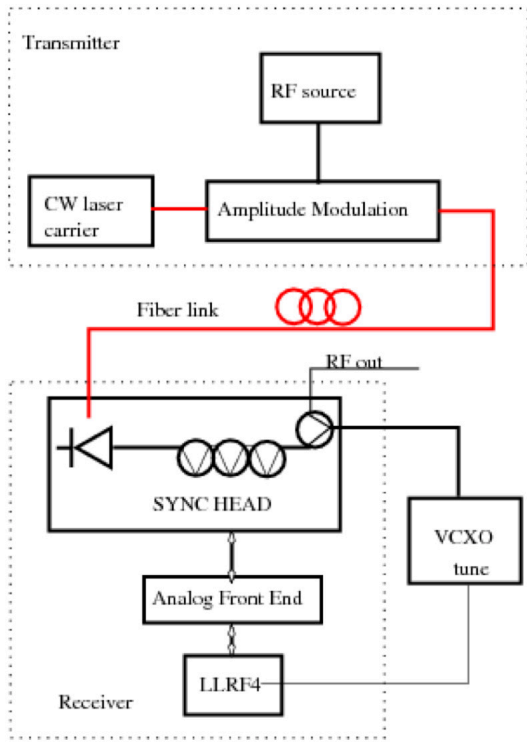

Figure 1: Simplified block diagram of the timing distribution system.

among both channels; we call it the calibration signal. The cable from the photodiode to the combiner is not included in the calibrated path, so that part needs to be temperature stabilized.

Physically, we split our receiver into a sync head, close to the device under control, and a stabilizer chassis, in a rack. The variation of the cable between them can be calibrated out. In the stabilizer chassis, an analog front end circuit downconverts the RF signal and upconverts the calibration signal. There is another bandpass filter on the LLRF4 board in front of the fast ADC.

After the signal is digitized, we measure the phase of each spectrum line in the signal and calculate the corrected RF phase accordingly.

We set up a simplified experiment to evaluate the out-of-loop error of our phase measurement, and the result was 15 mdeg at a 250 kHz sample rate.

ANALOG FRONT END CIRCUITS

We measure the phase difference between two signals: reference (REF) and signal (SIG).

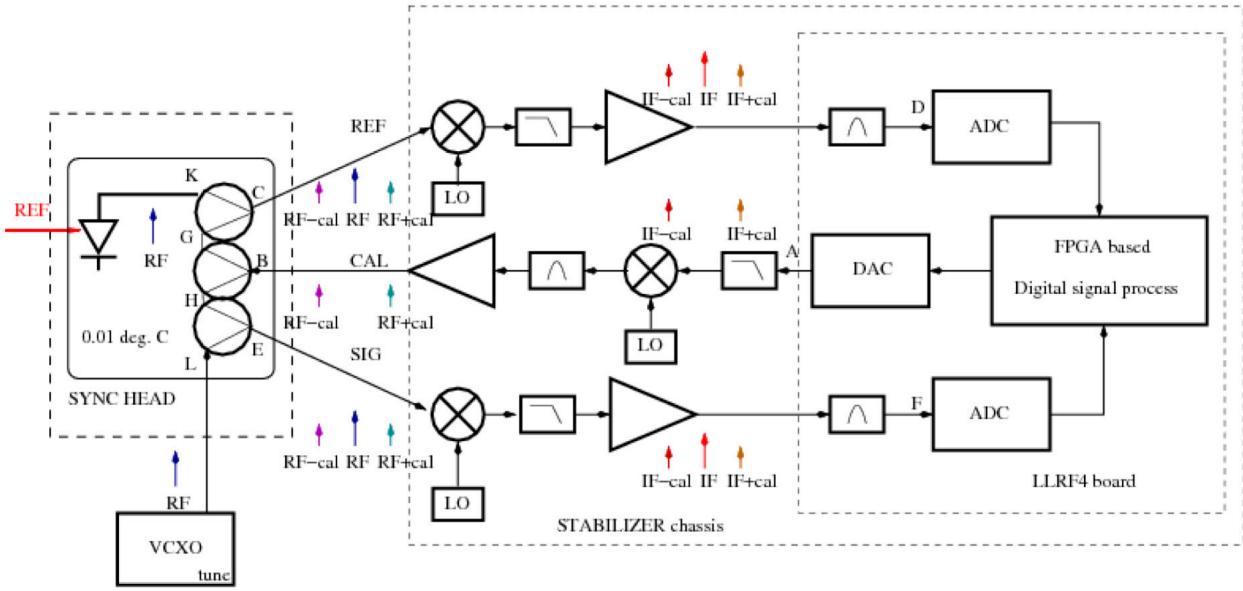

Figure 2: Analog front end circuits.

The analog front end circuit (Figure 2) contains two downconverter channels (REF and SIG) and one upconverter channel (CAL). The reference comes from the fiber link and the signal comes from a VCXO. We can further control the VCXO to follow the reference signal while we have the phase difference.

In the sync head, we have the RF detection photodiode and a combiner/splitter circuit to add the calibration signal onto the RF signal.

The photodiode output and the VCXO output contain only the RF signal. These RF signals are downconverted to IF by the mixer and filters as usual. A DSB-SC calibration signal co-propagated with the RF signal from point C to D as well as E to F. The DSB-SC signal is synthesized by the DAC and upconverted by the mixer. The phase delay from A to B is common to both the REF channel and the SIG channel.

The phase delay on the path BGC-BHE-KC-LE cannot be canceled, so we put them in a temperature controlled box to keep their phase delay variations as small as possible. The in-loop temperature error of our control loop is less than 0.01˚ C.

After the combination of RF signal and calibration signal, we have 3 spectrum lines propagating through the cable, mixer, amplifiers and filters. The intermodulation among them by the nonlinear effects of components will generate a new spectrum line. To minimize this effect, we select high-IP3 components in our system, and lower the signal power going to the mixer as much as possible and boost it up later. We also scan the whole spectrum in software to make sure the intermodulation products are low enough. Temperature control of all the analog front end circuit was added at first, but eventually we found that is not really necessary for meeting our specifications.

The LO phase noise is not critical here, since it is common to both channels and the differential calculation process eliminates it.

After the mixer and low pass filter, the signal contains IF and two sidebands separated by the calibration frequency. The IF power level is adjusted to a range appropriate for the ADC.

DIGITAL SIGNAL PROCESSING

The digital signal processing in phase measurement detects the phase of each spectrum line and then calculates the phase difference between REF and SIG.

The signal being digitized contains multiple frequencies. They are sent to a series of mixers to detect the phase of each spectrum line relative to the LO.

Each phase detector contains a mixer and a low pass filter as shown in Figure 3. The mixer can be implemented directly by a multiplier or by a Coordinate Rotation Digital Computer (CORDIC). The low pass filter (LPF) is implemented by a Cascaded Integrator

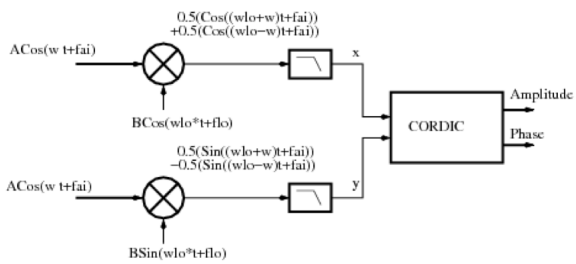

Figure 2: Unit circuit to detect signal phase relative to LO

Comb (CIC) filter. The mixer LO port is used to select the spectrum line to be measured. Ideally, only when the $w=w_{lo}$ does the LPF have nonzero output.

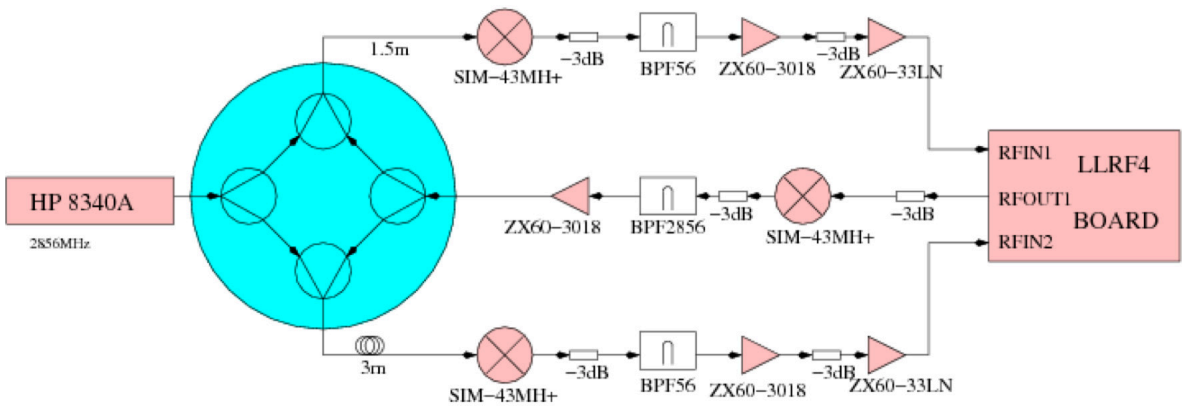

Figure 3: Out of loop test experiment setup.

After the mixer and LPF, the x and y values of each spectrum line are converted to amplitude and phase by another CORDIC. To achieve higher accuracy, the x and y are shifted together to make their MSBs are not all zero. Then we feed the result into the CORDIC. The shift does not affect the phase calculation, but for the amplitude calculation, we need to shift it back afterward.

The phases of the two calibration sidebands are detected independently; the amplitude of those spectrum lines does not affect the phase result.

When we have the phase of sideband calibration signals and RF signal for both the REF and the SIG channels, we can calculate the phase difference by

$$\phi_{REF,SIG} = (\phi_{RF,REF} - \phi_{RF,SIG}) - (\phi_{CALU,REF} - \phi_{CALU,SIG})/2 - (\phi_{CALL,REF} - \phi_{CALL,SIG})/2$$

where REF and SIG represent two channels, CALU represents the RF, and CALL represent the RF signal and upper and lower calibration sideband.

Considering a linear phase system, the phase delay of the RF is equal to the average phase delay of the two sidebands. Since the all the phase wrap around 2π, there is a π ambiguity when averaging two phases. We can resolve that by checking the phase difference of the upper and lower sidebands.

Here we assume the electric path from the photodiode to the ADC does not change by an extent comparable to a half wavelength of the calibration signal.

OUT OF LOOP TEST

We set up an experiment as shown in Figure 4 to test the phase detector out-of-loop error. A simplified sync head containing only 3 splitters is temperature controlled to 0.01˚ C (in loop temperature error). A 2856 MHz RF signal is split in the same temperature controlled box and fed the input of the sync head.

The cable lengths between the sync head and the analog front end circuit are different for the two channels (1.5 and 3 m) so as to be able to pick up some thermal expansion on the cable. The cable is in a room where an air conditioner regulates room temperature every 2 hours, and the peak to peak temperature variation is about 2˚ C.

The test is measuring the out of loop phase difference before and after we apply the calibration signal. We are trying to measure the difference of the same signal split to two channels. Ideally, we should get, as the result, zero phase difference between two channels.

The test result is shown in Figure 5. The red line is the uncorrected phase difference between the two detected RF signal, which followed the room temperature variation. The green line is the corrected phase difference between the two detected RF signals, which flattened all the temperature related fluctuations.

The live calibration process suppressed the rms value of the phase difference between the two channels from 0.142˚ to 0.015˚, which limited our phase detection accuracy.

If we did 128 more averages, which implies decreasing our sample rate from 250 kHz to 1.95 kHz, the rms value could even decrease to 0.003˚.

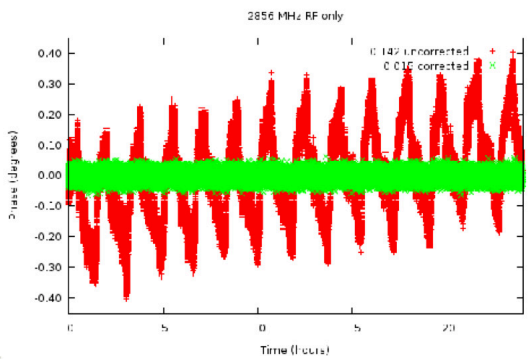

Figure 4: Out of loop test experiment data.

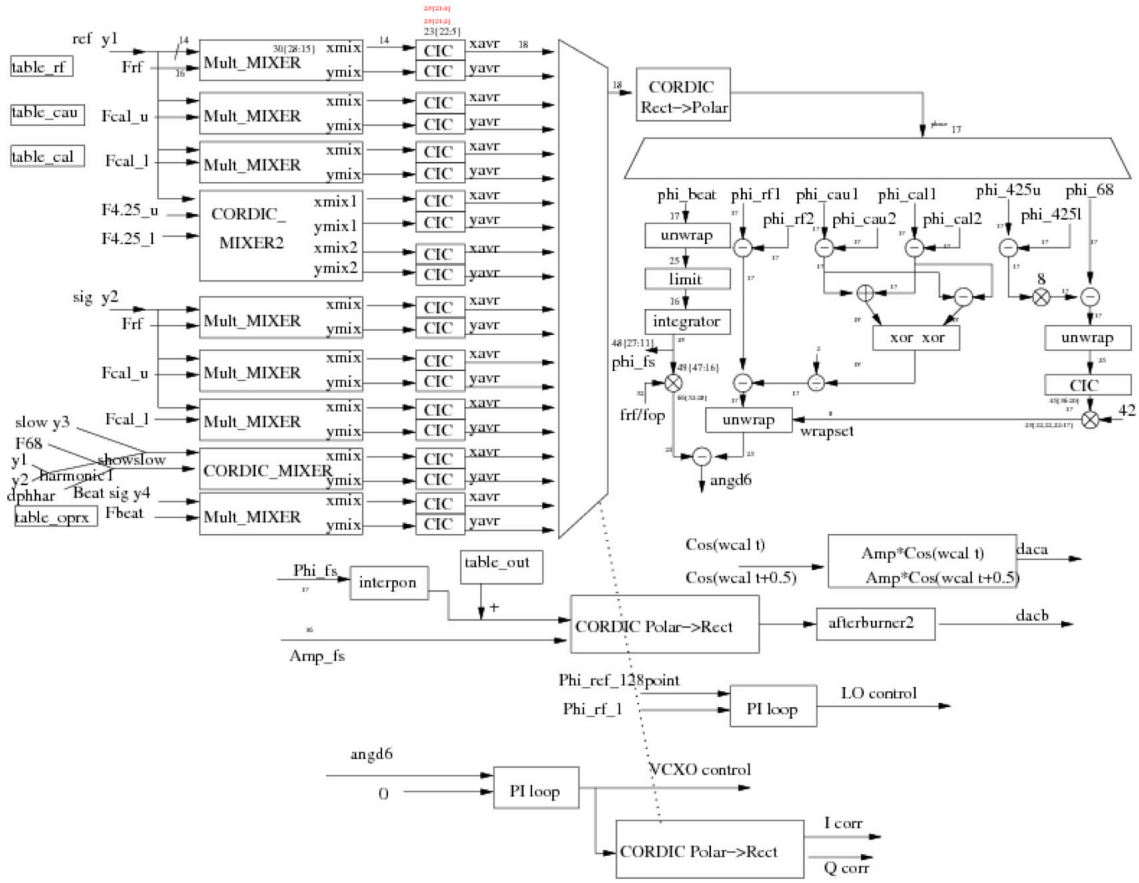

Figure 5: DSP for fs timing distribution system at LCLS.

APPLICATION IN FEMTOSECOND TIMING DISTRIBUTION SYSTEM

This high precision phase measurement technique is applied in the femtosecond timing distribution system.

The phase difference between the reference coming from the fiber and the harmonic signal coming from the laser is detected by the phase measurement system. The the error signal is sent to a PI loop to control the pico motor and piezo transformer [3].

Figure 6 shows the block diagram of digital signal processing for the timing distribution system.

Y1 is the reference signal. Beside the RF signal and calibration signal, it has another pair of sidebands, which are used to transfer another lower frequency (4.25 MHz) clock. By using this frequency, we can resolve the bucket ambiguity.

We tested such a timing distribution system at LCLS in SLAC. The jitter and drift from the out of loop test is about 20 fs.

REFERENCES

[1] R. Wilcox, J. M. Byrd, L. Doolittle, G. Huang, J. Staples, Optics Letters, Vol. 34, No. 20, 2009 (3050).

[2] http://recycle.lbl.gov/llrf4.

[3] J. Byrd, L. Doolittle, J. Arthur etc. Femtosecond Synchronization of Laser Systems for the LCLS, these Proceedings.