# A NEW, PXI BUS BASED, PATTERN MEMORY SYSTEM FOR THE SIAM PHOTON SOURCE

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*Abstract*

A new pattern memory system has been built from PXI bus modules to ramp the booster synchrotron magnet and RF power supplies, replacing an old and proprietary Toshiba system. The new system is compact, rugged, easy to program using LabVIEW, easy to repair and low cost.

## INTRODUCTION

The SPS is a modified ring which was previously SORTEC [1]. The pattern memory system for the booster was the original and proprietary system custom made by Toshiba. This old system can be considered obsolete as finding any replacement parts if difficult if not impossible. As there are no spare parts available or detailed system description we were faced with a maintenance problem for this critical sub-system and we decided to look for a replacement system well before we had a failure. One of the main requirements was that it be easily repairable from commercially available replacement modules or components.

Most existing synchrotron facilities use many VME crates and modules and therefore historically VME based pattern memory systems have been used typically. We have no such history of using VME here and a lower cost modular PXI National Instruments based Pattern Memory System has been applied to replace the (much larger) Toshiba one. We believe that this is the first time that a synchrotron facility has utilized a PXI based pattern memory system.

## DEVELOPMENT OF THE NEW PXI BASED SYSTEM

The old Toshiba system provides eight, 16 bit plus strobes, RS 422 differential outputs to the Bending Magnet power supply (3), Quadrupole power supplies (4) and RF power supply (1) of the booster synchrotron. To provide differential output at the RS422 levels to the power supplies we chose the National Instruments model PXI-6534 digital I/O waveform generator with 32 Mb onboard memory for pattern storage. This module has 32 single ended outputs which we configured as 16 differential outputs by programming. As each set of 16 bit outputs also needs a strobe signal one more 6534 module was used to provide the eight differential strobe outputs.

Initially the system concept was tested with just two 6534 modules, one outputting signals to the RF power supply, which only needed one set of 16 bit input signals, and another 6534 module for outputting the strobe signals and inputting the main trigger signal from our timing system. This test worked perfectly the first time. Figure 3 shows the input data stream and the output signals of the RF amplifier over one synchrotron injection and ramping cycle.

After the successful system concept test a complete new pattern memory system was purchased comprising of nine PXI-6534 modules, one 18 slot PXI-1045 19" chassis and one CPU controller module, a PXI-8186 P4 2.2 GHz running Windows XP. This controller has an Ethernet interface which was used to connect to our control system server for remote operation as well as for downloading the magnet and RF pattern data to the 6534 waveform generators.

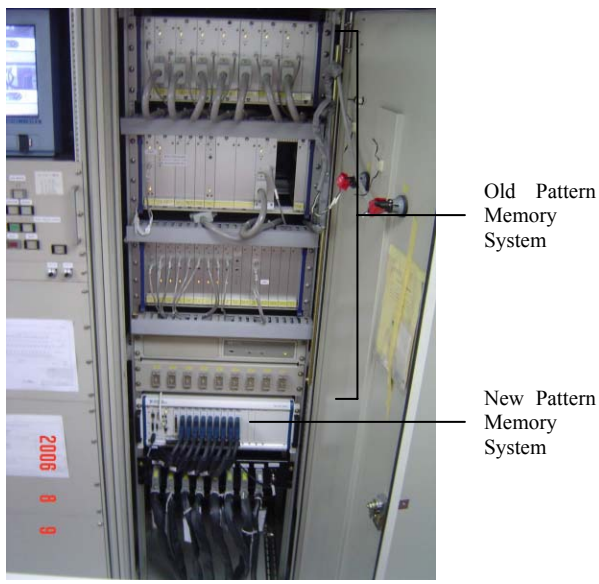


Figure 1 : Both old and new Pattern Memory Systems.

The whole system was configured, programmed and installed in the same Toshiba rack, see Fig. 1. Switching from the old system to the new system is done by simply unplugging the eight outputs from the Toshiba system and inserting them into the National Instruments system shown in Fig. 2. The Toshiba system is, for the time being, kept as a spare and eventually we shall remove it completely.

The ramping pattern is created and stored in the control server as 7001, 16 bit words for each power supply. The ramping time of the booster is 700.1mS so the data, after transfer to the digital I/O module memories, is sent during ramping to the power supplies at the rate of one word per 100 microseconds or 10kHz. This exactly emulates the old Toshiba timing although the new pattern memory can transfer data at much higher rates (up to 20MHz) allowing for the possibility of upgrading the system in the future.

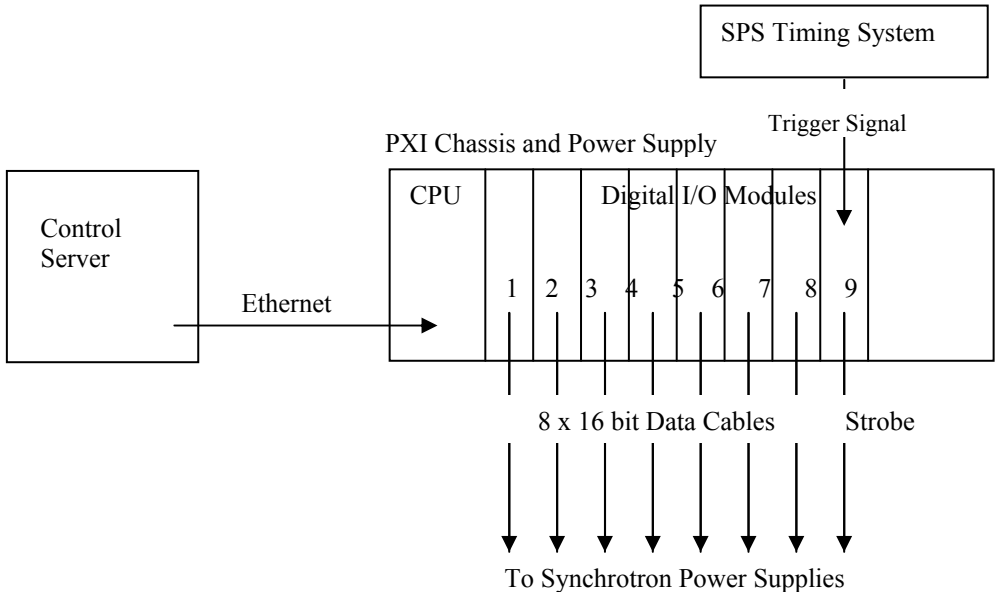


Figure 2: The NSRC built PXI Based Pattern Memory System.

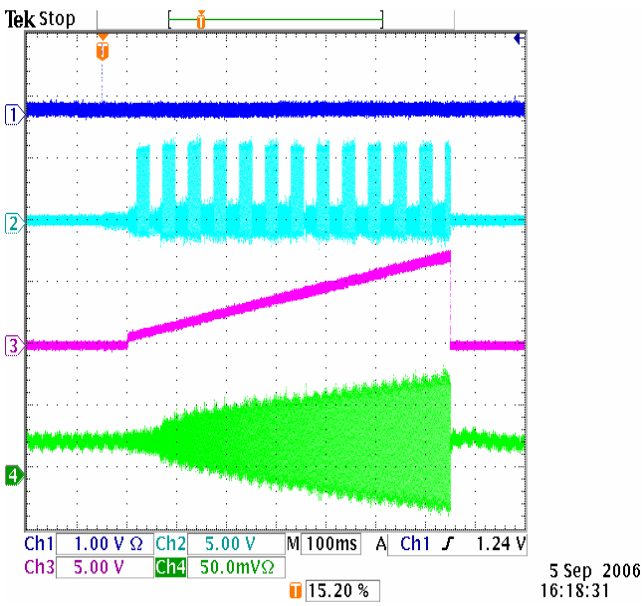


Figure 3: Input and output signals of the synchrotron RF amplifier system. Channel 1, the 1 cycle trigger signal. Channel 2, PM data output example. Channel 3 RF voltage envelope generated by the data. Channel 4, the RF signal at 118MHz.

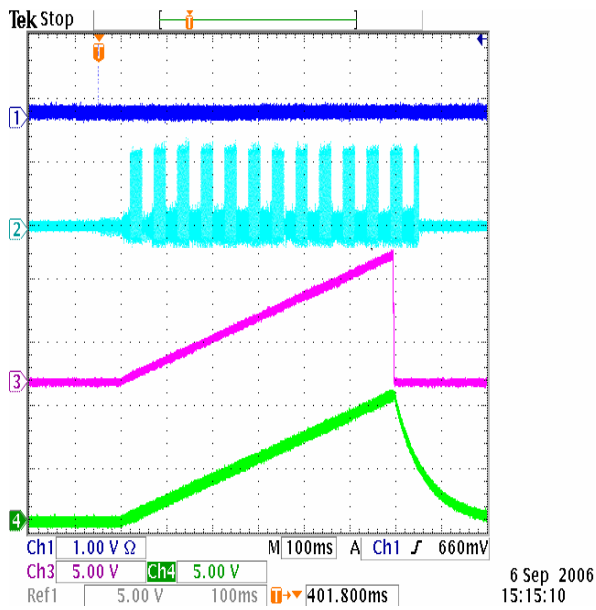


Figure 4: Input and output signals of the synchrotron bending magnet power supply. Channel 1, The 1 cycle trigger signal. Channel 2, PM data output example. Channel 3, Current reference envelope generated from PM data. Channel 4, Bending magnet current.

Table 1: Comparison of old and new pattern memory systems at NSRC.

| System | Control & Data Bus | Memory | Programming | Cost ($) | Size (mm) |
|---|---|---|---|---|---|
| Toshiba 1985 | Proprietary | 100KB | Difficult | 500,000 | 2000H<br>570W<br>850D |
| NSRC PXI-based 2006 | PXI | 32MB | Easy, LabVIEW | 20,000 | 117H<br>446W<br>435D |

The memory used, 14 Kbytes, is also much less than the 32 Mbytes capability of the new memory modules leaving ample for any upgrade. The ramp repetition rate is presently 0.5 Hz controlled by the SPS timing system trigger signal.

Figure 4 shows the input and output signals of the synchrotron bending magnet power supply. Table 1. is a comparison chart of the old and new pattern memory systems used at NSRC. The new system is a very cost effective solution to our potential maintenance problem.

## SUMMARY

A new PXI bus based pattern memory has been commissioned for the SPS booster synchrotron. The new system is compact, rugged, easy to program using LabVIEW, easy to repair and low cost. It is now used as the primary pattern memory and has been used successfully continuously for the past six months.

## ACKNOWLEDGEMENTS

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## REFERENCES

[1] A New Timing System for the Siam Photon Source, Isoyama, G, Kawasima, Y., Hoyes, G., Attaphibarl, M., Pimol, P., Saguansak, N., Rujirawat, S., Apiwatwaja, R., Boonanan, L. and Pairsuwan, W. (2001). Proceedings of the 13th Symposium on Accelerator Science.