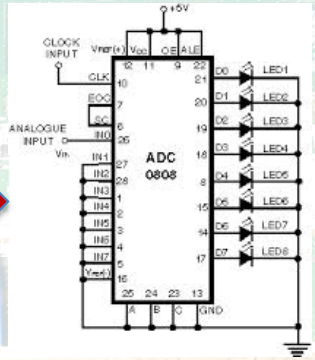
The Digital RF Control Revolution

Curt Hovater



Outline

- RF Control Challenges ….Why?
- How We Got Here …..Some History
- Hardware
  - Receiver …Transmitter
  - FPGA/DSP
- Pulsed RF
- CW RF
- Ring RF
- Algorithms, Tools, Features
- Summary

RF Control Challenges/Starting Points

- **Required Field Control to meet accelerator performance:**
  - **Proton/ion Accelerators/Rings: 0.5^{o} and 0.5%**
  - **Nuclear Physics Accelerators: 0.1^{o} and 0.05%**
  - **Light Source: 0.01^{o} and 0.01%**
- **Loaded *Q* Optimized for beam loading:**

  Nuclear Physics < 1 mA,

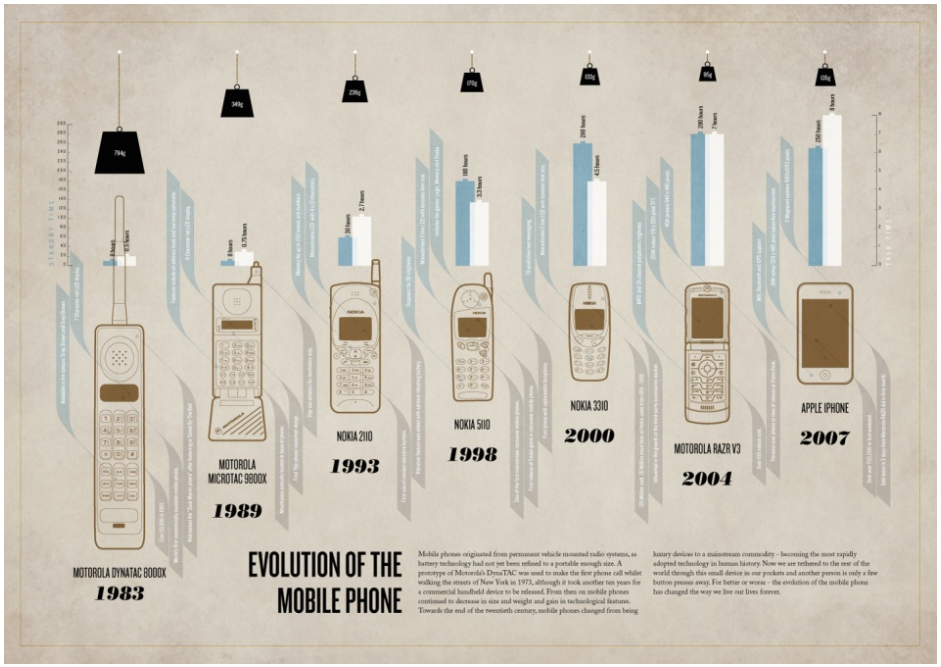
  ERLs close to zero net current

  Light Sources 10's of μA to 100 mA (Rings/high current in injectors)
- **Microphonics & Lorentz Detuning: Determined by cavity/cryomodule design and background environment.**
- **Master Oscillator/Timing/Synchronization: Determined by application (light sources < 100 fs, frequently < 20 fs).**
- **Accelerator Specific: Operational, Reliability/Maintainability Access etc.**

External Factors Pushing Digital Control

Commercial and Defense Electronics drives technology becomes cheaper, smaller and easier to use

- Personal Computers
- Cell Phones
- Networks
- Universities
  - Accelerator scientists and engineers trained in DSP in the 70/80's

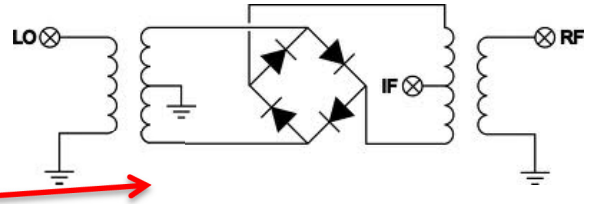


30+ Years

RF Control History

LLRF Pre ~ 1990

- Analog Receiver
- Analog signal processing.
- Phase detector was a double balanced mixer.
- Amplitude detector was “hot” carrier or Schottky diode
- Typically separate Phase and amplitude control



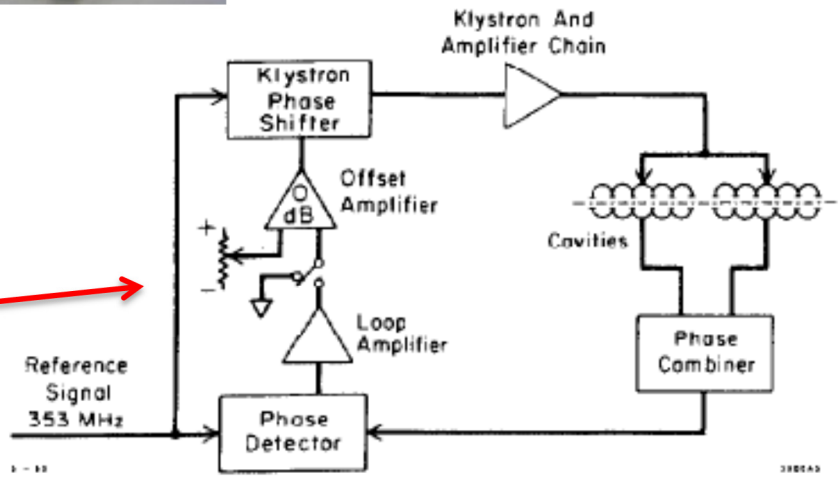


Fig. 4. Circuit of the phase control loop.

CONTROL ELECTRONICS OF THE PEP RF SYSTEM

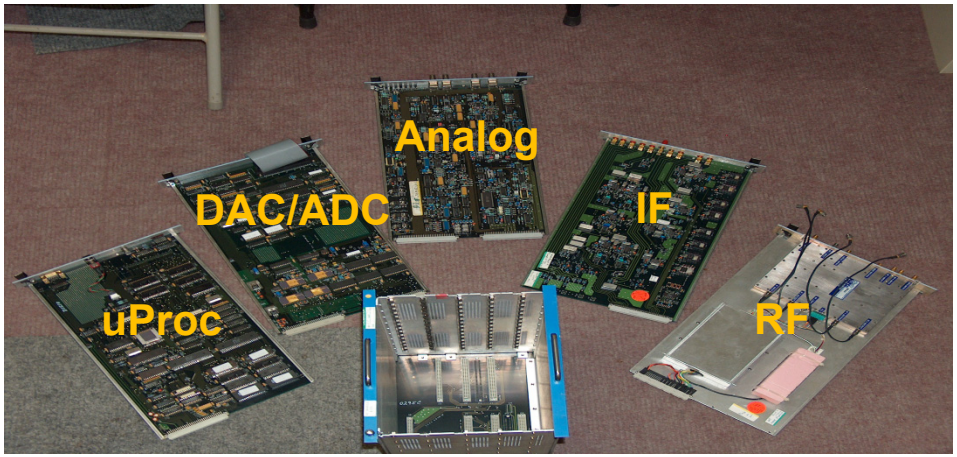
J.-L. Pellegrin and H. Schwarz
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

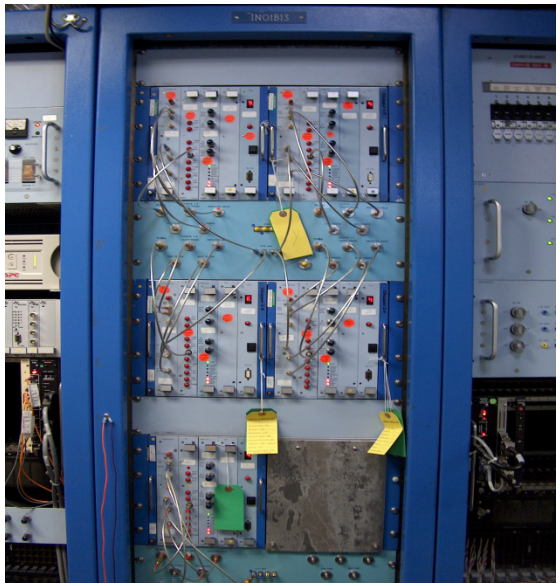
Analog Components suffered from dynamic range, linearity and temperature variation issues.

Reference [J.-L. Pellegrin and H, Schwarz, J. Fugitt]

CEBAF Hybrid System Circa 1992

- **CEBAF system utilizes analog signal processing with Intel 186 processor to correct offsets and drifts**



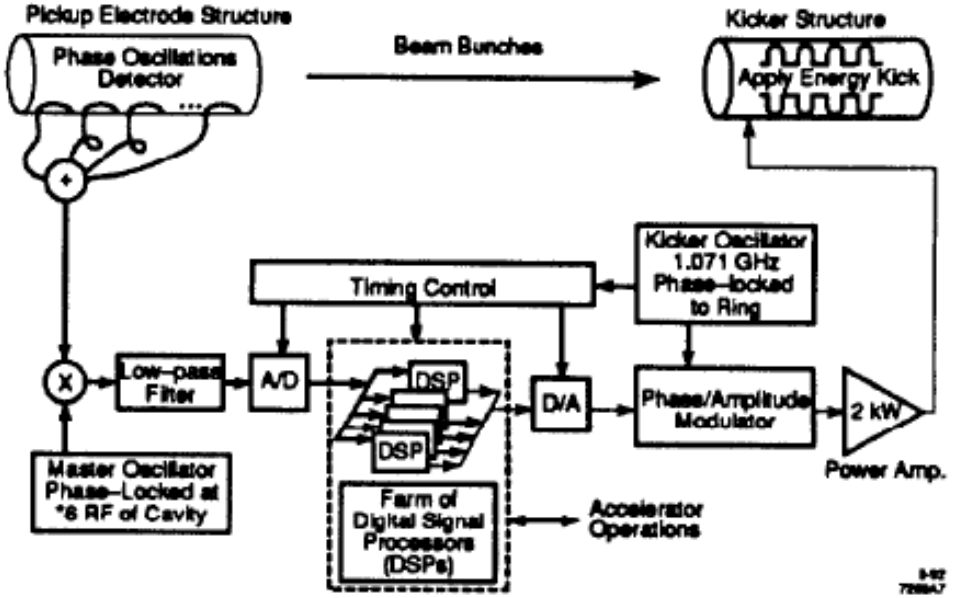


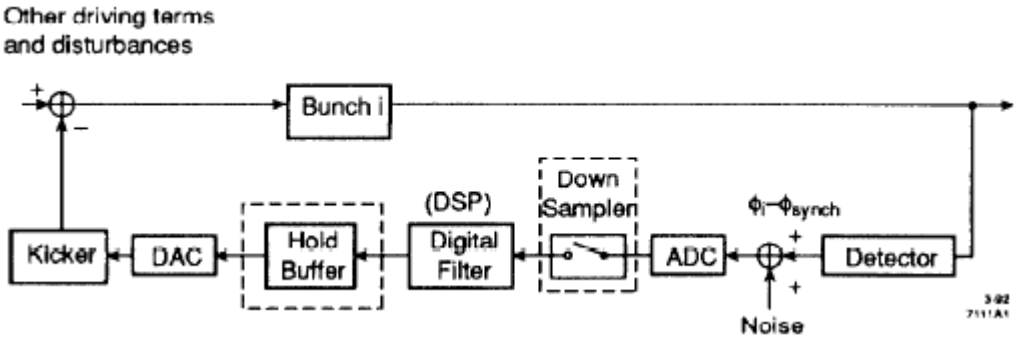
- **RF Transceiver**
- **IF Signal processing**
- **Analog Feedback**
- **I/O: DAC/ADC**
- **Intel 186 μProc for simple drift correction and communication to CAMAC**

Reference [S. Simrock]

Early Work: Digital Signal Processing (DSP)

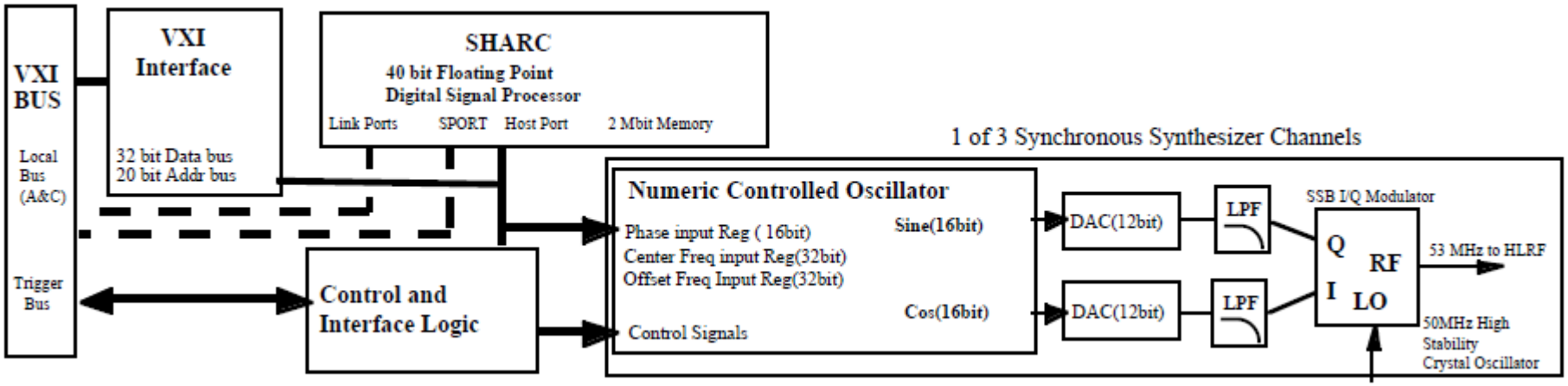
- With the growth of faster and cheaper microprocessors, designers started to look at ways to to take advantage of DSP.
- First efforts were in beam based feedback
  - ~'92 Fox, Hindi at SLAC use Digital Signal processing in implementing a bunch by bunch feedback system





Reference [H, Hindi]

Early Work: FERMI LLRF



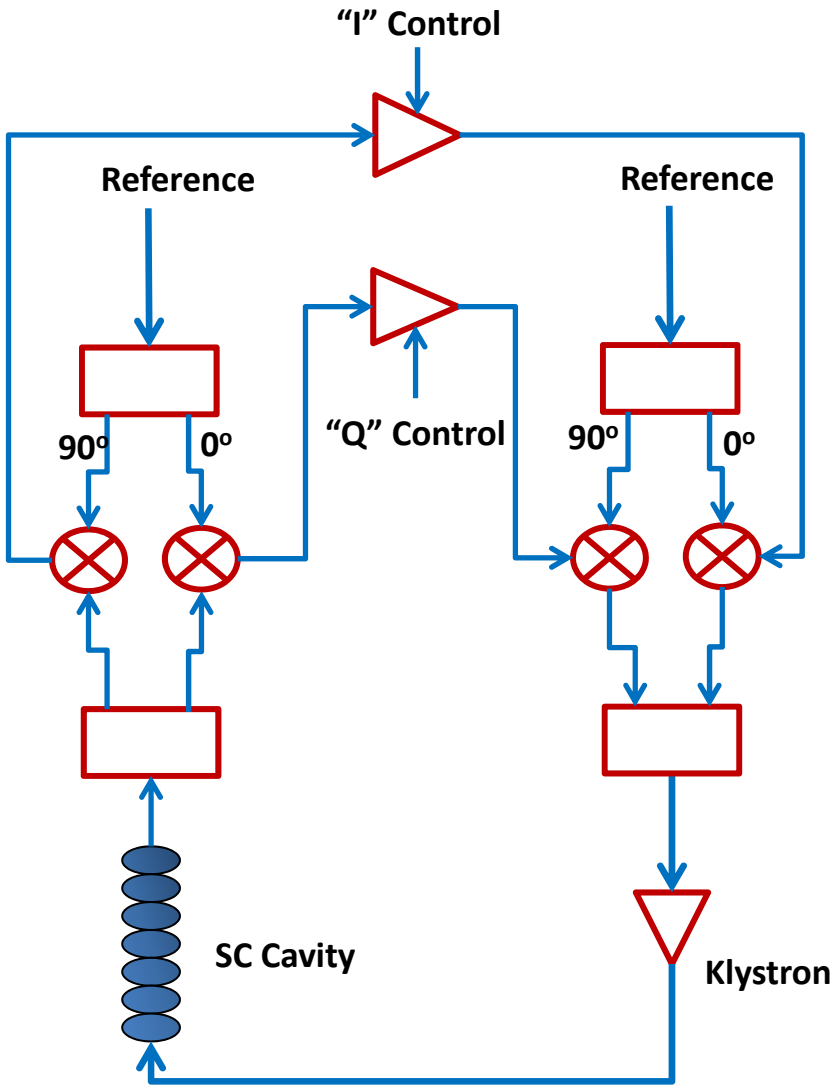
- ~ '95 Chase et al developed a DSP LLRF system for use on the Main ring at Fermi Lab.
- Featured a Direct Digital Synthesizer (DDS) VXI module that could generate three channels of frequency and phase modulation.
- The new digital hardware replaced an analog system that had limited range and improved the phase noise in the RF system.
- System still relied on Analog components to get the signal to dc ….slow enough to digitize

Reference [B. Chase]

The Digital Receiver and Transmitter

I&Q: A Different View of Field Control

- Quadrature Phase –Shift Keying (QPSK) became a communication standard for increasing channel bandwidth
- Separates an RF carrier into quadrature components (real and imaginary …In-phase and Quadrature)
- 1975-1990 Scientists/Engineers at LANL/CERN/ANL (Jachim, Boussard, Delayen) devise method to control cavities using elements of analog I&Q
- Next step is Digitization (once the digital hardware speeds caught up.)



Reference [Couch]

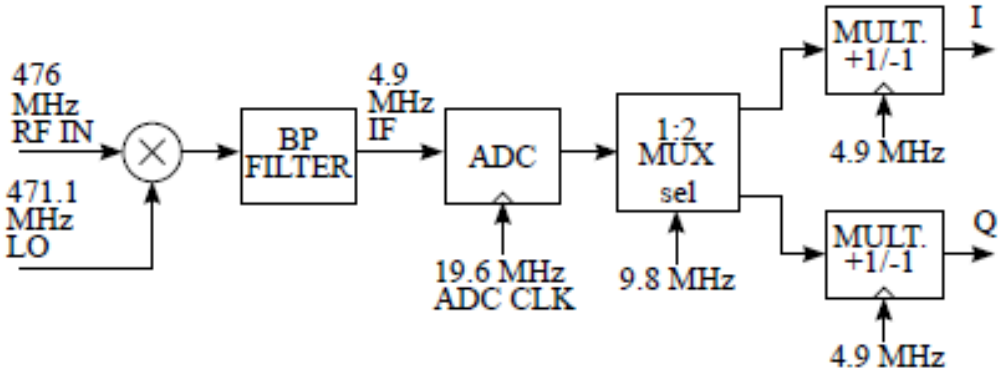
A to D Conversion: Quadrature Sampling

- The two issues with analog signal processing were
  - The susceptibility to drifts and non-linearity a deal breaker as accelerators needed increased field control and timing precision.
  - No flexibility or automated adaptability

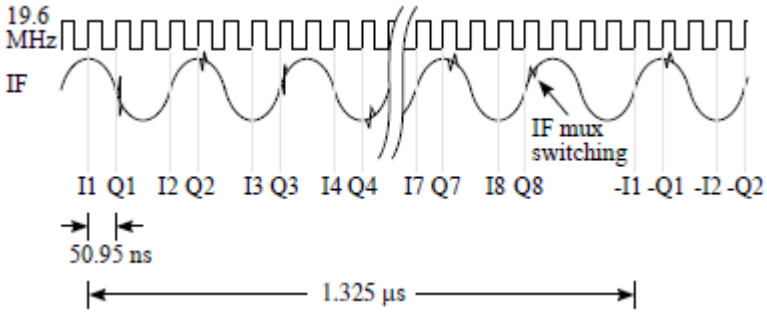
- Solution was to quadrature sample the RF/IF signal using a fast ADC.
- Easily implemented as ADC bandwidths became larger (> 1MHz) when using precision clocks
- A simple digital mux is then used to separate quadrature components (I and Q)
- Since cavity field information is in the digital domain and infinite amount of digital signal processing, control algorithms can now be used.

The Fuse is Lit ….Direct Digital Sampling

- ~'94 Chris Ziomek and Paul Corredoura at PEP-II (SLAC) design first RF control system using direct digital sampling.
- The control algorithm was then implemented in in a VXI crate using a digital signal processor.



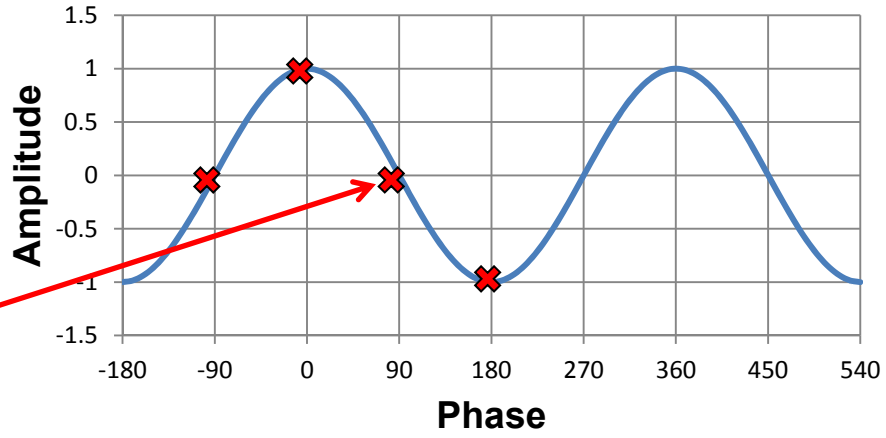
Digital I/Q Demodulator

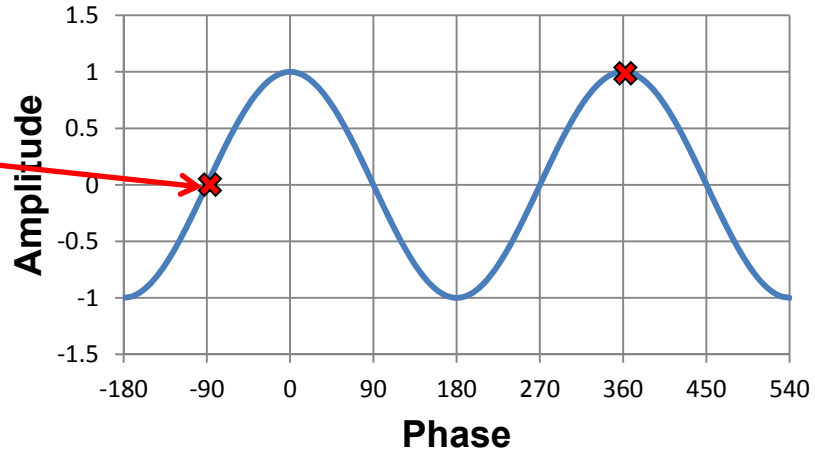


Time Response of I/Q Sampling

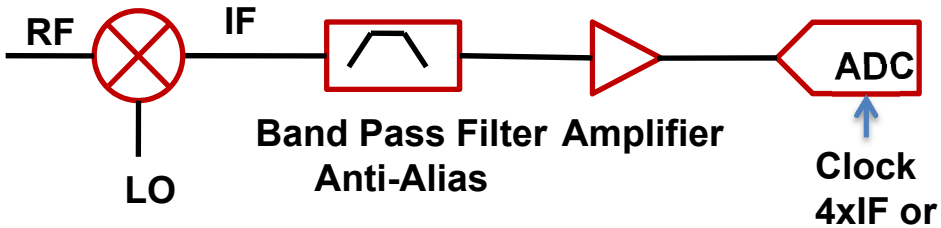
Digital Quadrature Sampling

- Sample a frequency at four points
- Can either harmonic sample or sub harmonic
- Example: A signal at 50 MHz.
  - Harmonic Sampling frequency is 200 MHz
  - Sub-harmonic Sampling or 40 MHz (200/5)
- Easier to sample at lower frequencies

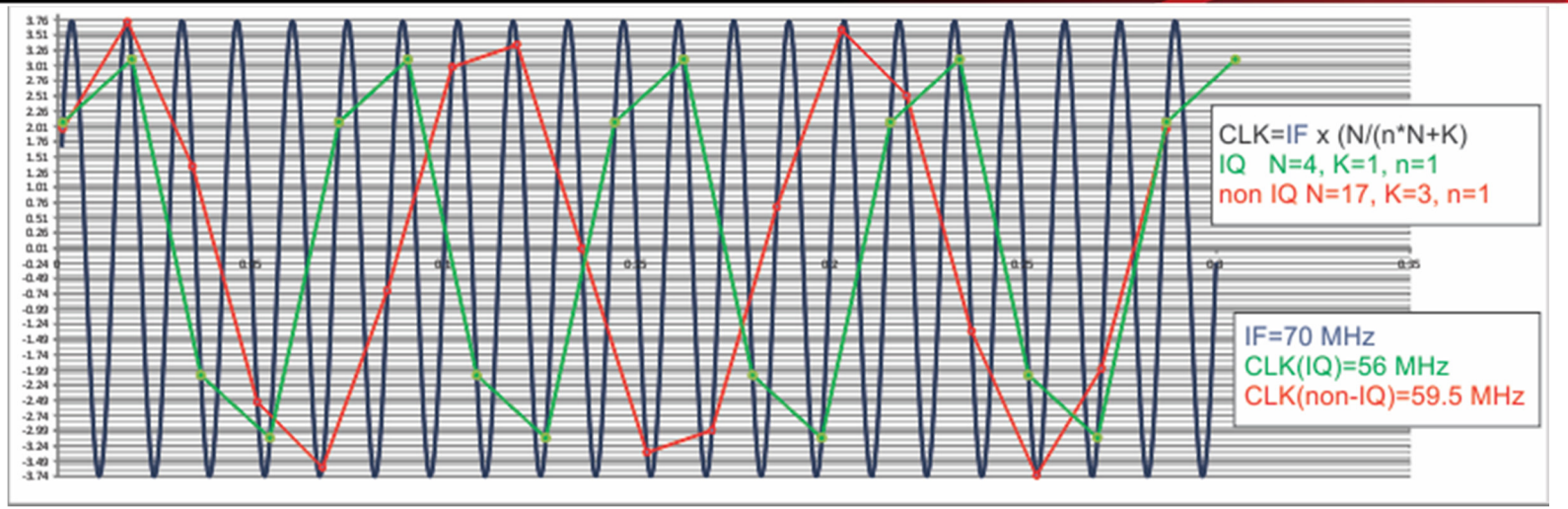




Digital I/Q Sampling using Clock



Better: Non Quadrature Sampling



- **In quadrature sampling the clock samples the same four points on the carrier (ADC range) – time domain explanation (see green dots)**
- **Because of this the non-linearity of the mixer and ADCs, generates odd harmonics which aliases with IF signal and become undistinguishable.**
- **In case of non quadrature sampling most harmonics do not line up with IF signal and can be filtered. Depends on the selected clock samples can use whole ADC range. (See red dots) From multiple (here 17) samples one can calculate I and Q**

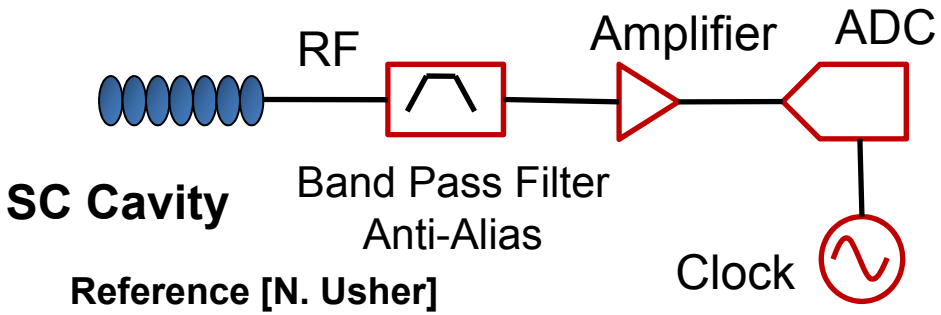
Reference [L. Doolittle, T. Plawski]

Eliminating The Analog Receiver: Direct Sampling

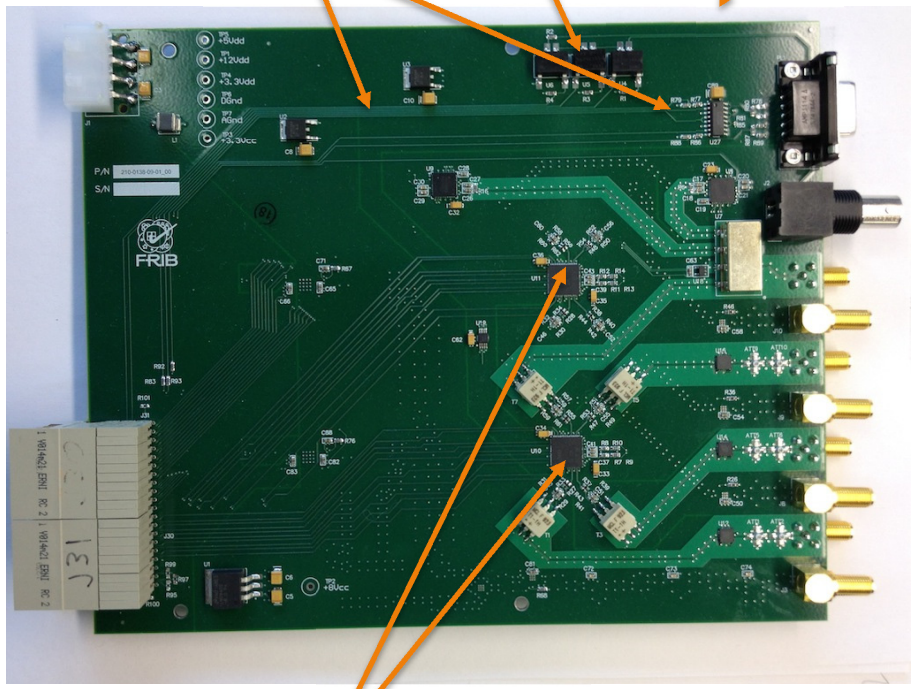
- Commercial ADC's bandwidths are 2 GHz
- No Mixer! Which is a source of system offsets and non-linearity
- Excellent option for field control specifications >0.5° and 0.1%
  - Proton and Ion accelerators!!

Benefits

- Economy …. $$$
- Simpler receiver for multiple frequencies
- Simpler Master Oscillator (MO) distribution



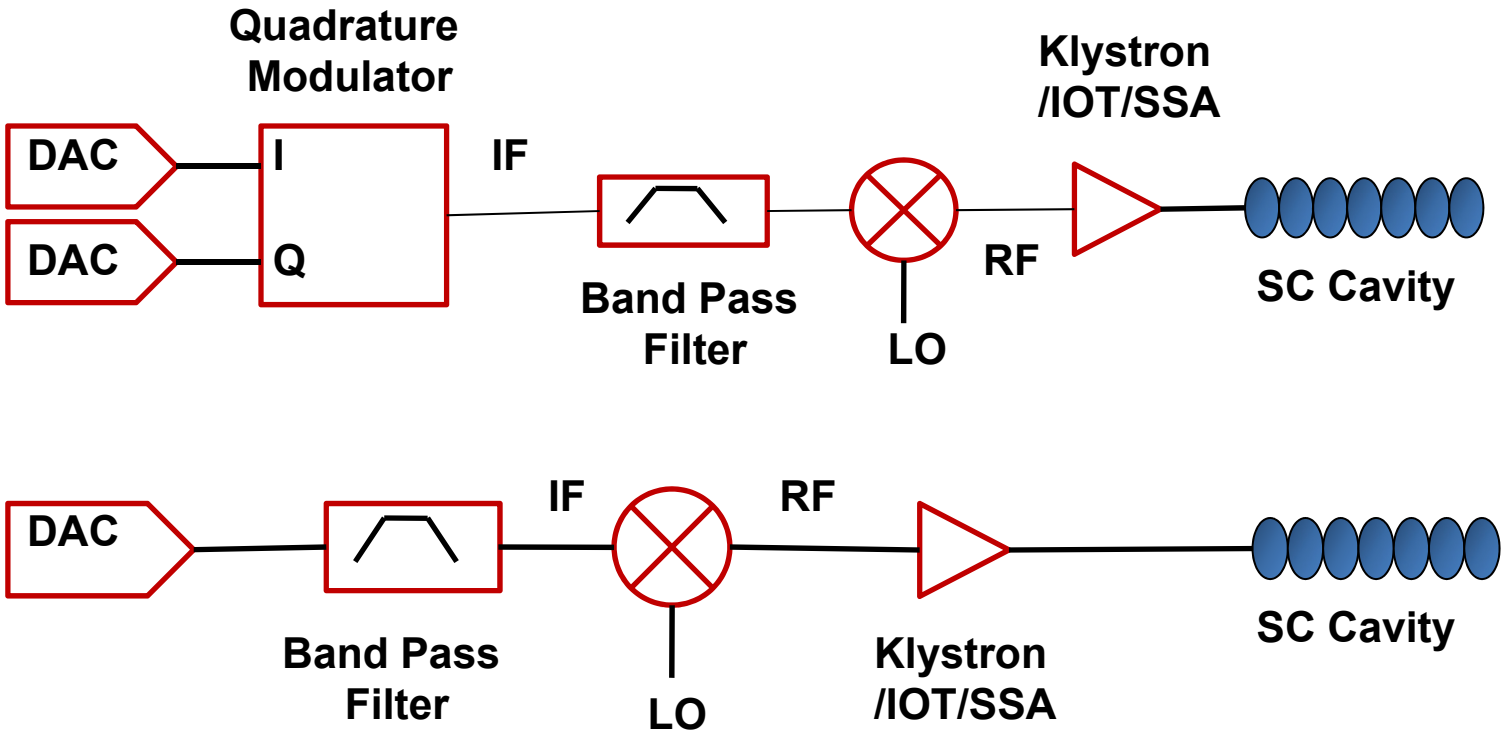
Reference [N. Usher]



FRIB RF Board NO Mixers !

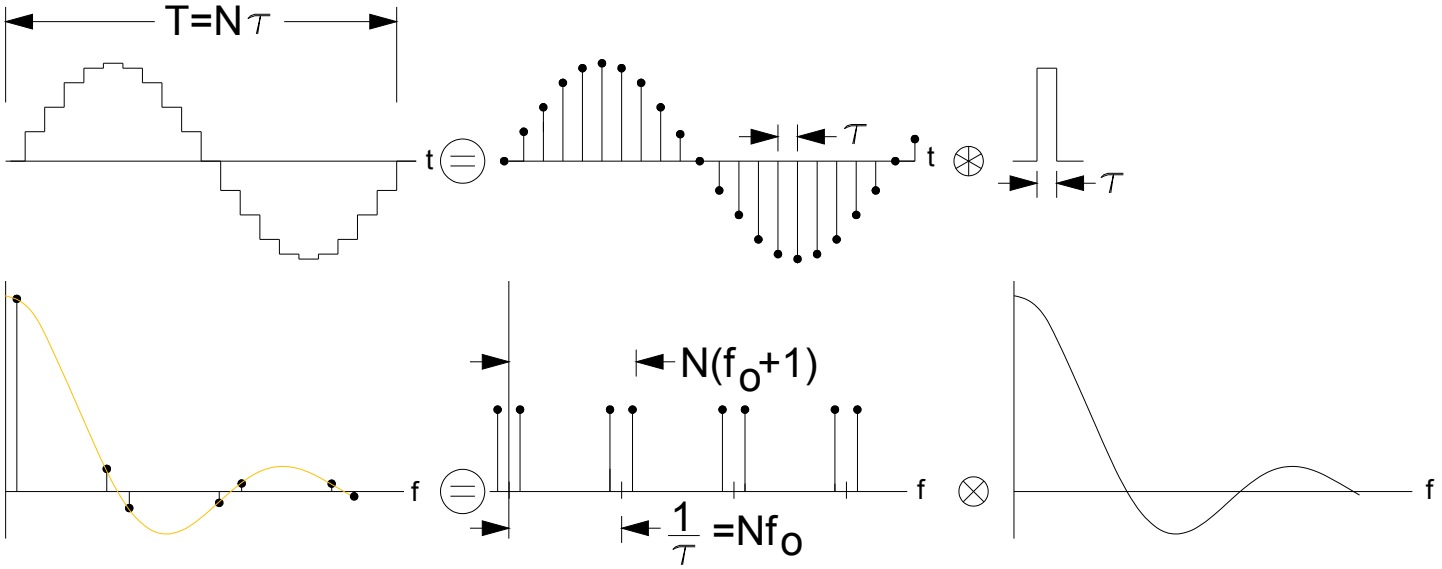
Transmitter/Up Conversion

- You still have to re-generate an analog signal to drive the amplifier-cavity system.
- Two ways to do it.



Direct Digital IF Signal Generation

Advantage: Single DAC can eliminate Quadrature Modulator



- **Concept use one of the harmonics out of your DAC for your IF frequency[12].**

- **One can show that the harmonic contains the proper phase signal and is:**

$$A\sin(2\pi f_0 + \varphi) \Rightarrow B_k A\sin(2\pi(kf_S \pm f_0)t + \varphi) \quad \text{where } k = 0, 1, 2 \ldots$$

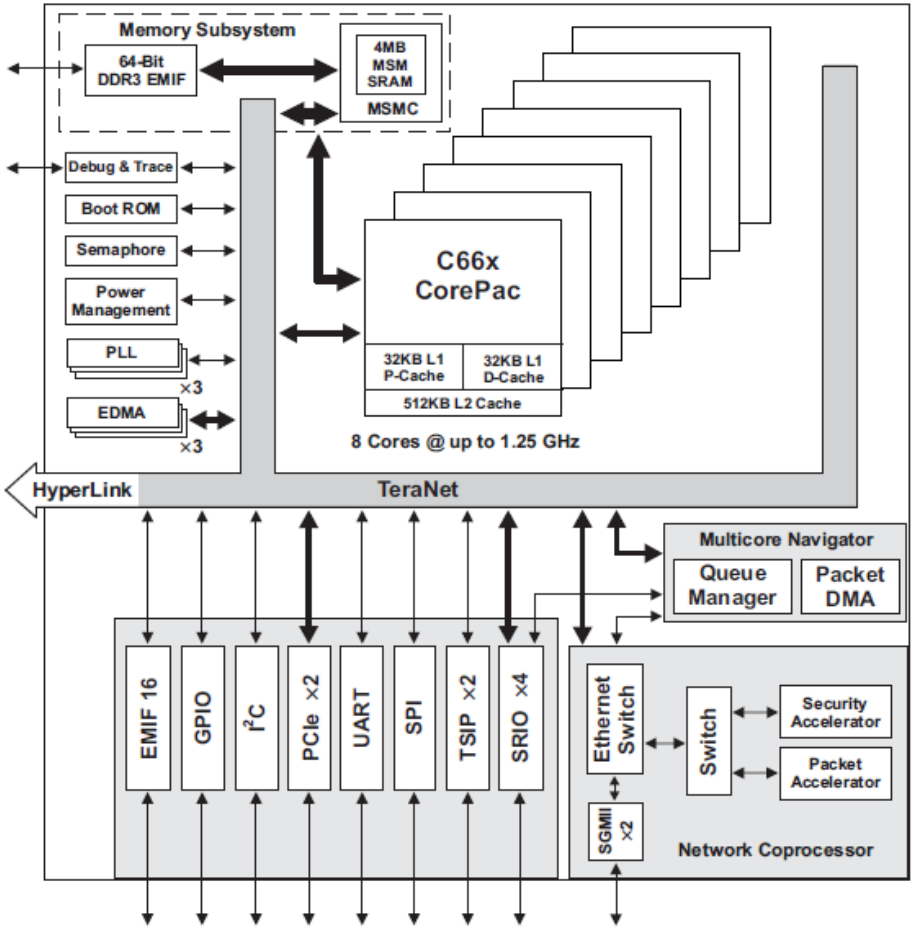
Reference [Doolittle]

Digital Engines

Digital Signal Processors

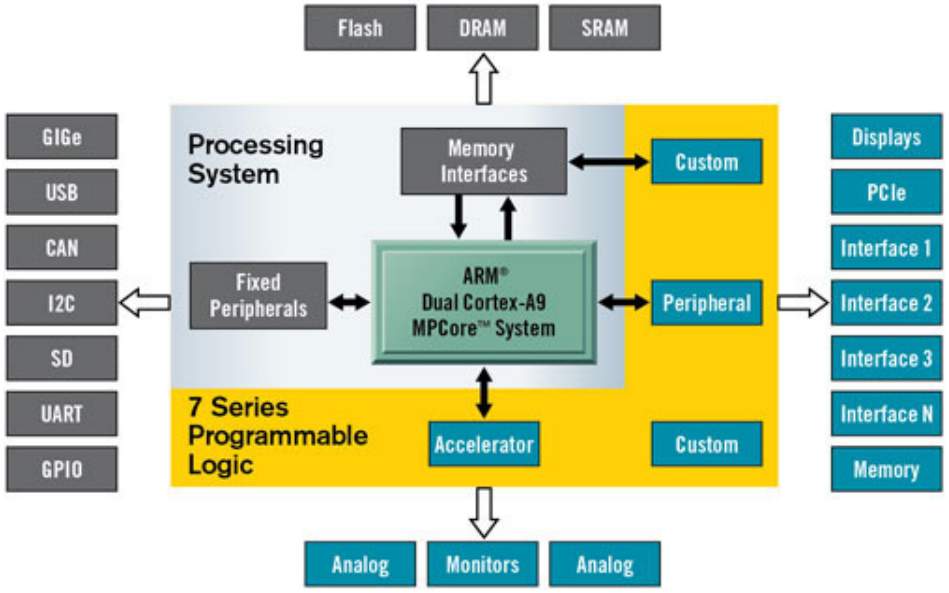
- Depending on the speed needed and the complexity of a control algorithm a dedicated digital signal processor may be used.
- Tend to be slower than an FPGA but more flexible.
- **Applications**
  - SNS RF Ring
  - DESY (TESLA) initially used a DSP for their pulsed multi-cavity designs.
  - Cornell LLRF has chosen to use a FPGA for the fast part of the algorithm and a DSP for the slower parts.

Block Diagram of a TMS320C6678



Field Programmable Gate Array

- The FPGA has been the engine of the conversion to digital control.
- As the chips became larger (more gates) and faster it became practical to actually build the DSP and feedback algorithms in logic.
- Soft-core and hard-core processors are also being implemented into the logic ….



Digital Signal Processing

FPGA or DSP?

- For fast processing Field Programmable Gate Array (FPGA) wins
- DSP a little more flexible but FPGAs not far behind (especially when married with a hardcore processor)

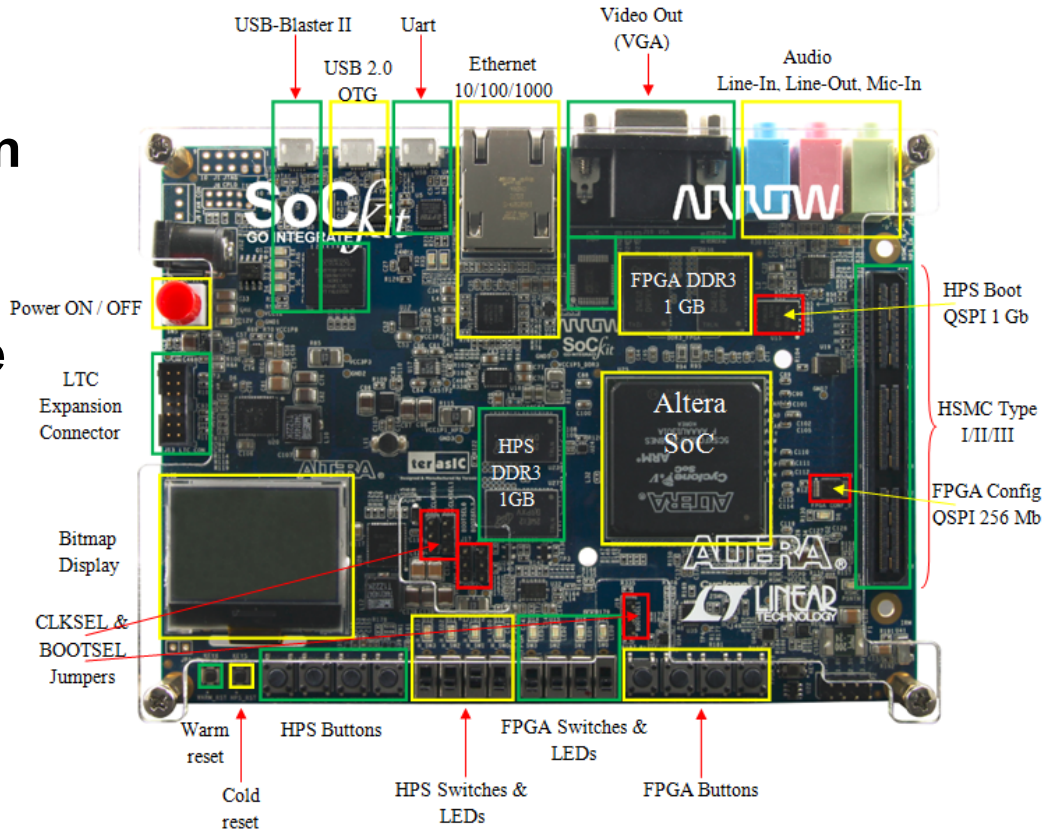
FPGA: Xilinx … Altera …. Both are used by the accelerator community

DSP: Texas Instruments …Analog Devices dominate industry

Digital version of Ford vs. Chevrolet!

Commercial FPGA Board "System on a Chip"

- As the gate count and options have increased, FPGA's are now hosting complete systems
- With dedicated μprocessors embedded into the FPGA it can now run Linux, Rtems, EPIC's etc.
- Designer now can concentrate on the I/O, ADC/DAC interface etc.
- Examples
  - BNL: Xilinx, PPC, VxWorks
  - FNAL: Altera, ARM, VxWorks
  - KEK: Xilinx, PPC, Linux



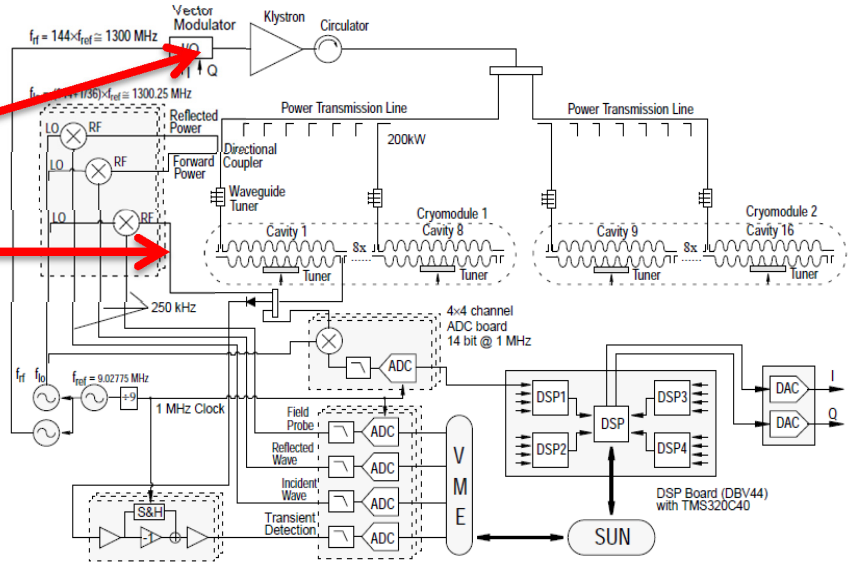
Commercial FPGA board that FNAL is using to design new instrumentation including LLRF

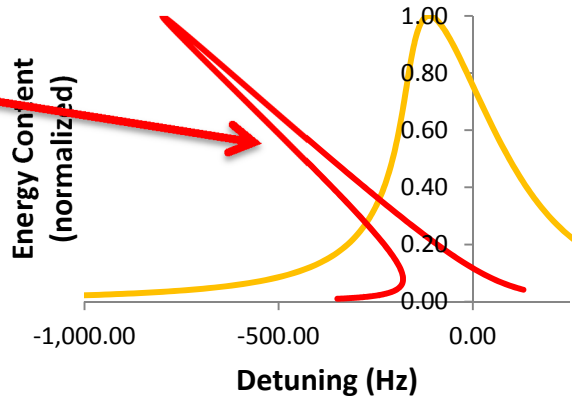
Reference [P. Varghese, K. Smith]

LLRF Applications

Pulsed RF: TESLA LLRF

- Beginning in the early 1990's work began on a sc linac for a collider
- For economical reasons the RF footprint was driven by a single pulsed amplifier driving multiple cavities [15]
- A digital RF system using vector sum was the preferred method for cavity control.
- Numerous LLRF challenges
  - Lorentz Detuning
  - Cavity Coupling
  - Different Emax
  - Cavity Phasing
- The initial TESLA work became the basis for LLRF for pulsed LINACs such as FLASH, XFEL ….ILC



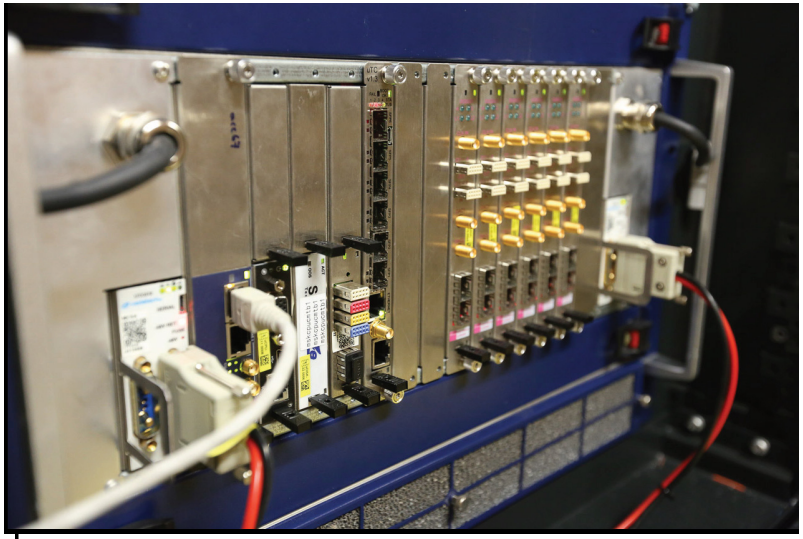


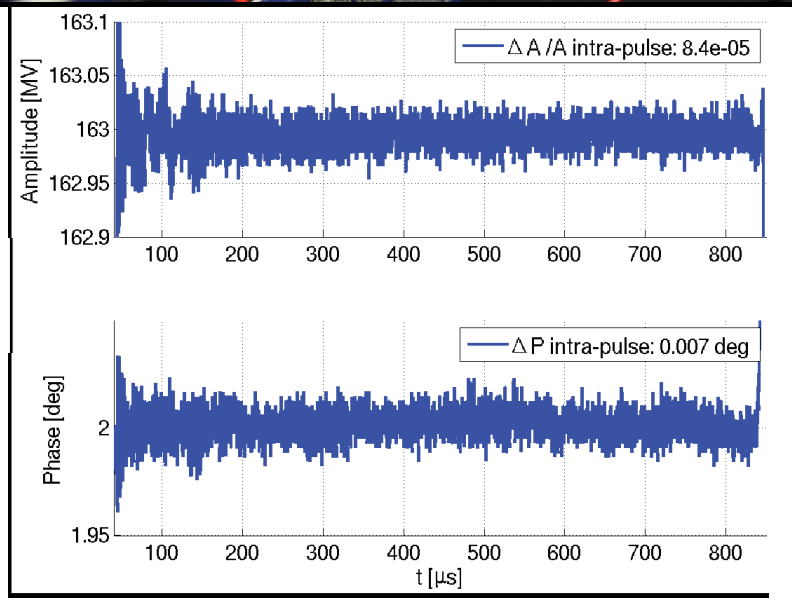
Reference [S Simrock]

Pulsed RF: FLASH-XFEL

- XFEL Vector sum must control up to 32 SC cavities
- In the design process DESY LLRF has migrated from DSPs to larger FPGAs
- They have investigated packaging formats,
  - VME,
  - ACTA
  - MTCA.4. based system
- The MTCA.4 format has demonstrated it can meet the specifications needed for the tight field control 0.01% and 0.01° required for the XFEL[16]

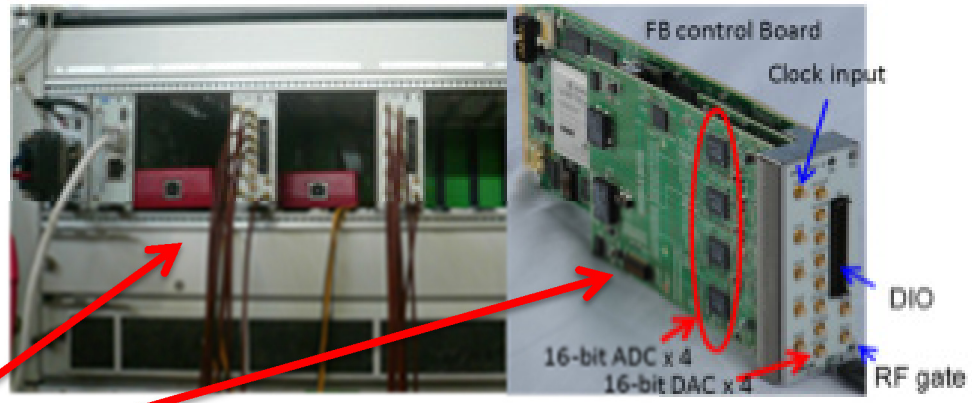
Reference [S, Simrock, C, Schmidt]



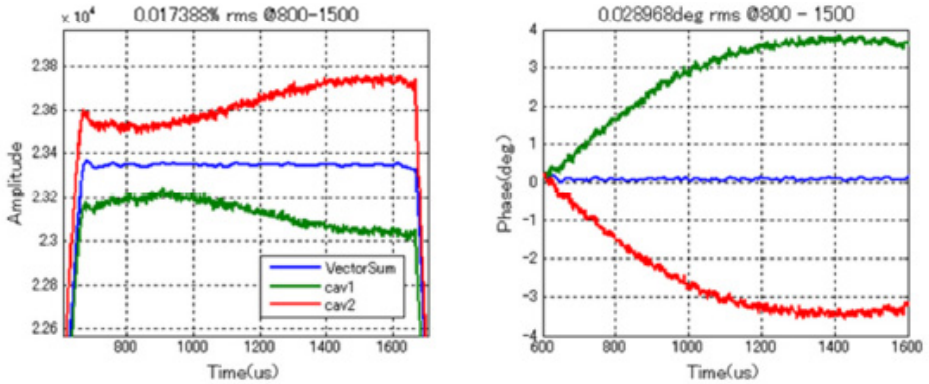


ILC LLRF Collaboration

- The feedback mechanism will be performed on Virtex-5 FPGA
- I/O: 16-bit ADCs and DACs.
- The card was designed in the form-factor of an advanced mezzanine card (AMC) for a
- Platform: MicroTCA.
- An embedded EPICS IOC on the PowerPC core in FPGA will provide the global controls through channel access (CA) protocol on the backplane interconnect of the shelf.



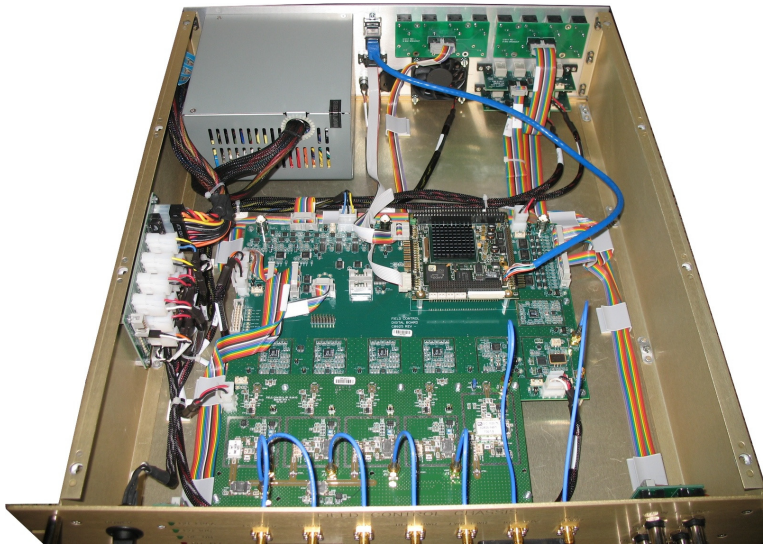
KEK



Result of amplitude and phase around flattop region using feedback and feed-forward

Reference [T, Miura]

CW LLRF: CEBAF

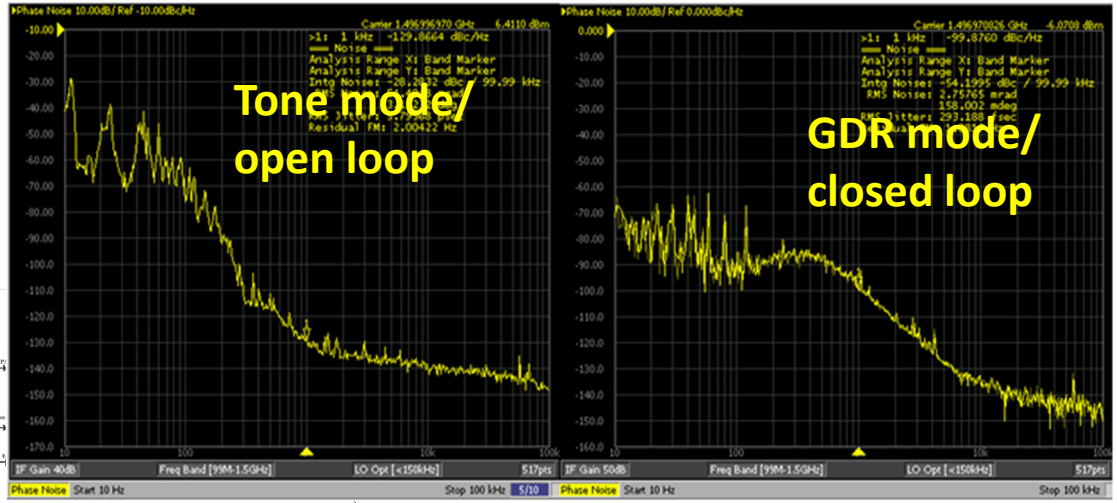


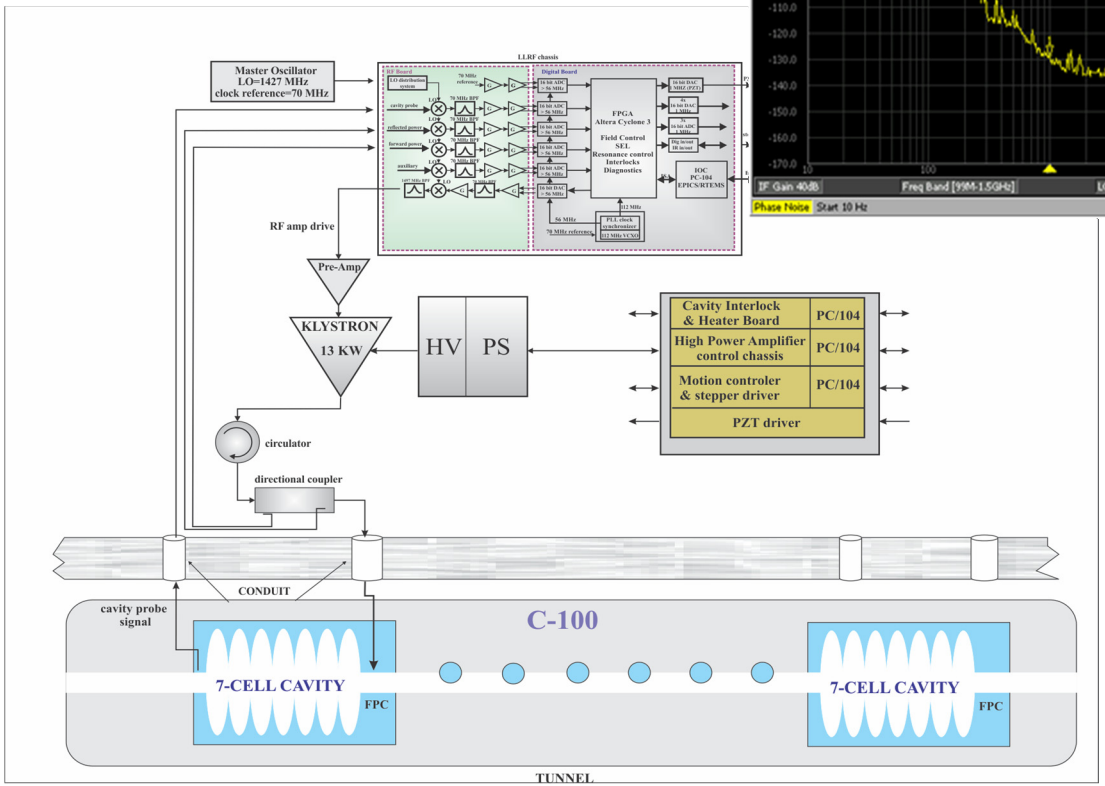
- "Pizza box" design (does not use a commercial package VME etc.)
- Designed for single cavity/single amplifier control
- Features
  - 4 Receivers, 1 Transmitter
  - Large Altera/Cyclone FPGA
  - EPICs IOC on board PC104
  - Digital card can mate with multiple RF front ends
  - Numerous I/O: analog and digital
  - Uses commercial PC power supply

Reference [C. Hovater]

CW LLRF: CEBAF 100 MV Cryomodule

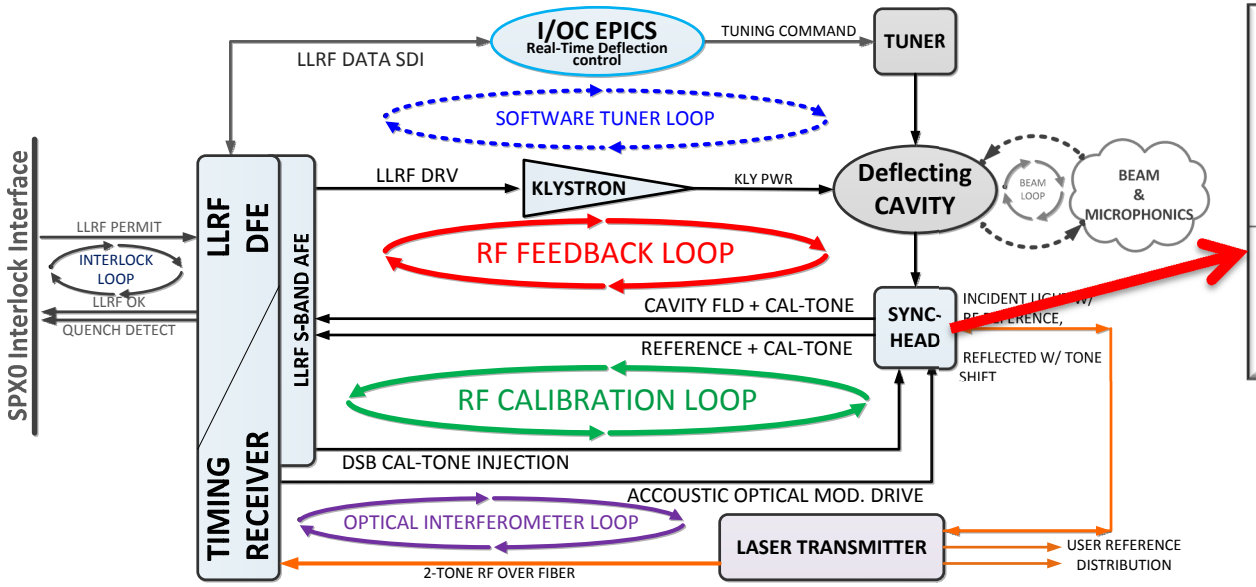
Typical CW SRF operation:
High QL (10^7+)
Gradients 15-20 MV/m
One power source/cavity

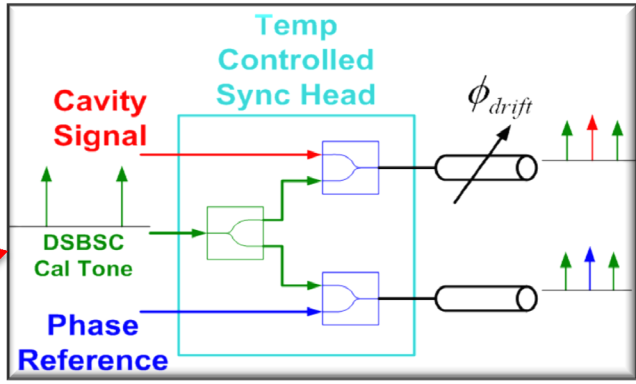




Phase noise spectral density for Tone Mode (< 3MV/m) and GDR (IQ regulation at 21 MV/m) mode
Phase control ~ 0.16 deg

CW LLRF: Precise Phase Control



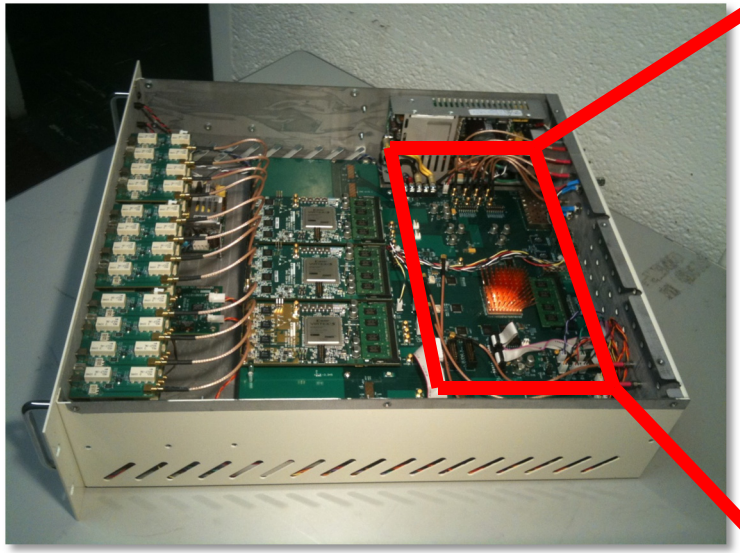


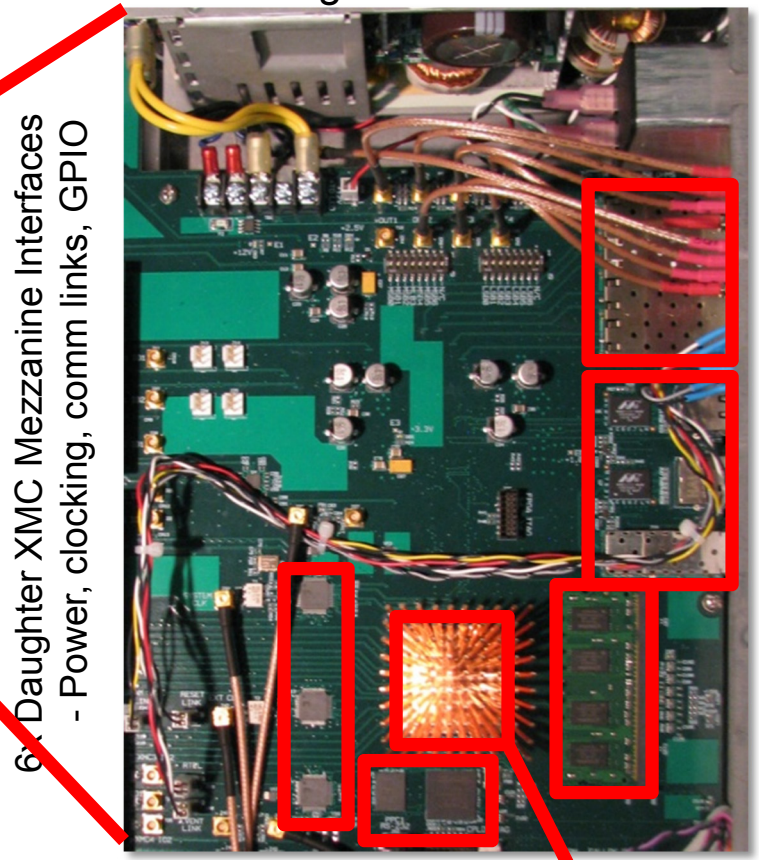
- **The Argonne SPX project requirements called for tight phase stability of 0.038 deg between two distant deflecting cryomodules**
- **The LBNL/ANL collaboration designed a LLRF system together with a precision fiber reference system**
- **The LLRF employed a pilot/cal. tone that was synched with the fiber reference the practically eliminated any aspect of temperature effects.**
- **A complicated continuous calibration scheme was made easy by gratuitous use of DSP!**

Reference[H. Ma]

RING RF: RHIC Modular Multipurpose System

The Carrier Board uses an embedded power pc running Vxworks on a Xilinx FPGA





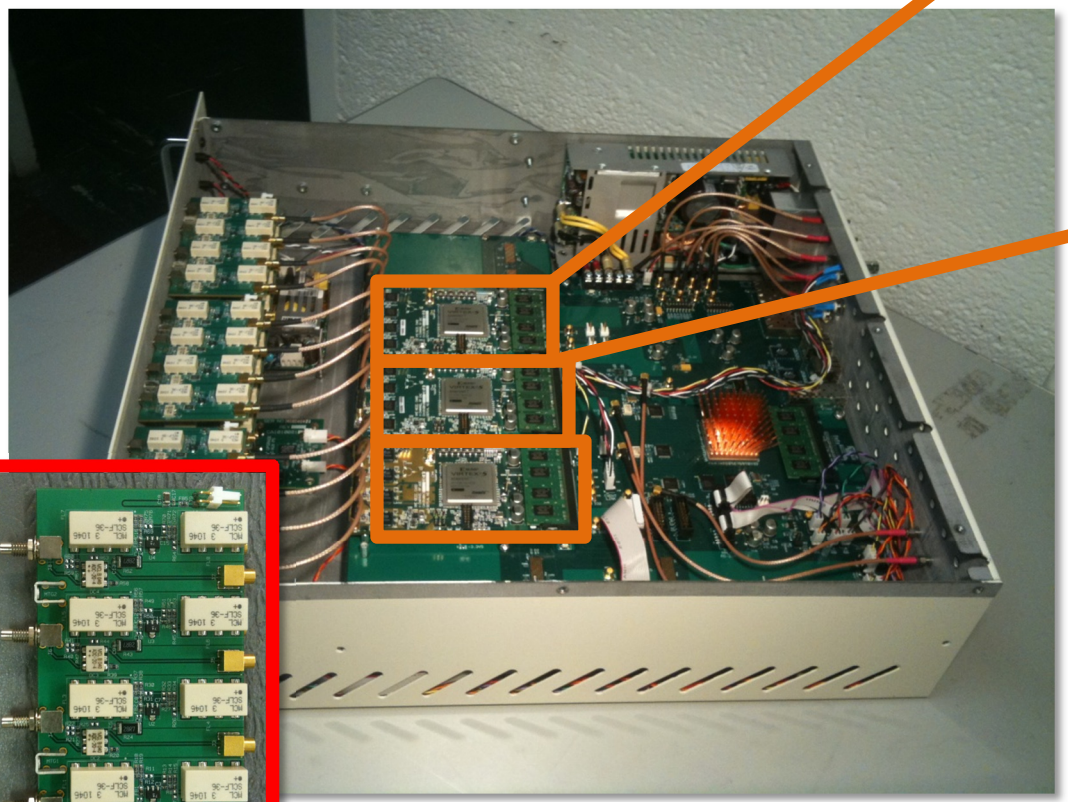
Hosts up to six custom or COTS daughter modules.

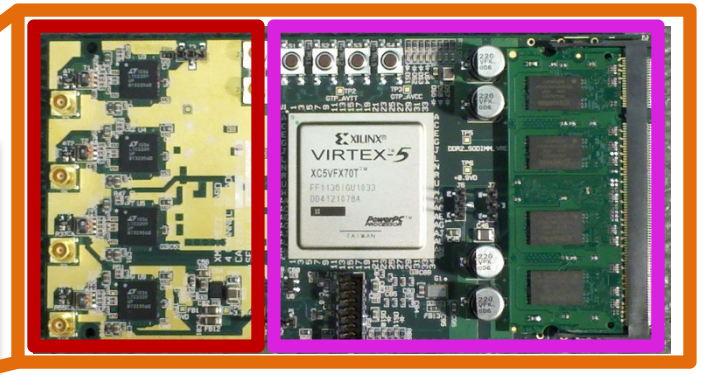
Supports internal functionality and external interfacing.

Reference [K. Smith et al]

RHIC : Daughter Cards

Daughter modules provide the application specific functionality for a particular system.





Reference [K. Smith and T. Hayes]

Analog filtering and buffering separated from daughter modules.
Considering active up/down conversion as well

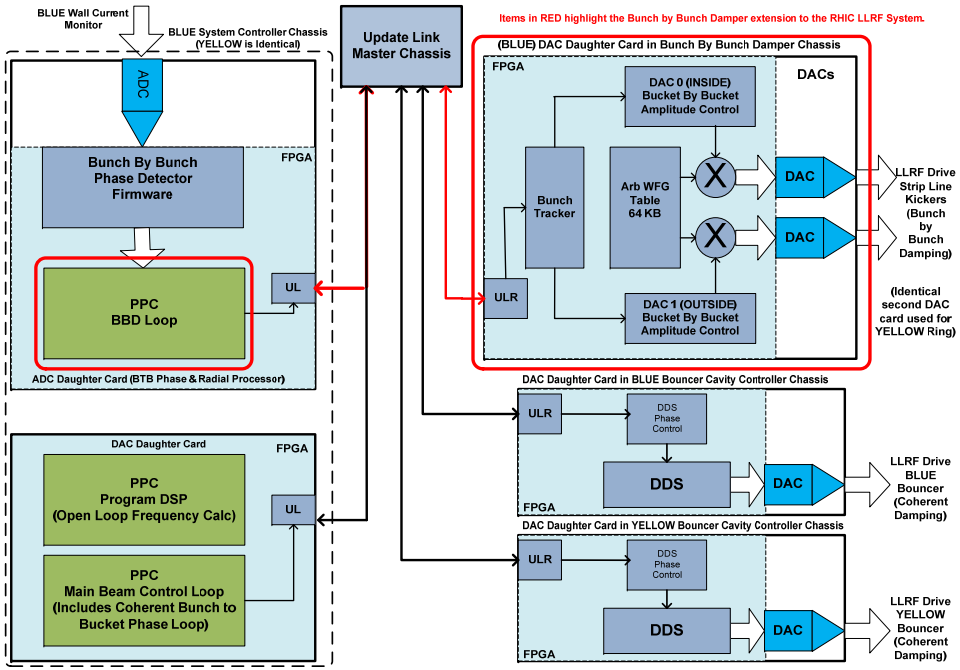
Currently have 3 modules
- 4 CH Wideband DAC (Maxim 5891)
- 4 CH Wideband ADC (LTC2209)
- RHIC Spin Flipper Module

Daughter modules differ only in their customized front end design.

Share a common back end design.
- FPGA based (Xilinx Virtex-5)
- Carrier Interface (XMC, VITA 42.X)
- Peripheral support (DDR2 SO-DIMM, Configuration FLASH, CPLD …)
- DC Power Supplies, etc.

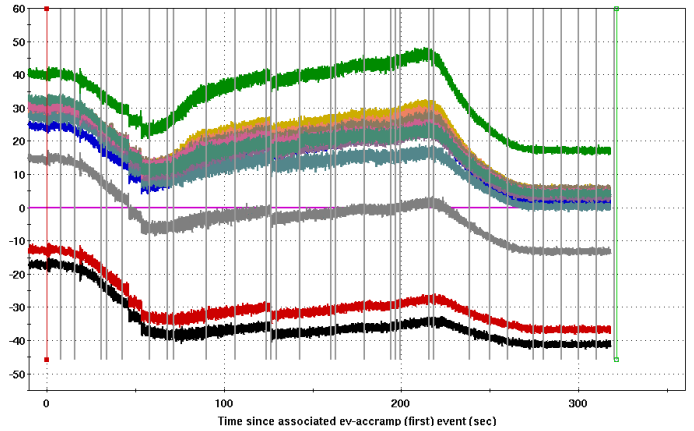
RHIC Bunch by Bunch Dampers

Bunch phases of select bunches along RHIC energy ramp.

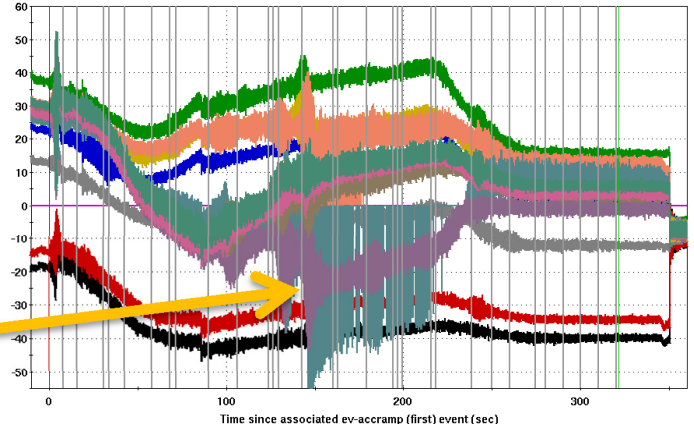


With damper, bunches are stable and growth is minimized (IBS still induces growth).

Damper On



Damper Off



Without damper, bunches become unstable and grow severely.

Reference [K. Smith et al]

Algorithms, Tools, Features

Cavity Control Algorithms

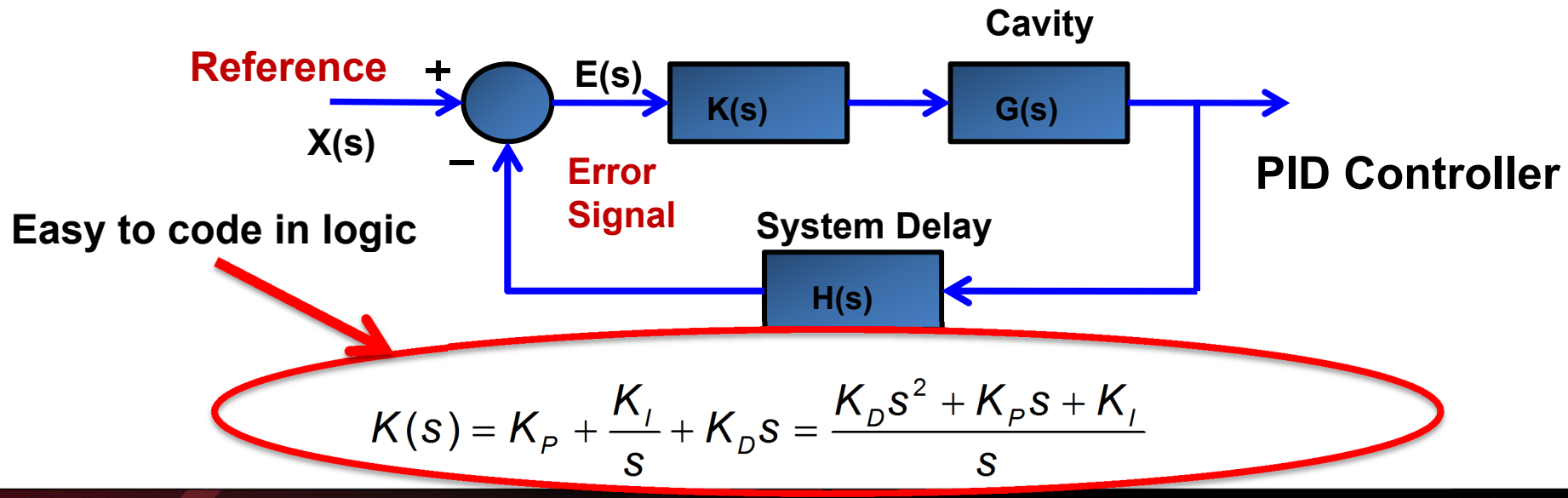
Generator Driven Resonator (GDR)

- Vector Sum (Flash ….ILC)
- Feed forward (for pulsed systems)
- Adaptive Controls

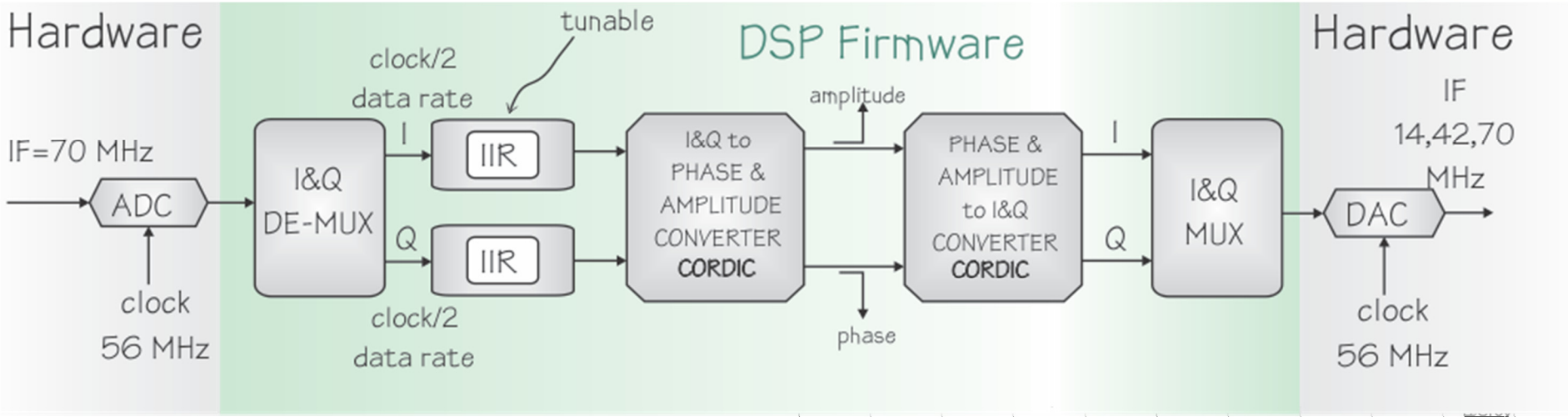
Self Excited Loop (SEL)

Control Algorithms

- Proportional-Integral-Derivative (PID)
- Active Disturbance Rejection Control (ADRC)
- Kalman Filter
- Adaptive Control (LMS)



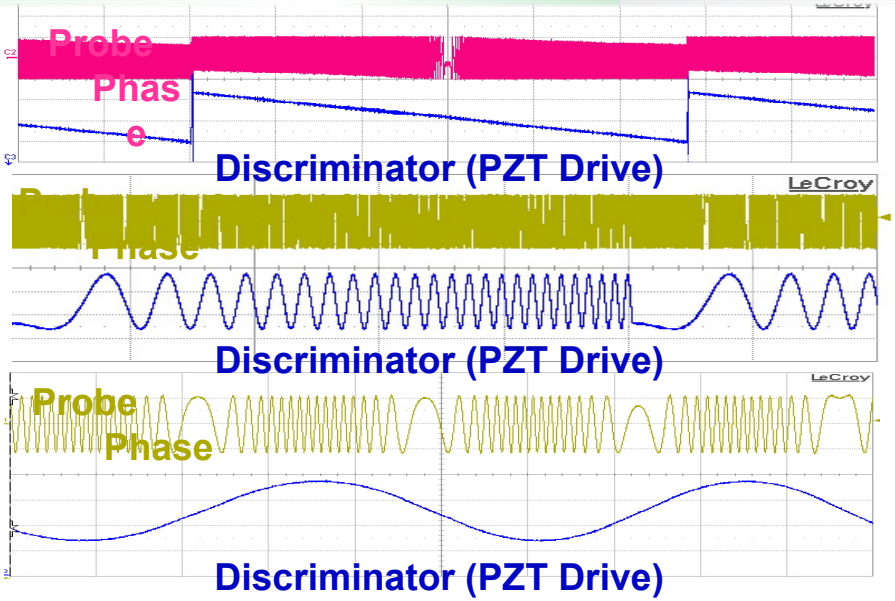
Algorithms: Digital Self Excited Loop



DSP Fall Out: Frequency Discriminator

Four frequency ranges

1-125 Hz (PZT)
125 Hz- 1250 Hz (stepper, PZT)
1250 Hz- 50 kHz (stepper)
50 kHz- 500 kHz (stepper)

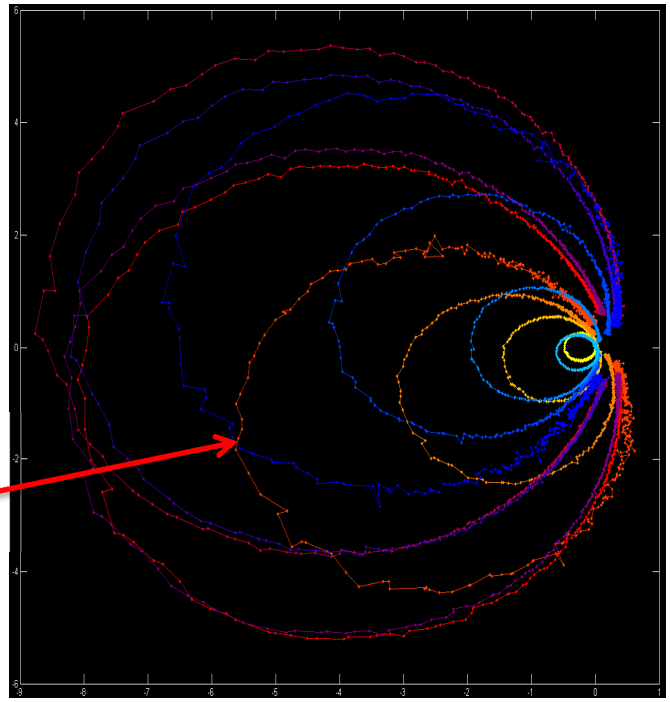


Reference [T. Allison, T. Plawski]

Cool Tools

Along with better operational performance the digital LLRF systems give the operators and system experts an information bonanza.

- **Real time measurements of cavity**
  - **QL,**
  - **Qo,**
  - **Cavity detuning and microphonics**
  - **Waveforms of cavity faults**
  - **As vector network analyzer**



Transfer function: Polar plot Raw Data. J.C. Molendijk - LLRF11

Cool Tools ….Fault Analysis

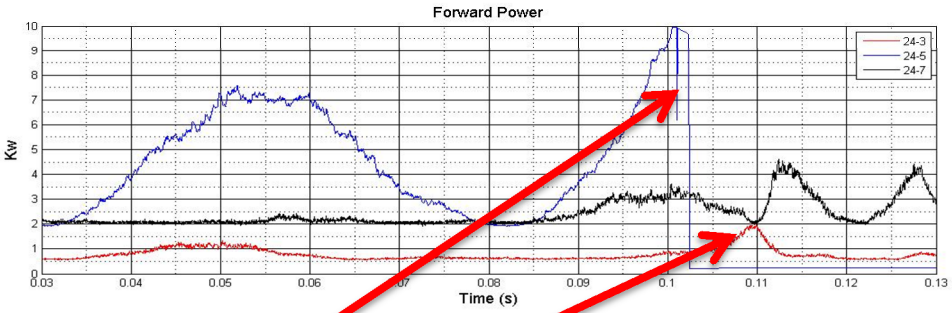
In the past engineers would have to set up O'scope's and analyzers to catch faults.

Now the digital system can be coded such that it can capture and display fault data.

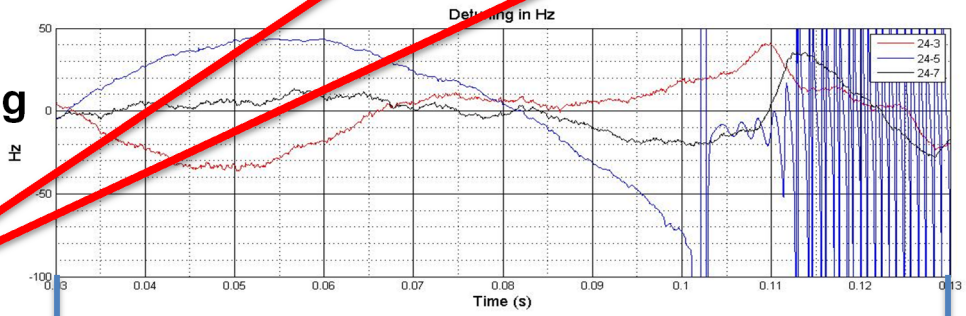
CEBAF 100 MV Cryomodule cavities reacting to adjacent cavity 5 as it faults and turns off

Data collected using ring buffers in the digital LLRF system and displayed In EPICs.

Forward Power



Detuning Hz

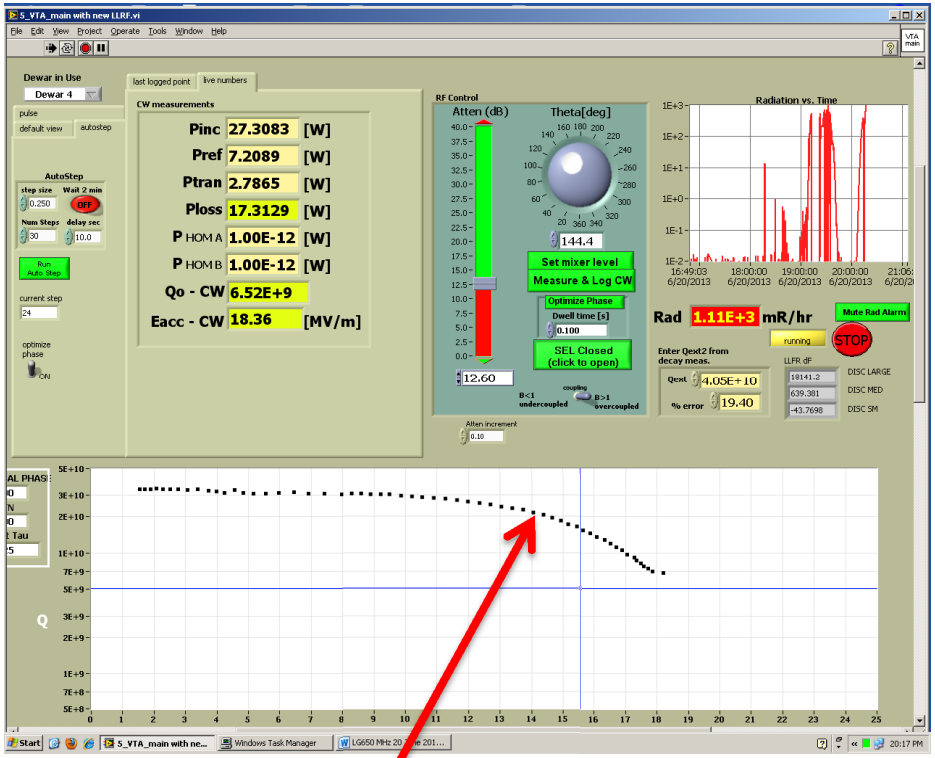


0.1 sec

Cavity 3 10 MV/m
Cavity 5 16 MV/m
Cavity 7 18 MV/m
Cavity 1, 2, 4, 6, and were not powered

Automated Cavity Testing

- **Many labs are taking advantage of the ability to eliminate test equipment by incorporating the functionality into the digital RF controls**
  - **Cavity Qo Measurements**
  - **Cavity power coupler QL**
  - **Cavity transfer function and transmitted power (Gradient calibration)**

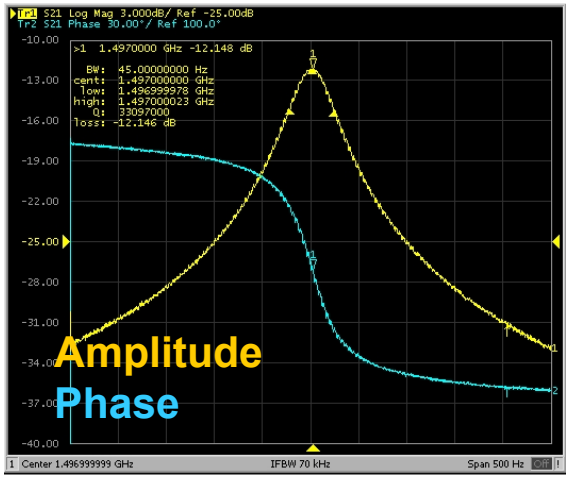


Q_o vs E curve in the JLAB Vertical Test Area. Test was completed using a digital LLRF controller operating in SEL mode. Interface Is Labview.

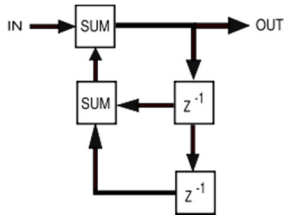
Reference: T. Powers

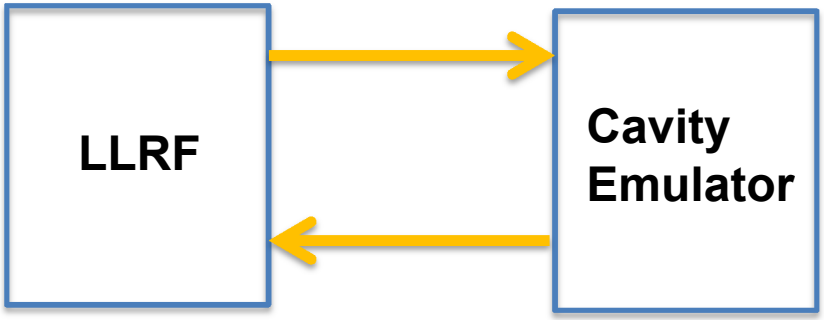
Cavity Emulators

- In the past it has been difficult to test LLRF systems with out an actual cavity.
- High Q crystal filters have been used with varying degrees of success.
- With the advent of digital technology designers have discovered that they can program a cavity emulator into logic that can give a good representation of a cavity.
  - Microphonics
  - Lorentz detuning
  - Beam loading
  - CW and pulsed



Cavity Emulator using IIR Filter





Final Thoughts

- RF control is still evolving as the IC's continue to get larger and faster ….. the analog function is becoming smaller and smaller
- RF/Analog is still needed for system design

Thanks for your Attention

Special Thanks to
Brian Chase, Larry Doolittle, Kevin Smith, Hengjie Ma, Nathan Usher, Tomasz Plawski, Trent Allison, Rama Bachimanchi, Philip Varghese, Mark Crofford, Stefan Simrock

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