A STRIPLINE KICKER DRIVER FOR THE NEXT GENERATION LIGHT SOURCE*

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Abstract

Diversified Technologies, Inc. (DTI) has designed and prototyped a novel high voltage pulse generator applicable to beam deflector applications. This work is funded by an SBIR grant from the U.S. Department of Energy in support of advanced accelerator development. The technical goals include 10 kV output into 50 Ω with 2 ns rise time and a repetition rate of 100 kHz. These challenging specifications were based on the original Next Generation Light Source (NGLS) fast deflectors (stripline kicker) required in the proposed beam switchyard. DTI believes the advanced pulse generator will have numerous applications requiring fast risetime and high repetition rate. This paper describes the current status of the project.

BACKGROUND

In Phase I of the project, DTI investigated several high-speed switching circuits, using a variety of emerging solid-state switch technologies, including GaN and SiC. After much experimentation, DTI has settled on an inductive adder circuit topology, using a two-step, silicon MOSFET Marx approach in each stage. The use of parallel FETs at each stage of the inductive adder allows a flexible design which can be adapted to new requirements. The Phase II prototyping efforts have validated the design approach. Figure 1 shows an operational prototype pulse generator.

Motivation

The NGLS facility concept uses a high bunch rate accelerator (1 MHz) to efficiently supply beam to 10 independent X-ray FEL beam lines. Each beam line receives pulses at 100 kHz, though the fields in the deflector must settle in less than 1 μs to avoid perturbation of un-deflected pulses in the bunch train from the accelerator.

It is envisioned that the deflection will be imparted by a symmetric pair of shaped parallel deflection electrodes, pulsed in opposition at 10 kV. Matching 50 Ω resistors terminate the deflector to avoid the creation of backward-traveling waves.

SYSTEM ARCHITECTURES

Various system designs were explored for producing the required pulse wave forms. The options included a direct series high voltage switch, solid-state Marx bank, inductive adder, or more conventional pulse transformers and transmission-line adders, several of which were considered in detail. The inductive adder was ultimately selected as the preferred development path for the remainder of the program. The favored embodiment of the overall pulse generator was based on measurements, multiple circuit test boards, extensive modeling, and practical considerations regarding component performance in the sub-nanosecond regime.

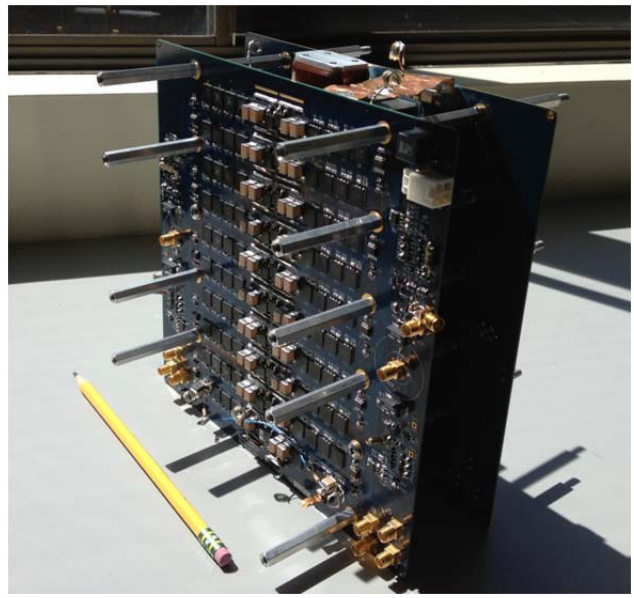

Figure 1: Prototype pulser hardware. In the center of the rectangle at the top is the output connection, and the two circuit boards on either side carry the pulse amplifiers and MOSFETs.

Pulse Generation

The overall pulse generation network is presented in Figure 2. This represents the principal schema, but variants on this approach have been developed as well. The key components exhibited in this figure include:

- Each stage is comprised of a pair of STMicroelectronics STL21N650 compensated silicon MOSFETs, capable of 2 nanosecond-class switching speed, along with extremely fast charge-pump driver circuitry to enable such fast switching. Note that the gate drivers must be referenced to the source pins in the diagram, meaning that one set of gate drivers must be floating – a key technological issue in this speed domain.
- A set of transformer cores, Tn, to couple the 1 kV pulses into a common tapered secondary structure. Matching the impedance of the output structure to

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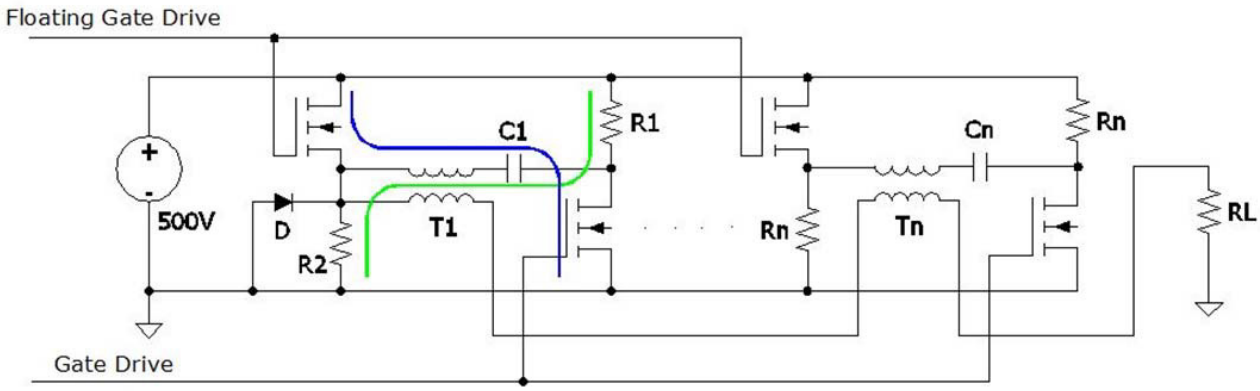

Figure 2: Basic inductive adder scheme, showing "n" stages. Note that the gate drives are shown all in parallel. This is due to DTI's innovative gate driver architecture which enables high voltage charge pump circuitry to drive multiple compensated-silicon MOSFETs with the speed required to achieve nanosecond-class switching. In this Marx arrangement, C1 is charged through resistors R1 and R2 (GREEN). The MOSFETs then discharge the capacitors through the transformers T1 through Tn, applying two times the charge voltage, or 1kV in the arrangement shown (BLUE). The secondaries of the transformers are a tapered stripline to match the output impedance of each stage to the load impedance RL. Diode D enables sharp turnoff to meet the stringent turnoff specification.

each stage's output impedance in a tapered fashion enables the fast leading edge required by the application.

Not shown is the gate driver circuitry or the circuit board itself. The pulse amplifier developed for driving the STL21N650 transistors was designed with minimum group delay and maximum gain to effectively utilize charge-pump drive techniques. This charge-pump design has been successful in prior work at DTI, and is ideally suited to this application. The circuit board itself is highly tuned for this pulse application—extreme care has been taken to achieve very low trace inductances. Plane-to-plane spacing was kept to 0.003 inch in order to achieve power traces under 300 pH. This was critical in order to switch 500 V and 50 A per transistor in roughly 3 nanoseconds. The small, low inductance parts allow for the fast switching speeds. This board technology was crucial and left the intrinsic inductance of the packaged parts as a limit to the achieved rise times.

In order to keep the overall size and parts count down, a 10-stage 1 kV-per-step approach was chosen. The Marx topology at each stage allows 1 kV to be applied to the transformer cores while still using the fast 650 V transistors. Four MOSFETs are used in parallel at each position to carry the current and keep the inductance down. Measured inductance of each stage comes to less than 8 nH, dominated by the leakage of the coupling transformer. Capacitors Cn are chosen to have low inductance and acceptable voltage ripple and recharge time. The pulse amplifiers used to drive the transistor gates are tailored specifically to pump the appropriate amount of charge required to turn the devices on, while still having a propagation delay in the 8 ns range and being driven by TTL signals. The amplifiers consist of four stages; first a FET stage for level shifting and inversion, then bipolar followers, and finally FET inverters backed by followers. Each was chosen specifically to utilize their respective strengths (FETs for fast turn on, bipolars for current, etc.). Additionally, the gate pulse amplifiers for the floating side of the Marx are floating, referenced to the source of those power FETs only. Blocking cores are used to stand off the pulsing and float the stages at AC, but still provide a DC charging path to ground.

In the absence of diode D in the circuit above, the core reset of T1 through Tn happens through recharging of the capacitors in the Marx stages. However, this process is lengthy and somewhat chaotic, so diode D shuts off the secondary current flow due to recharge, effectively damping the ringing at turnoff and removing any stray pulses allowing the output to settle to better than 1 V in less than 1 μs.

Current Results

An example waveform is shown in Figure 3. The purple trace shows the command pulse, the green shows a capacitively-coupled probe with an arbitrary scale, and the red trace shows the voltage into 50 Ω on a 2 kV/division scale. Note the turn-on of 10 ns, the turnoff of 10 ns and the flattop of 30 ns. The peak is 8 kV at 160 A, the power is 1.28 MW. At this power level, the system was run at 1 kHz repetition rate on the bench with anything but a fan for cooling of the FETs. The peak temperature of the FETs was 65 C. With more aggressive cooling, operation at 10 kHz repetition rate should be possible.

Figure 4 shows operation at 10 kV, 200 A into 50 Ω; a full 2 MW per pulse. The red trace is the command pulse and the gray trace is the output pulse at 2 kV/division. Note the 7 ns rise and 8 ns fall times with 20 ns flattop.

Current pulser hardware is capable of pulses as long as 70 ns without any additional electronics for core reset. Additional core reset circuitry has been explored, but is not necessary at this time to meet the requirements of the

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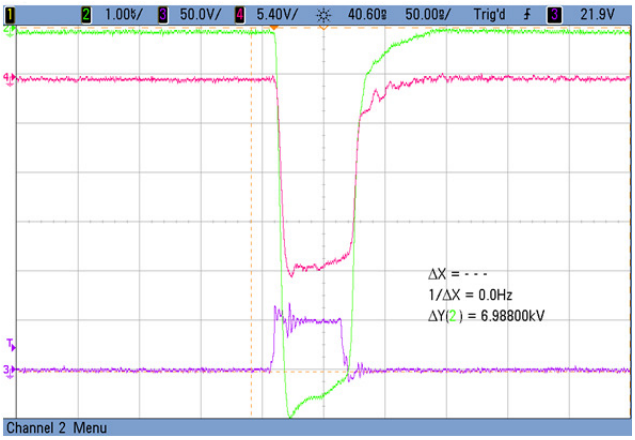

Figure 3: Performance at 8 kV into 50 ohms. Red trace is 2 kV/division. Note the 10 ns rise and 10 ns fall.

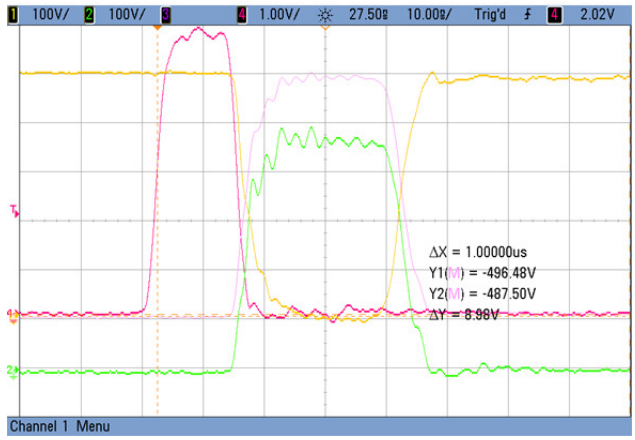

Figure 4: Operation at 10kV into 50 ohms. The faint gray trace is 2kV/division. At this higher power level, the transistors operate a touch faster, and the rise and fall times consequently are faster than at the 8 kV case.

NGLS kicker. Exploration of the current hardware limitations is underway, and it is likely that much higher currents are possible. The 200 A at 10 kV result was achieved with only 3 transistors at each location, and with the possibility of 4 transistors on the PCB. Perhaps 10 kV at 250 A may be in the future.

FUTURE PLANS

DTI is in the process of adapting this circuit architecture for other applications, including pulsed RF sources, pulsed plasma surface treatment systems and others. The remaining questions surround the maximum pulse rate and delivered power levels. Additionally, given the small size of the 2 MW pulser hardware, high voltage insulation and cooling are challenging. DTI will initially investigate immersion in oil bath, and later in phase-change cooling with refrigerants.

The current work is based on the C6 generation MOSFETs from STMicroelectronics. STMicroelectronics is currently shipping higher performance C7 generation devices, which will translate into faster pulses with more current capacity per device, or perhaps higher pulse repetition rates at the existing power levels. As these devices are available, we will be examining their performance in the current hardware.

Additionally, there are larger devices that are capable of as much as 125 A per device in single-state tests. This could project to a peak pulse of nearly 500 A at 10 kV, and testing is ongoing to explore the full performance envelope of the current architecture.

SUMMARY

The DTI team has designed and demonstrated the key elements of a solid-state kicker driver capable of meeting the NGLS requirements, and extension to a wide range of kicker driver applications. The MOSFET array switch itself is suitable for many accelerator systems with < 10 ns kicker requirements.

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