FAST ORBIT FEEDBACK SYSTEM FOR THE LNLS STORAGE RING

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Abstract

The Brazilian Synchrotron Light Laboratory (LNLS) is based on a 1.37 GeV storage ring, currently operated by means of a Slow Orbit Feedback system at a maximum rate of 1 correction every 3 seconds. Since photon beam stability is a key issue for light source users, a faster orbit control system was envisaged to provide better beam stability. This work presents an overview of the hardware architecture and the preliminary results achieved with the implementation of a Fast Orbit Feedback (FOFB) system using commercial hardware. BPM signals are acquired in a distributed topology and sent through a deterministic EtherCAT network to a PXI controller, responsible for applying the SVD-based correction matrix multiplication and communicating with the accelerator control system; the calculated current setpoints are sent to the correctors' power supplies (PSs) through a second EtherCAT network. FPGA-based acquisition and actuation chassis perform pre-filtering and PID control on the digitized input and output signals, respectively.

INTRODUCTION

Beam stability is a key issue in synchrotron light sources. At the LNLS storage ring, orbit correction is limited up to a rate of 0.3 Hz and provides an orbit stability along a user's shift of ±5 μm, which has been suitable to meet user needs since 1997 [1]. Several improvements have been done along the years in order to increase the beam stability, mainly focused in the mitigation of very low frequency perturbation related to thermal issues [2]. However, the development of Sirius, a 3rd generation 3.0 GeV low emittance synchrotron light source, and the increasing user demands for photon flux stability, encouraged the upgrade of the LNLS orbit feedback system. This will improve beam stability and provide an excellent way to test orbit correction strategies for Sirius, besides allowing the fast acquisition of BPM signals and its frequency domain analysis.

Due to the long development time and the high costs inherent to proprietary feedback systems, it was decided to use multipurpose commercial devices. This approach skips the hardware development phase.

SYSTEM TOPOLOGY

The LNLS storage ring has 25 beam position monitors distributed along its six superperiods (the injection straight section counts on 3 BPMs), and 24 vertical and 18 horizontal steering magnets. Bergoz MX-BPM boards are used for processing the BPM signals and providing analog position signals ranging from -10 to +10 Volts.

The FOFB system is subdivided in acquisition chassis, a central controller and actuation chassis. The central controller manages two network loops, one for acquisition and another for actuation. Data transfer over these two loops is done using the EtherCAT protocol (Ethernet for Control Automation Technology), which guarantees the synchronism of all devices connected to the network. This feature provided by EtherCAT protocols is essential to attend sampling simultaneity required for feedback systems.

In the acquisition chassis, BPM analog signals are acquired through 4-channel 16-bit AD converters with isolated inputs (model NI 9215), distributed in six FPGA-based acquisitions chassis (model 9144) connected at the same EtherCAT network. The acquisitions are performed at a 100 kS/s rate and are responsible for oversampling and pre-filtering the incoming beam position signals. The AD boards and the Bergoz electronics are connected by individually shielded pairs of cables distributed along the storage ring circumference (Helukabel, PA.TR. CY-CY type). The cables length is about 6 meters.

The central processing is performed by a PXI 2.53 GHz Intel Core 2 Duo T9400 controller running the Phar Lap ETS real-time Operational System, important to assure the determinism of the software routines. The controller receives the filtered data and calculates the current setpoints, which are sent through a second EtherCAT network that connects six actuation chassis equipped with digital I/O, DA and AD converters (modules NI 9401, 9215 and 9263) for commanding and adjusting the PSs.

The system topology is illustrated in Fig. 1.

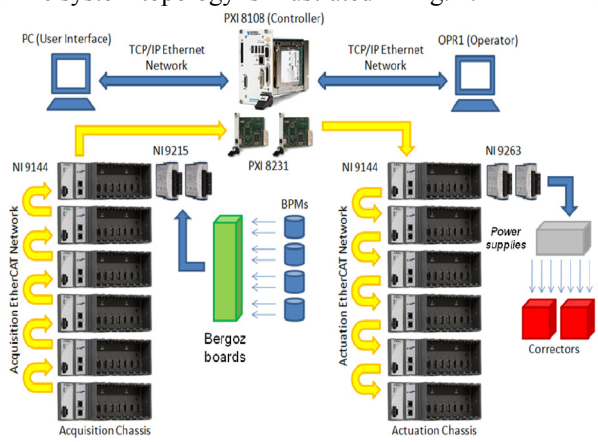

Figure 1: Feedback system topology. OPR1 is the name of the central PC that centralizes the accelerator control.

SOFTWARE SETUP

The correction algorithm was implemented in the LabVIEW environment. It is described in the following subsections.

FPGA Acquisition Firmware

The FPGA Acquisition Chassis contain two loops running in parallel, with the first performing

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oversampling at 100 kS/s of the digitized beam position data, applying a 2-order Butterworth filter (1 kHz cutoff frequency) and writing the fixed-point values in registers (local variables). The second loop is synchronized with the Scan Engine, a native LabVIEW software component used to improve the access to sets of data channels that scans and stores data in a global memory map, updating all values at a single rate [3]. This loop transfers the values from the local variables to the central PXI controller through the EtherCAT acquisition network.

The position signals are limited in frequency by 2nd order active filters on Bergoz boards, but the pre filtering is necessary to decrease spurious components multiple of 1/4th of the clock signal present in the signal with relatively high amplitude even after the onboard filtering. The clock leakage is always above 2 kHz and is inherent from the analog multiplexing scheme adopted in the MX-BPM boards and, due to that, small aliased components can appear in the passband of the system after the decimation realized between the acquisition chassis and the PXI controller.

PXI Controller Software

This controller software contains the control loop responsible for calculating the correction vector to be sent to the PSs. It also writes data information in the PXI controller hard disk (accessible through the TCP/IP Ethernet network), exchanges information and commands with the accelerator control system and applies the configuration setups defined by the user.

FPGA Actuation Firmware

The FPGA Actuation Chassis also contain two parallel loops: one is synchronized with the Scan Engine [3], and responsible for writing the PS setpoint values and on/off commands to the DAC and digital output cards (NI 9263 and NI 9401) as well as reading the PS on/off status from the digital inputs of the NI 9401 modules; the second loop is in charge of oversampling the PS current return at 100 kS/s and filtering it with a second order filter with 500 Hz cutoff.

SYSTEM INFRASTRUCTURE

In the acquisition network, the six chassis responsible for processing and transmitting the BPM data to the PXI controller were allocated in individual electrical boxes, located adjacent to the concrete shield in the inner region of the storage ring tunnel.

The actuation chassis were allocated in 3U 19" rack mount cases, in order to be placed in the PS racks. Standard, shielded and not-twisted DB-25 cables connect the actuation chassis to the PSs. The DA converters are channel-to-ground isolated. This is not the optimum configuration, but the PSs will be upgraded to models with isolated inputs. Figure 2 shows an actuation chassis.

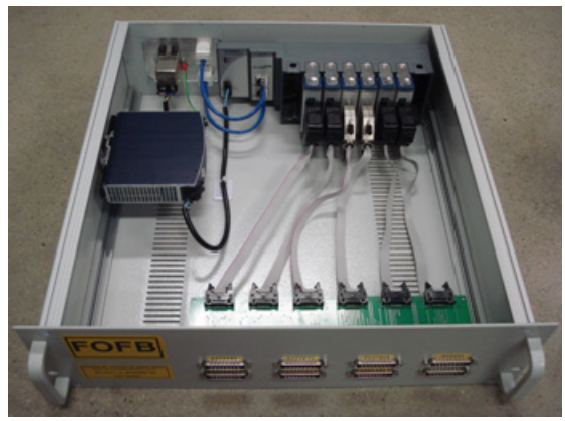

Figure 2: Actuation chassis. The PCB board organizes and groups the signals coming/going from/to different PSs in order to connect them in different modules.

RESULTS

Bench Tests

To assure the simultaneity of BPM samples, a proof of concept was carried out with 1/6 of the final system. An experimental setup was prepared in order to determine the simultaneity of samples acquired from different channels from distinct chassis (connected through the same EtherCAT network), using a signal generator and an oscilloscope. The delay was calculated applying FFT on the two acquired samples and determining the difference of phase at the frequency of the 1st harmonic. The delay variation is measurable, it was determined as being 750 ns. Since the feedback loop is supposed to have a minimum 100 µs period (10 kHz), the delay between samples (< 1 µs) can be neglected and the acquisition process can be considered simultaneous for the FOFB purposes.

Besides time synchronization, the maximum feedback loop rate and the real-time execution capabilities were determined. The experimental setup also relied on 1/6 of the total system and with a signal generator providing the simulated position signal and an oscilloscope reading the DAC outputs. The variables were read and written several times similarly in the synchronization test. In addition, a matrix multiplication was computed by the controller to simulate the orbit correction. In order to avoid extra computation time, the matrix calculation was performed using a custom implementation based on a for loop, with simple multiplication and sum functions, faster than the LabVIEW's native matrix multiplication function, which is based on a DLL call.

The limit for proper operation was found to be about 7 kHz. Above that rate, erroneous values were written in the DAC. Figure 3 shows the system running properly at 6 kHz.

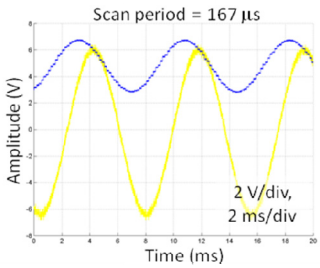

Figure 3: Maximum feedback loop rate determination. The waves represent one input and one output of the FOFB system. The delay between curves is due to the matrix multiplication. The DAC output is the upper trace.

Tests with Beam

The system was tested with real beam after installation in the storage ring. The final software added several features which improved reliability and configurability but reduced the maximum acquisition rate to 3 kS/s when only reading BPM data and to 2 kS/s for close-loop operation.

Fast acquisitions were performed in several situations: energy ramps, injection and during response matrix measurement. For the last, it could be observed the transient response of the corrector PS for a step change in the current setpoint. Figure 4 shows an example of fast acquisition at 3 kS/s.

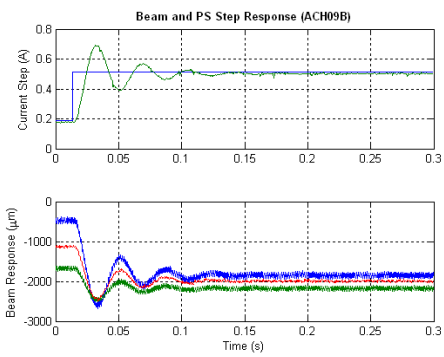

Figure 4: Step response of a PS during a response matrix measurement (above). Beam response at 3 BPMs (below).

These tests revealed that many corrector PSs exhibit very slow and poorly tuned time responses. An upgrade program for the corrector PSs is currently in progress and it is foreseen to have all the storage ring units replaced until the end of this year.

The tests in closed-loop were successfully performed. They attested that the whole implementation, hardware and software, were working properly. Notwithstanding, the maximum update rate which could be reached was 10 corrections per second (100 ms correction period) due to the asynchronies among the PSs behavior. The beam was lost when higher update rates were tried.

FUTURE STEPS

Currently the BPM signals are acquired at a 100 kS/s rate, filtered in 1 kHz bandwidth and decimated to 2 or 3 kS/s. The low-pass filter order is limited by the available space in the FPGA chassis. Methods for increasing the digital filter rejection and tests with different bandwidths can improve the final signal to noise ratio of the BPM signals.

New corrector PSs (under development by the LNLS Power Electronics group) are expected to be installed until the end of 2011, allowing the system to operate at faster correction rates. The characterization of these PSs will provide useful information for the best choice of the PID parameters, further improving electron beam stability.

Fast acquisition data obtained from the beam position monitors is a powerful tool to detect perturbations at the frequency domain. Toll for performing fast analysis in the frequency domain will be developed, as well as routines to automatically identify faulty PSs or BPMs.

Certainly the more important task, the performance optimization of the system, after the PSs upgrade, can provide insights for the feedback system of Sirius, including the development of efficient control algorithms that take in account the dynamics and limitations of the PSs [4].

CONCLUSIONS

The FOFB system is currently being commissioned, and several tests concerning data acquisition, system integration and orbit correction were performed successfully.

Software developments in LabVIEW proved to be simple and relatively not time-consuming. The major software tasks (fast orbit feedback loop, feedback configuration and process variables monitoring) as well as FPGA pre- and post-processing (oversampling and filtered acquisition for inputs and PID control for outputs) were quickly implemented with a robust architecture. The simultaneity of acquisitions, within 1 µs between adjacent EtherCAT slaves, is perfectly acceptable for the fast orbit feedback application.

The guaranteed loop rate of 5 kHz, although not ideal, is still acceptable for the LNLS FOFB system. Moreover, the achieved update rate is not so far from the state-of-the art of similar systems operating around the world.

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