SLAC P2 MARX CONTROL SYSTEM AND REGULATION SCHEME

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Abstract

The SLAC P2 MARX Modulator consists of 32 cells charged in parallel by a -4 kV supply and discharged in series to provide a -120 kV 140 amp 1.7 millisecond pulse. Each cell has a 350 uF main storage capacitor. The voltage on the capacitor will droop approximately 640 volts during each pulse. Each cell will have a boost supply that can add up to 700 V to the cell output. This allows the output voltage of the cell to remain constant within 0.1% during the pulse. The modulator output voltage control is determined by the -4 kV charging voltage. A voltage divider will measure the modulator voltage on each pulse. The charging voltage will be adjusted by the data from previous pulses to provide the desired output. The boost supply in each cell consists of a 700 V buck regulator in series with the main capacitor. The supply uses a lookup table for PWM control. The lookup table is calculated from previous pulse data to provide a constant cell output. The paper will describe the modulator and cell regulation used by the MARX modulator. Measured data from a single cell and three cell string will be included.

INTRODUCTION

The P2 Marx Modulator, as discussed earlier in [1],[2], uses two different regulation systems to achieve an output that remains within 0.1% of the desired value during the 1.7 millisecond pulse.

The initial output voltage of a pulse will be the sum of the voltages on the 32 main storage capacitors. These capacitors are charged in parallel by a -4 kV 150 KW capacitor charging power supply. The modulator output voltage will be digitized and used to adjust the voltage of the 4 kV supply for the next pulse. Since each storage capacitor will nominally droop 680 volts during a pulse, each cell contains a boost supply that can add up to 700 volts to the cell output. The correction supply relies on a 875 uF capacitor. A -1 kV 30 KW capacitor charging power supply is used to charge these 32 capacitors in parallel to a nominal -1050 volts. A buck regulator is used to convert to a 0 to -700 volt output. The voltage is regulated by the duty cycle of the PWM to maintain the cell output voltage constant during the pulse.

The 4 kV supply determines the modulator output voltage. Any deviation in the measured output from the desired voltage will be used to adjust the 4 kV supply for the next pulse. The correction supply is zero at the beginning of each pulse, and initially makes no contribution. Its function is to maintain the cell output voltage constant during the pulse. Any droop in the cell output during a pulse will be compensated in successive pulses by adjustments to the cell PWM look-up tables.

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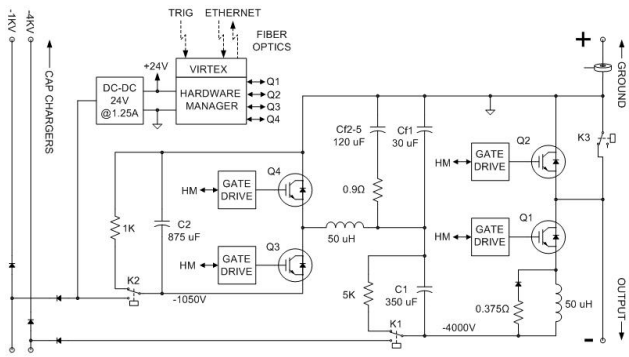

Figure 1: Simplified cell schematic.

CONTROL SYSTEM

The modulator does not use feedback to adjust the output during a pulse. The 4 kV supply voltage and correction PWM are set prior to the start of the pulse based on initial values from simulations and modified by data from previous pulses. All of regulation functions are performed by a single computer, known as the application manager[3]. In a production system, this would be an Experimental Physics and Industrial Control System (EPICS) Input/Ouput Controller (IOC). During hardware development, Windows based PCs are being used to run programs written in Visual Basic. The application manager communicates with the 32 cells using gigabit Ethernet over optical fiber. This provides high speed communications and high voltage isolation.

All messages are command/response using UDP datagrams. This allows any computer with an Ethernet port and TCP/IP to serve as the application manager.

VIRTEX BOARD

The control system is built around gigabit Ethernet and a standard interface board. The board provides communications, control, timing, protection, and data acquisition for each cell and peripheral. This board has a Xilinx FPGA (Virtex XC5VLX30T) that provides an Ethernet MAC for communications, an SFP module for fiber or copper connection, and 2 Mb of RAM for data storage. There are 96 general purpose I/O lines that can be programmed to control ADCs, DACs, relays, etc. The boards are programmed to be distributed I/O and data acquisition under control of the application manager.

Even though the Virtex has immense processing capability, cell regulation is handled by the application manager. This centralizes the complex code in one location written in a high level language rather than

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distributed code in VHDL. This approach simplifies the development process. After the regulation algorithms become fully developed, they can be migrated into the Virtex in order to reduce the application manager's processing between cycles.

The modulator does not rely on Ethernet communication for any critical safety or protection circuits. The Virtex in each cell is programmed to inhibit or abort pulses if any abnormal events are detected. The design goal is to have the individual cells be self protecting. The cells must also respond to loss of Ethernet communications in a manner insures safety and protects the hardware.

The latency of the Ethernet is assumed to be tens or hundreds of microseconds. To insure that the cells are synchronized to less than a microsecond, each cell has a dedicated fiber optic trigger. All timing during the pulse is handled by the Virtex. No Ethernet traffic is required during a normal pulse, so fault messages can be broadcast with a latency of several microseconds.

The Ethernet interface uses local Ethernet and IP addresses that are not unique. This requires a dedicated local network without direct access to any other network. The lower 8 bits of the Ethernet and IP address are set by switches on the board. The upper 40 bits of the Ethernet address, and upper 24 bits of the IP address, are fixed. The board will respond to address resolution protocol (ARP) requests to allow any computer with Ethernet and TCP/IP to communicate.

TRIGGER CONTROL BOARD

The modulator will have a board using a Virtex module to distribute fiber optic trigger signals to the 32 cells. The board will have ADCs to read the modulator output voltage and current. The Virtex will save blocks of 2048 ADC samples during a pulse for later display as waveforms. This board will also handle all safety and hardware interlocks for the modulator cabinet. It will monitor water, airflow, and critical temperatures. The application manager will be able to read all status over Ethernet. The board will have a hardwired connection to allow inhibiting the 4 kV and 1 kV power supplies for safety or equipment protection. It will remove triggers if a klystron arc or over current is detected. It will generate inhibit signals for the 4 kV and 1 kV supplies during pulses.

4 KV AND 1 KV SUPPLY CONTROL

The 4 kV supply will be controlled by a board using the Virtex module. This allows the power supplies to be located away from the modulator and be controlled by the application manager using Ethernet. Safety interlocks and pulse inhibit signals are hard wired from the modulator. The board will have ADCs to read the outputs of both power supplies, and record 2048 sample waveforms. The board will have DACs to set the output voltage and current of the power supplies. The application manager will adjust the 4 kV output voltage to maintain the modulator output voltage at the desired level. The 1 kV supply will have a fixed setting of -1050 volts. This supply not only powers the correction PWM, but is used to provide 24VDC control power in each cell. Therefore this supply must be on before there is any control or communication with the 32 cells.

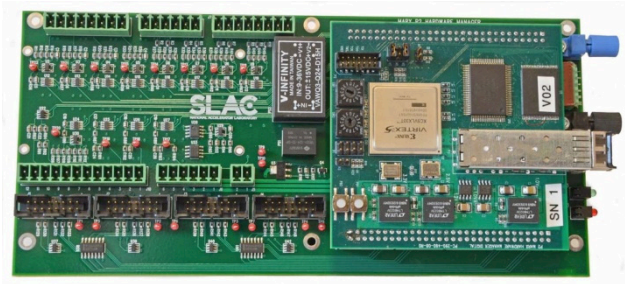

Figure 2: Hardware manager with Virtex board.

HARDWARE MANAGER

Each cell has a control board called a Hardware Manager. It uses 24VDC from a converter that uses the 1 kV for the correction supply. The board has twelve 12 bit serial ADCs that monitor cell operation. Eight of the ADCs capture 2048 sample records during each pulse. The data is read by the application manager after the pulse. Due to the large amount of data involved with 32 cells, it will only be downloaded when a cell fault occurs, or periodically for regulation and diagnostics. The hardware manager receives a trigger from the trigger board to start a pulse. The pulse will continue until the trigger is removed or maximum pulse time is reached. The cell then enters a 800 microsecond energy recovery period where the energy in the correction supply output capacitors is returned to the correction storage capacitor.

The Virtex has programmable delays for the start of the pulse, and the start of the correction supply. Each of the 32 cells will have a different delay to control the rise time of the modulator output. The delays for the correction supplies will be used to phase shift the ripple voltage from each cell for maximum overall cancelation. The Virtex board generates PWM signals for the correction supply. The PWM has a 25.6 microsecond period comprised of eight hundred 32 ns ticks. The duty cycle is set by a 72 entry lookup table in the Virtex. The table is configured by the application manager using simulation data modified by data from previous cycles. The ADCs take 25 readings every PWM cycle. The ADCs are synchronized to the PWM to provide fixed sample times on each cycle. Averaging 25 samples will provide the DC level with no effects from the output ripple.

The application manager uses a calculated unit impulse waveform for a single 32 ns PWM tick to calculate the changes to the table. The PWM pulse is centered in the cycle and grows symmetrically from the center. For each 1 tick increase, the PWM is turned on 16 ns sooner and left on 16 ns longer. This provides a constant ripple phase and unit impulse response over the full duty cycle range.

The application manager will periodically read the ADC that measures the sum of the main storage capacitor and the correction supply. The goal of the cell regulation

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is to maintain the value just prior to the start of a pulse constant over the length of the pulse. If the value varies more than 0.1% over the pulse, the application manager will adjust the PWM table to reduce the error. The PWM correction is made sequentially from the first PWM period to the last. The duty is modified from to compensate for the error signal two PWM cycles downstream. Due to the delay in the PWM filter, the second term of the impulse response is four times greater then the first term. The effect of the PWM change is subtracted from downstream data using the calculated unit impulse multiplied by the number of PWM ticks changed.

MEASURED RESULTS

To aid software development, a test fixture was built that mimics cell operation. The output is 48 V at 1 A with all time constants and readbacks scaled to behave like the full power cell. Figures 3 and 4 show the Visual Basic form used to test the cell regulation algorithm. The top plot is the PWM duty cycle table. The bottom plot shows the cell output as read from the ADC, and the average value for each PWM cycle. The rise time is due to the inductance included in each cell. After the rise time, the average voltage remains constant to within 0.1%.

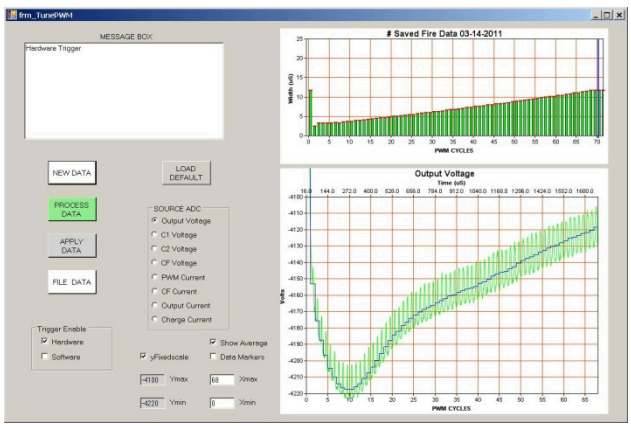

Figure 3: Cell regulation form before correction.

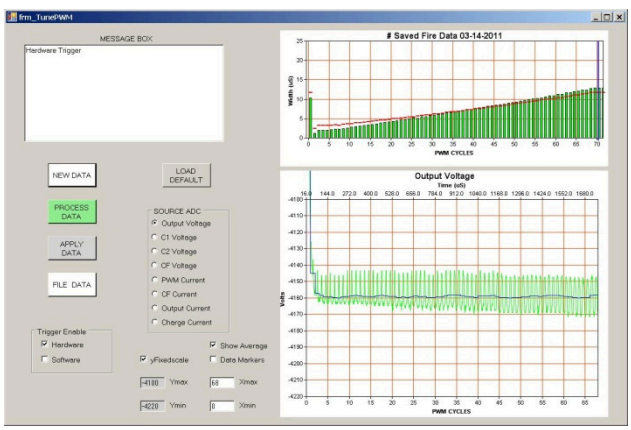

Figure 4: Cell regulation form after correction.

Figure 5 shows the waveforms obtained from a test of three cells in series to produce a -12 kV output. The bottom two traces are the 3 cell output voltage and current. The top two traces are the correction power supply from a single cell. The voltage is read at the input side of the PWM inductor.

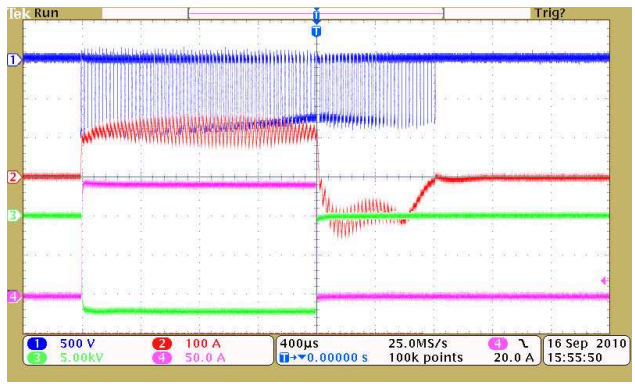

Figure 5: Three cell oscilloscope waveforms.

SUMMARY

This paper presented an overview of the control system for the SLAC P2 Marx. As of the time of this publication, the full modulator is under construction in anticipation of full output testing in the summer of 2011. Mentioned above, the software is still under development with primary efforts towards ensuring a robust and fault-tolerant control system. In addition, there is additional effort required to further optimize the correction algorithm. Finally, potential collective effects of the 32 cells may need to be accounted for in the application manager software.

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