THE LOW-LEVEL RADIO FREQUENCY SYSTEM FOR THE SUPERCONDUCTING CAVITIES OF NATIONAL SYNCHROTRON LIGHT SOURCE II *

Hengjie Ma, James. Rose, B. Holub, J. Cupolo, J. Oliva, R. Sikora, M. Yeddulla
Brookhaven National Laboratory, Upton, NY 11973, U.S.A.

Abstract

A digital low-level radio frequency (LLRF) field controller has been developed for the storage ring of The National Synchrotron Light Source-II (NSLS-II). The primary performance goal for the LLRF is to support the required RF operation of the superconducting cavities with a beam current of 500mA and a 0.14 degree or better RF phase stability. The digital field controller is FPGA-based, in a standard format 19"/1-U chassis. It has an option of high-level control support with MATLAB running on a local host computer through a USB2.0 port. The field controller has been field tested with the high-power superconducting RF (SRF) at Canadian light Source, and successfully stored a high beam current of 250 mA. The test results show that required specifications for the cavity RF field stability are met. This digital field controller is also currently being used as a development platform for other functional modules in the NSLS-II RF systems.

INTRODUCTION

The NSLS II RF system will include four 500 MHz, 2.5 MV/300 kW superconducting cavities, two passive 3rd harmonic superconducting cavities in the Storage Ring (SR), one 1.2 MV/80 kW normal conducting PETRA cavity in the Booster, and up to four 3 GHz travelling-wave accelerating structures in the LINAC. The performance requirement for the SR RF is derived from the beam stability requirement of user experiments. The beam stability requirement translates into a set of general requirements on the RF, among which, the most basic one is the RF phase stability of 0.14 deg, RMS (over 0.5~50 kHz bandwidth) [1], [2]. The planned LLRF sub-system design for each cavity/RF power source has a cavity field controller front-end as its key device for the core functionalities. The planned standard integration method for the LLRF sub-system to the accelerator global controls infrastructure is through a cell-controller (or "concentrator") which serves as an interface to the control network [3]. The developed field controller has a USB2.0 port and a set of common application programming interface (API), including MATLAB which allows the field controller to be hosted and operated with a local PC.

CONTROLLER HARDWARE

The digital hardware of the cavity field controller front-end module is implemented on a high-density FPGA device. The primary reason for choosing an FPGA over an ASIC DSP is that the FPGA implementation allows a concurrent processing of many signals, and thus results in shorter data processing latency. The mechanical format for the field controller is chosen to be a standard 19"-1U chassis for good EMI performance and ample front and rear panel space, while still maintaining the modularity of the LLRF system. Figure 1 shows the hardware construction. To implement the required LLRF functionalities, the necessary analog/digital I/O peripherals are added around the FPGA device in the LLRF controller hardware as shown in Figure 2. These peripherals include

- RF input - 8 channels, 14-bit resolution, simultaneous sampling up to 80 Msps.
- RF output – 2 channels, 14-bit resolution, update rate up to 250 Msps. One channel can be used to output the LLRF controller drive, while the other for generating a test/calibration signal.
- 1.5M gate FPGA (Xilinx Spartan 3 family) with an external memory of 512Mb.
- Trigger I/O, 6 channels
- Low-speed analog I/O, 12-bit, 8 inputs, 4 outputs.
- Dual 100Mbps Ethernet port, planned connection between the LLRF front-end and the cell controller.
- USB2.0 port. A connection to a local host.

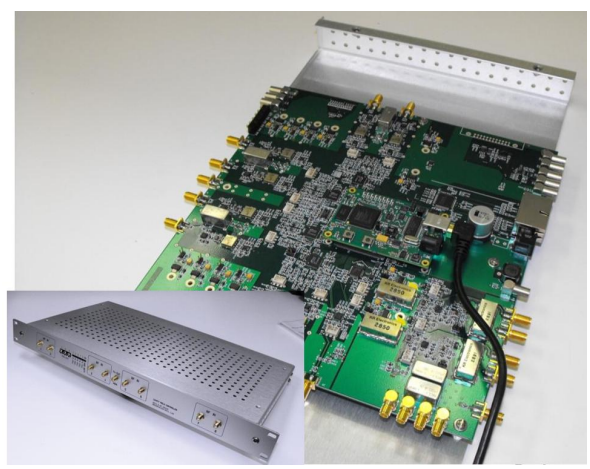

Figure 1. The digital cavity field controller for NSLS-II storage ring is FPGA-based, and packaged in a 19" 1-U chassis.

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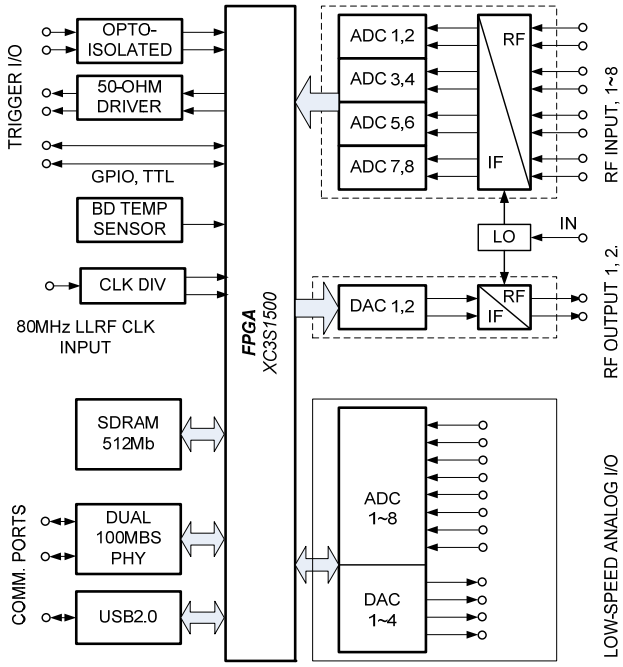

Figure 2. The architecture of NSLS-II LLRF controller hardware. The added peripherals around the FPGA device provide the necessary signal I/Os, as well as the communication ports.

HIGH/LOW-LEVEL CONTROLS

The primary functionality of the cavity field controller implemented in the FPGA is a cavity impedance modifying "wideband feedback control loop". It includes the input signal filtering, vector signal detection (such as "I/Q"), loop phase correction, the low-latency P-I feedback control, and the digital synthesis of output drive signal [4], [5]. The supporting functionalities for improving the LLRF operability include the data buffering for the set-point table, feed forward table and signal waveform display. The logic for the necessary protective interlocks is also included. The operator screen of the Graphical User Interface (GUI) as shown in Figure 3 depicts these functionalities. Some of the high-level control functionalities are implemented and run on the host computer (or "IO/C" in EPICS). These functionalities include setting the LLRF control parameters, generating the cavity field set-point curve tables and feed forward control curve tables, plotting the signal waveforms, etc. The MATLAB LLRF GUI screens in Figure 1 and 2 illustrate that. The LLRF GUI screens are also where some of the operation automation sequencers reside.

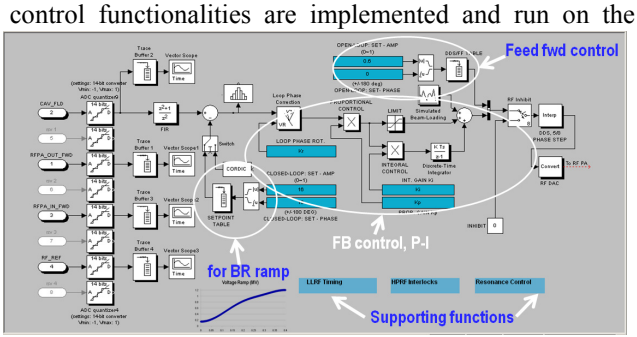

Figure 3. The LLRF Operator Interface screen shows some of the fast low-level controls that the field controller performs in its FPGA, and the control parameters are set through this screen

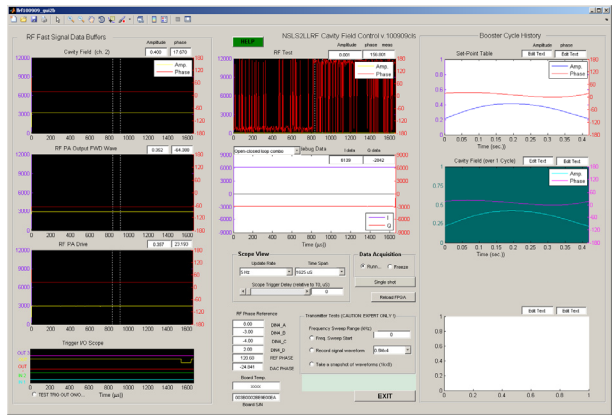

Figure 4. Signal wave display screen of the LLRF MATLAB GUI. This built-in digital scope function greatly improves the usability of the LLRF system.

FIELD TEST WITH SRF

Three samples of the digital LLRF field controller prototype were constructed and bench tested. Upon the completion of the controller firmware and software necessary for operation, the controller prototype was taken to Canadian Light Source (CLS) for field test in April, 2010. The CLS was chosen for field testing because it has the same RF system configuration as the NSLS-II which is not completed as of yet. The CLS SRF system contains a Thomson 300kW RF transmitter and a 500 MHz CESR-B superconducting cavity.

At CLS, the field controller under test successfully ran the RF power up to ~290kW, and stored a full beam current of 2.9 GeV/250 mA. Good operability and controllability were demonstrated.

The cavity field spectra captured with an HP 89410A Vector Signal Analyzer (VSA) in Figure 5 and 6 show the good performance of the new digital controller in suppressing the harmonic sidebands of the klystron HV modulator switching frequencies. The good control performance is also shown in cleaning up the noise floor in the close-in frequency range. With the existing CLS analog LLRF, there is a significant noise sideband produced by the cavity micro-phonics, as well as the beam instabilities.

The result of a statistical analysis in time-domain with the buffered cavity RF data (Figure 7) indicates that the NSLS-II design specification for a RF phase stability of 0.14 deg RMS is well met with this cavity field controller.

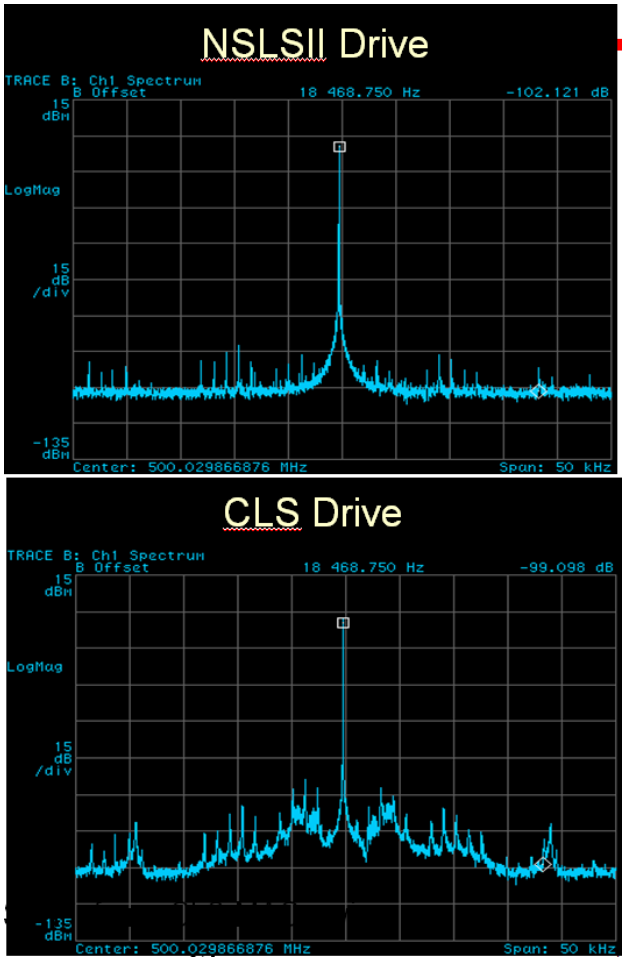

Figure 5. Spectra of the cavity field with a 2.9GeV/250mA beam, measured with HP 89410A VSA. The performance of NSLS-II digital LLRF controller vs. the existing CLS's analog LLRF (courtesy of Song Hu, CLS).

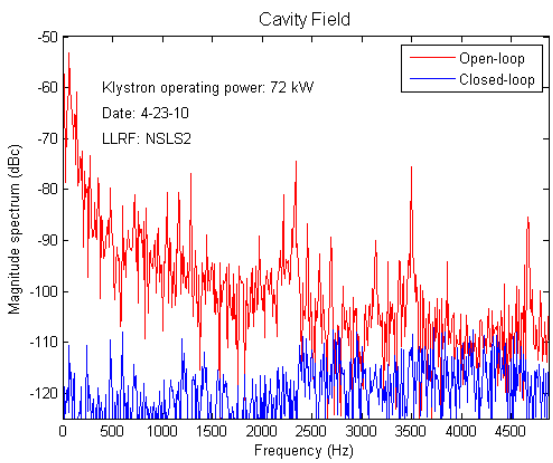

Figure 6. The effectiveness of the fast feedback control in suppressing the noise level of the cavity field in close-in frequency range (open vs. closed-loop control condition), calculated with the buffered data, NSLS-II LLRF, 72 kW, no beam.

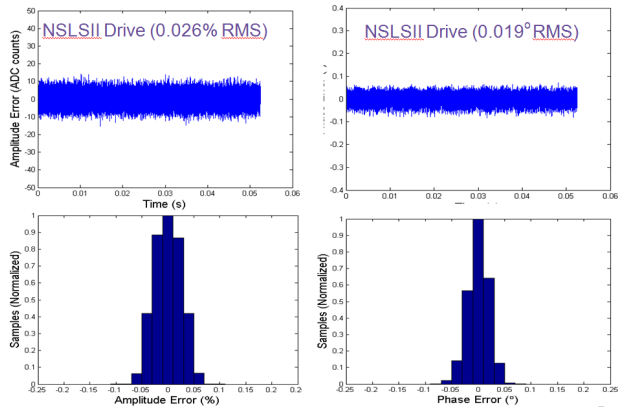

Figure 7. Cavity field stability with 250 mA/2.9 GeV beam, calculated with the buffered cavity field data, analysis bandwidth: 10Hz~100kHz (courtesy of Song Hu, CLS).

SUMMARY

The NSLS-II digital LLRF development is well on track with the success of its key component – the digital cavity field controller. The result of the field test at CLS has demonstrated that the digital field controller is capable of producing the required RF stability with the targeted high-power SRF for the Storage Ring.

ACKNOWLEDGEMENT

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