DIGITAL FEEDBACK CONTROL FOR 972 MHz RF SYSTEM OF J-PARC LINAC

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Abstract

A 972 MHz rf system is being developed for upgrade of the J-PARC linac. The rf field stabilities should be less than +/-1% in amplitude and $+/-1^{\circ}$ in phase. The basic digital llrf (low-level rf) concept is the same as that of the present 324 MHz llrf system with a compact PCI crate. The main alterations are rf and clock generator (RF&CLK), mixer and I/Q modulator (IQ&Mixer) and digital llrf algorithm. Since the typical decay time of the new system is faster (because its operational frequency is higher than that of the present 324 MHz cavity), chopped beam compensation is essential. The performance of the digital feedback system with a cavity simulator is summarized.

INTRODUCTION

The J-PARC linac delivers proton beams to the 3-GeV synchrotron (Rapid Cycling Synchrotron, RCS), following which the beams are injected to the Materials and Life Science Facility (MLF) or the 50-GeV synchrotron (main ring, MR). A digital llrf system has been successfully developed at the J-PARC linac. The rf field stabilities are approximately +/-0.2% in amplitude and $+/-0.2^{\circ}$ in phase [1-3]. Since the recommended values are +/-1% and $+/-1^{\circ}$, the rf field is 5 times more stable. The upgrade of the J-PARC linac will involve the further development of this present llrf system.

In the upgrade, a feedforward control system that can be used in the chopped beam mode, where the beam is modulated at a frequency of about 1 MHz, will be incorporated in the digital llrf system. Figure 1 shows the beam structure of the J-PARC linac. The macro-pulse beam duration is 500 μ s (maximum peak pulse current is -





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50 mA). This macro-pulse beam is chopped, and the intermediate pulses generated are synchronized to the injection timing of the RCS (and micro-pulse) [1]. Since the present rf system is operated at 324 MHz, the micro-pulse is bunched every 3.09 ns (=324 MHz). A 972 MHz digital llrf system is being planned for the upgrade of the linac. It is important to incorporate chopped beam compensation in the 972 MHz llrf system because the 972 MHz cavity is more sensitive to the chopped beam than the 324 MHz system is.

DIGITAL FEEDBACK SYSTEM

The schematic of the 972 MHz digital llrf system is shown in Fig. 2. An FPGA board having four 14-bit ADCs and four 14-bit DACs is the daughter card of the commercial DSP board ("Barcelona"). The DSP board is used for control purposes, for example, to provide cavity tuner-control, which is a slow, complicated process. The FPGA board concentrates to the fast llrf feedback.

Rf (972 MHz), LO (local oscillator, 960 MHz), and clock (48 MHz) signals are generated from the 960 MHz signal input to the RF&CLK board. An IQ&Mixer board contains two I/Q modulators and four downconverters. These two boards have been newly developed on the basis of the 324 MHz system.

Cavity pickup and cavity input signals are downconverted to the intermediate frequency of 12 MHz. The IF signals are directly acquired by the ADCs. The sampling frequency of the ADCs is 48 MHz. After the I (in-phase) and Q (quadrature) separation from the IF signals, PI feedback is provided.



Figure 2: Schematic of the 972 MHz digital llrf system.

SYSTEM PERFORMANCE

The performance of the 972 MHz digital llrf system is evaluated under various conditions. First, simple feedback is used without any beam loading effects. Then, chopped beam loading is applied using an rf combiner. Beam loading was adjusted to the typical design value. Two beam loading compensation schemes—the present beam compensation scheme for the 324 MHz system and the new algorithm for chopped beam compensation—are compared. A timing scan of chopped beam compensation is carried out in order to examine the margin of delay adjustment.

Feedback Only

The rf stabilities under feedback are +/-0.2% in amplitude and $+/-0.12^{\circ}$ in phase, as shown in Fig. 3. These values are identical to those of the present 324 MHz llrf system. This indicates that the new components including the RF&CLK and IQ&Mixer boards are working well.

Chopped Beam Loading

Since the typical decay time of the 324 MHz system is $20 \ \mu s$ (loaded Q values are in the range of 15,000–20,000), the effects of the intermediate pulse (chopped beam) are small. On the other hand, the 972 MHz rf cavity has a shorter decay time, which means that further compensation based on the intermediate beam structure is essential for stable rf control. The typical cavity parameters of the 972 MHz system are as follows:

RF consumption at cavity: 1.5 MW Beam loading power: max. 0.28 MW Beam phase: -30° Q value: 17,000 Optimum loaded Q: 7,800 (decay time: ~2.5 μs) Beam loading: max. ~8%

The cavity simulator is a TE_{111} -mode cavity resonator.



Figure 3: RF stabilities under feedback. Amplitude (upper left), phase (upper right), amplitude during flattop (lower left), and phase during flattop (lower right).

The loaded Q value of the cavity simulator is adjusted to 8,000. In order to emulate the beam loading, the modulated rf output is combined before the cavity input (chopped beam generator). Figure 4 shows that the amplitude decreases under beam loading without feedback. The beam loading can be modified by changing the I and Q components of the beam loading generator. Beam loading is adjusted to approximately 10%, which is slightly higher than the maximum operation condition.



Figure 4: Beam loading effects.

Simple Beam Loading Compensation

The present 324 MHz llrf system employs average beam compensation, where feed forward is generated by the macro-pulse gate signals. Since the 324 MHz cavity is not sensitive to the chopped beam, this feed-forward compensation works well in the 324 MHz system.



Figure 5: RF stabilities (amplitude and phase) under feedback.

The same algorithm was applied to the 972 MHz system. The measured stabilities are $\pm/-0.7\%$ in amplitude and $\pm/-0.4^{\circ}$ in phase, as shown in Fig. 5. Although these values satisfied the requirements, small margins are left for accelerator operation.

Chopped Compensation

Chopped beam compensation is feed-forward with the chopped modulation, as shown in Fig. 6. The intermediate pulse (chopped beam) signals are multiplied in the FPGA and added to the feedback output. Since the chopped signal is not synchronized to the FPGA clock (48 MHz), the output of the feed-forward has a jitter of 21 ns (=1/48 MHz). Figure 7 shows the rf stabilities obtained with feedback and chopped beam compensation. The stabilities are +/–0.4% in amplitude and +/–0.2° in phase.



Figure 6: RF stabilities under chopped beam compensation (figure is temporary).



Figure 7: RF stabilities under chopped beam compensation.



Figure 8: Chopped delay scan.

Delay Scan

Chopped beam compensation can be delayed with the 48 MHz clock inside FPGA (chopped delay). In order to estimate the tolerance of the chopped delay, the rf stabilities are measured with various chopped delays (Fig. 8). The chopped delay should be adjusted within +/-3 clocks.

SUMMARY

We studied the upgrade of the present 324 digital llrf system at the J-PARC linac. A new 972 MHz digital llrf system was evaluated. The basic hardware satisfies the similar signal/noise ratio under feedback using a cavity simulator. One of the salient features of the new system is the incorporation of chopped beam compensation. It has been confirmed that the feed-forward table must be synchronized with the chopped beam in order to satisfy the rf stability requirements. The tolerance of the optimum delay of the chopped signals is approximately +/- 3 clocks, which is reasonably wide for accelerator operation in order to satisfy the requirements.

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