DEVELOPMENTS IN SOLID-STATE MODULATOR TECHNOLOGY TOWARDS HIGH AVAILABILITY*

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Abstract

Solid-state based high-power modulators utilize new technology yet must meet the operational needs of a high reliability facility. This modulator technology is in use at the SNS, and is under consideration and development for future machines, such as the PEFP. Through operational experience and a sustained development effort, a number of improvements have been deployed in the SNS modulator system to meet the high availability demands of operating facilities. The operating experience and development efforts of the world-wide community will also be reviewed.

INTRODUCTION

Modulator systems utilize technology and theory from multi-disciplinary fields and focus on compressing electrical energy in time, thereby expanding the output to high peak power pulses. Although techniques for generating electrical pulses of large amplitudes existed prior to World War II, the development of equipment to drive magnetron oscillators for microwave radar started the high power modulator specialization field [1]. While initially focused on defense-related applications, several scientific applications have also arisen, including particle accelerators, fusion systems, effluent treatment devices, and a myriad of biomedical applications [2].

Over the past decade or two, significant advances in new solid-state devices and improvements in high energy density components have led to a reduction in sizes of systems [3]. Also, developments in these areas have allowed engineers to take advantage of techniques and topologies traditionally reserved for the field of power electronics, resulting in more efficient systems. In the field of accelerators, this evolution will result in higher reliability systems with excellent efficiencies rivaling switch mode power supplies and requiring less-frequent maintenance cycles [4].

One such system is the High Voltage Converter Modulator (HVCM) presently in operation at the Spallation Neutron Source at Oak Ridge National Laboratory. Virtually identical systems are also in use at the SLAC National Accelerator Laboratory [5] to support ILC component testing and one is scheduled for delivery to the Proton Engineering Frontier Project at KAERI [6] later this year. A similar system is under development at E2V [7].

In this paper, a general overview of the HVCM system will be given in the first section. Operational experience at the SNS, with particular emphasis on the evolution of the HVCM system since initial commissioning, will be presented in the second section. The third section will concentrate on recent developments not previously reported as well as ongoing activities. The final section will focus on future developmental goals. Where appropriate, parallels will be drawn to existing modulator operational experiences at other facilities.

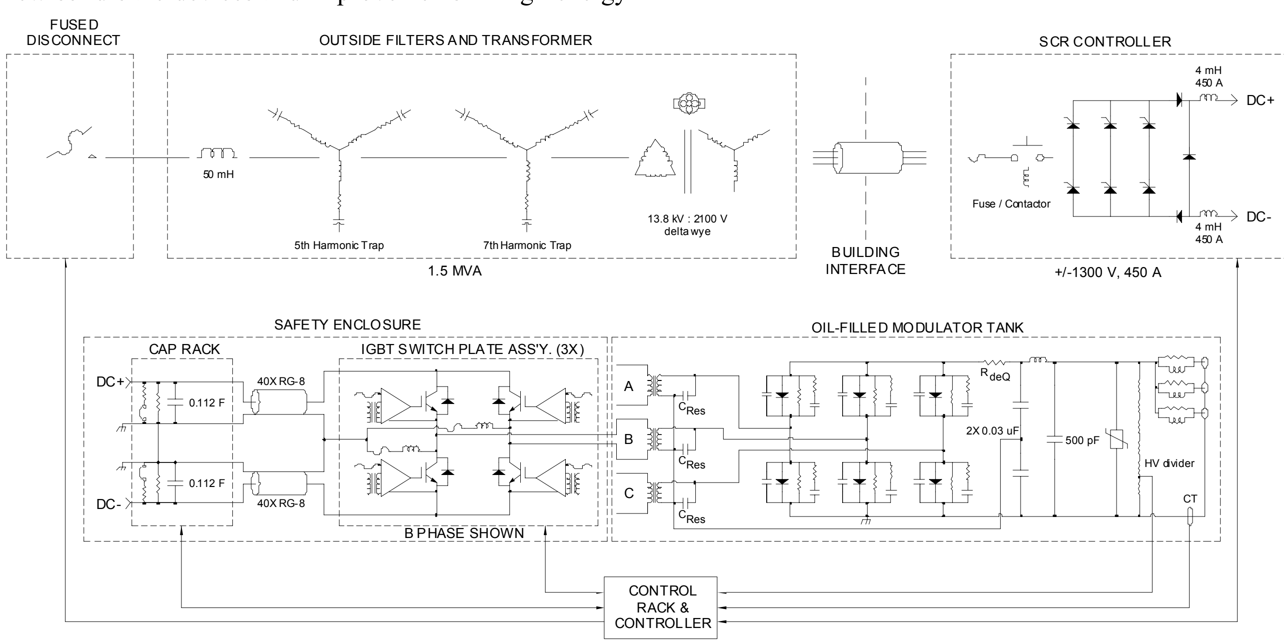

Figure 1: Simplified HVCM Block Diagram.

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HVCM SYSTEM OVERVIEW

A block diagram of the HVCM system is shown in Figure 1. A more thorough description of the system is given elsewhere and therefore only highlights will be repeated here [8]. The prime power is derived from a 13.8kV:2100V 1.5MVA substation cast-coil Δ:Y transformer complete with 5th and 7th harmonic traps. A ±1300V, 450A water-cooled SCR rectifier follows, incorporating soft-start and voltage regulation. Two large low inductance self-clearing metalized hazy polypropylene capacitor banks connected to the DC bus provide the primary energy storage for the system, storing up to 200kJ combined.

Three snuberless IGBT H-bridge networks, operating at 20 kHz, are used to drive 3 independent high voltage step-up transformers located in an oil-filled tank. Utilizing each transformer's leakage inductance with capacitor placed across the secondary produces a resonant circuit, providing for soft-switching of the IGBTs when properly tuned. Individual large series-stacked diodes are used to rectify the output pulses, after which the signals are combined and fed through a standard pi filter. A HV divider and current transformer, along with protection elements and output connectors, complete the HV tank. A DSP- and FPGA-based controller is used to monitor and record key system signals as well as provide fast-shutdown capability for system protection.

HVCM OPERATIONAL EXPERIENCE

The first modulator system was installed and operational by late 2002. Other than a recently-added modulator to reduce the number of klystrons each modulator in the cold linac, all 14 other modulators were operational by April 2005. Initially, operation was limited to not exceed 30 Hz until operational experienced was gained on the HVCM units. However, since April 2008 the SNS facility has been operating solely at 60 Hz.

Early on in the design program, an analysis was completed to predict the MTBF of the HVCM systems based on MIL HDBK 217F. Initial predictions of MTBF for the system were 3480 hours before any maintenance schedules or mitigation factors were applied. The SCR controller was identified as the largest contributor to the MTBF calculated figure. After adjusting component MTBF rates for scheduled maintenance and implementing standard techniques for improving poor failure rate components, the anticipated system MTBF is now about 20,000 hours. While still short of the goal of 23,000 hours [9] necessary to meet equipment availability goals, it is only an estimate and the real statistics must be borne out in the operational performance of the HVCM.

Early operation of the HVCM systems quickly supported the weaknesses identified in the MTBF analysis when problems with the SCR controller units were encountered, albeit at an order of magnitude lower in operational hours than predicted by the analysis. While many of the improvements on the SCR unit are summarized elsewhere [10], additional improvements have subsequently been made to this critical piece of equipment. More recent notable enhancements include the addition of a line conditioner on the control power feed for improved noise immunity, installation of fast over current shutdown features to protect the SCR devices during modulator faults, and control enhancements to phase back the SCRs prior to rapid removal of the line current.

Figure 2 shows the evolution of the MTBF for the two major subsystems associated with the HVCM. The SCR unit has steadily improved since the early poor performance due to the upgrades discussed earlier. The modulator system started strong, but quickly declined when SCL HVCM units were brought online and operated. Several measures were taken to stabilize the modulator reliability [11], resulting in a nearly flat reliability performance until 60 Hz operation was initiated at the approximately 200,000 total operational hours mark. Since 60 Hz operation has commenced, the modulator performance has continued to decline and the SCR performance has not improved at the previous rate.

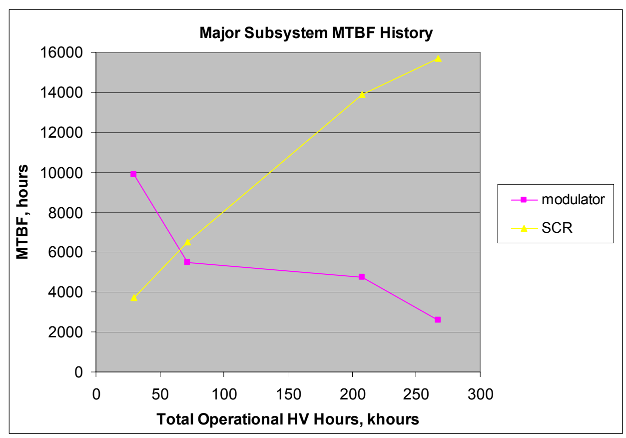

Figure 2: Evolution of Reliability for Modulator Subsystems.

60 Hz modulator reliability has been plagued primarily by large, low inductance H-bridge bypass capacitor failures and IGBT shoot-thru and over current faults. Some capacitor failures have generated high enough temperatures to ignite low flash point materials inside the modulator safety enclosure at ORNL [12]. Capacitor failures have occurred well before their specified lifetime and, while analysis by the manufacturer is ongoing, the extensive post-pulse current ringing measured on these capacitors may be a contributing factor [13]. Efforts are nearly complete to replace the capacitors with larger units with reduced dielectric stress, primarily to mitigate the perceived end of life on the original capacitors and to allow time to evaluate alternate capacitors using higher flashpoint dielectric fluids and/or self-clearing metalized electrodes. Self-clearing technology is favored as it allows the user to track the capacitor lifetime by monitoring the capacitance value during operation and remove units from service as required. Additionally, no

low flashpoint dielectric fluids are employed and catastrophic failures are very rare with these units [14].

IGBT faults grew exponentially when 60 Hz operation of the neutron production facility became the standard, but have also occurred at lower operating frequencies at ORNL and SLAC National Accelerator Center [15]. Component aging and resultant timing drifts of the V_{GE} drive signal were previously observed with the nominal IGBT gate drives, so protection features were put in place to prevent transformer saturation and resulting over currents in the IGBT modules [16]. Controller-induced shoot through is also suspected. Post mortem inspection of failed IGBT modules revealed improper heat sink compound application and probable locations for hot spot development so a more rigorous quality control program was implemented. However, with the simultaneous failure of capacitors or those immediately preceding IGBT failures, tracking a root cause for a given failure event became difficult. Very large currents through the IGBTs resulting when capacitors arced internally, limited only by the excessive drive voltage levels, clearly exacerbated the IGBT failure frequency and likely explain the majority of the failures.

RECENT DEVELOPMENT ACTIVITIES

Recent developmental activities for the HVCM system have focused on three primary areas, mainly the IGBTs and associated ancillary systems, the large bypass capacitors, and the controller which generates the gate timing signals and provides fast equipment protection functions. After observing aging effects and recognizing the impact of high drive levels on the IGBTs' ability to ride through a fault, significant development was focused in this area. To minimize IGBT collector saturation current levels, the gate drive voltage was reduced and the on and off resistances made independently adjustable to compensate for variations between devices on and off times. Active detection of excessive di/dt and over-voltage is also provided. Additional inputs and outputs were added to provide for interlocking between shoot thru devices and to allow for future expansion with next generation controllers. A simplified block diagram of the new driver is shown in Figure 3 and additional details can be found elsewhere [17].

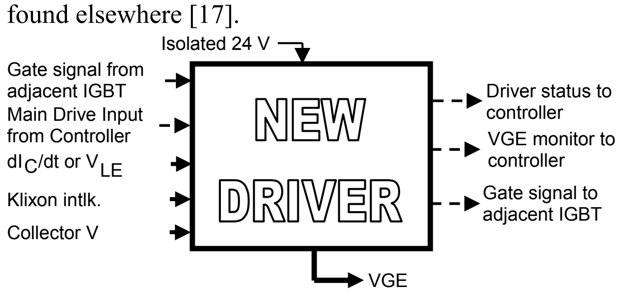

Figure 3: Functional Block Diagram of Next Generation IGBT Gate Drive Circuit.

Careful measurement of end-of-pulse collector-emitter voltages on the IGBTs revealed some potentially harmful operating conditions [18]. The existing controller abruptly terminates the gate pulses to each IGBT when the input gate signal is removed which, in some circumstances, results in large over-voltages appearing across the IGBT terminals due to L(di/dt) effects. Figure 4 summarizes these results for one of the H-bridges over one complete 20 kHz cycle. Note that the largest over-voltages, approaching the IGBT maximum voltage ratings, occur when the collector current is truncated shortly after the initiation of the device's conduction. This is likely due to the drift region not being fully conductivity modulated, leading to very rapid carrier recombination upon removal of the drive. In a three phase system it is not possible to truncate the pulse at such a point where over-voltages are minimized for all IGBTs, but optimizing to keep the over-voltage low on the A phase H-bridge was recently performed with no IGBT failures since that time. Extending the IGBT gate signals to complete an existing 20 kHz half-cycle after termination of the gate pulse is also being evaluated to eliminate all post-pulse over-voltages.

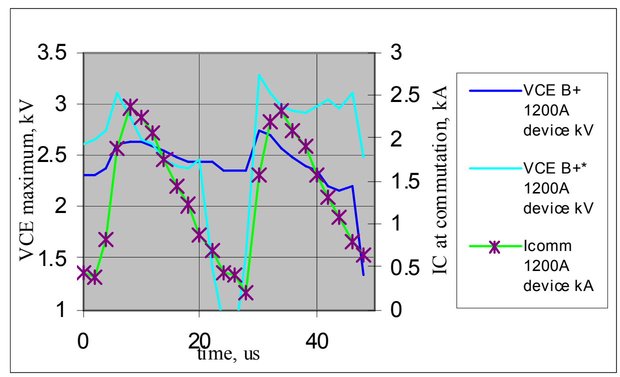

Figure 4: IGBT V_{CE} Over-Voltage Variations with Commutated Collector Current on the H-Bridge.

The commercial demand for higher voltage IGBTs has evolved to the point where 4500 V, 1200 A are now available in two package styles. These are presently being evaluated in an effort to provide higher voltage de-ratings and lower failure in time (FIT) rates for operational IGBTs. The traction motor industry typically specifies FIT < 100 for their applications and one industry representative recommends that the HVCM strive for < 10 [19]. Unfortunately, these higher voltage devices appear to be optimized for minimal conduction losses and not low switching losses, so excessive thermal cycling is anticipated, especially at turn-off [20].

Westcode T1200EA45E Press Pack IGBTs with a corresponding external anti-parallel diode were incorporated into a modified H-bridge switch plate assembly recently [21]. Figure 5 shows a photograph of the assembly. Initial peak power measurements at SLAC were quite encouraging although higher switching losses were measured. During attempts to bring the switch plate up to full average power at the SNS a catastrophic shoot thru event occurred. While this failure occurred at lower than nominal levels of stored energy, the failure did not result in destruction of the Press Pack package. The switch plate is undergoing further testing to attempt to understand the failure mechanism.

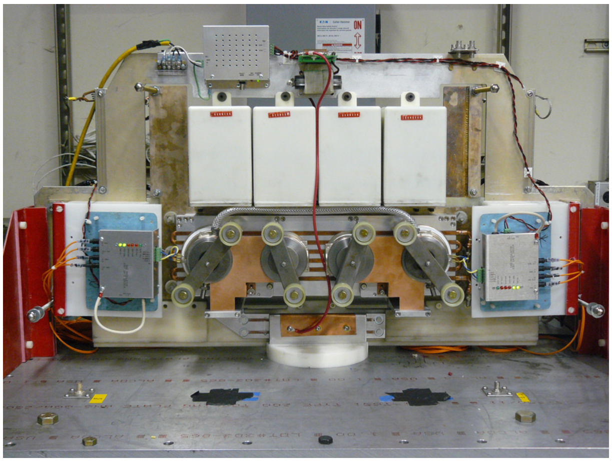

Figure 5: Retrofittable Westcode Press Pack IGBT Assembly with External Antiparallel Diodes.

Another 4500 V, 1200 A IGBT will soon be available as engineering samples from Mitsubishi. The device, CM1200HG-90R, is package-compatible with existing devices, making retrofitting easier. The published preliminary data sheet indicates that, while turn-on switching energies are comparable to existing 3300 V devices, turn-off switching energies are about 50% higher when scaled for the same test circuit conditions [22].

A next-generation IGBT controller is presently under development. The system new controller is envisioned to serve 3 major functions, mainly to drive the IGBTs, provide feedback and modulation schemes to address pulse droop and component drifts, and log critical analog signals and operational set points for retrieval via EPICS during routine operation or after system faults. Phase and frequency modulation will likely be employed to mitigate switching loss asymmetries encountered by utilizing phase modulation alone to compensate for energy storage capacitor droop [23]. Timing corrections will be employed based on measurements of flux signals and digitally-converted IGBT V_{GE} waveforms to virtually eliminate possible induced fault modes due to component drift. The system is currently being developed with LabVIEW R Series DAQ card with reconfigurable FPGA and embedded analog and digital I/O combined with a real-time processor.

FUTURE DEVELOPMENT GOALS

While it is anticipated that the previously-implemented system enhancements combined with those presently under development will vastly improve the overall system reliability and greatly enhance the HVCM's ability to recovery gracefully from faults, additional developments are envisioned to further enhance the overall system availability and extend the topology to operate at higher power levels. The primary areas of focus going forward include improving the energy storage capacitor bussing, provide a series opening switch between the energy storage capacitor and the H-bridge assemblies, adding harmonic traps to the modulator output to improve the voltage ripple, and possibly add a "N+1" redundant H-bridge to the system.

Analysis of the capacitor and bus currents associated with the main energy storage capacitor reveals that there are multiple ground loops and not all return current flows on the multiple parallel coaxial cables that connect the H-bridges to the energy store. Figure 6 shows the main capacitor bank current (Channel 3) and the return cable current (Channel 1). Clearly, the multiple ground loops share current during the pulse, creating post-pulse ringing that can lead to excessive stress on critical components.

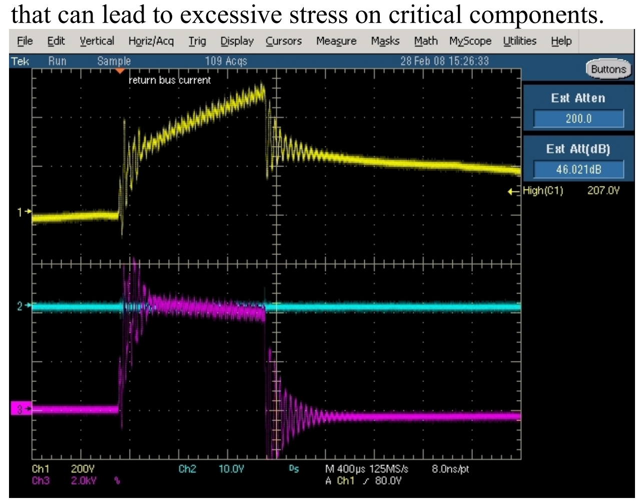

Figure 6: Capacitor Return Current Waveforms. Channel 1 (yellow) is the return bus current at 200 A/div and Channel 3 (magenta) is the energy storage capacitor current at 2000 A/div.

A series IGBT, placed between the main energy storage capacitor bank and each H-bridge assembly, is also under consideration. Originally envisioned to minimize collateral damage to the switch plates by minimizing the available fault energy, it could also be used to incorporate a redundant H-bridge switch plate to the modulator. With the series IGBT switch in place, a redundant switch plate, and the appropriate modifications to the controller, a fault on one switch plate could be detected and, in between pulses, the controller could automatically remove the faulty switch and add the redundant unit to the circuit, thereby continuing operations virtually uninterrupted. All present upgrades are being developed such that they are capable of support this future redundant H-bridge concept should it become necessary to implement it.

CONCLUSION

While the HVCM system is a major contributor to the overall accelerator downtime, it has supported 60 Hz neutron production operation at the SNS for over a year. This represents total HVCM operational hours approaching 100,000 hours at this repetition rate. Short-term solutions have been put in place to keep the systems operational to maintain neutron production capability while allowing additional time to investigate permanent system improvements. Most of those upgrades are presently under development and will be installed and commissioned in the upcoming years. There is also a renewed interest in the HVCM technology from other international accelerator facilities, so additional opportunities for collaboration exist.

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