DESIGN OF LOW LEVEL RF CONTROL SYSTEM FOR ACCELERATOR*

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Abstract

The low level RF (LLRF) control system for PLS is being upgraded to improve the performance of the system. The LLRF control system under development consists of FPGA and high speed ADC and DAC as well as analog front-end devices which process the signal from cavity and to RF high power system. In addition, it utilizes digital signal processing technology based on FPGA.

In order to optimize the accelerating electric field in the cavity, it is required to maintain field stability less than ±1% in amplitude and 1° in phase. And the resonance condition of the cavity should be monitored and controlled. The various digital signal processing theories such as digital filters, Cordic, PI control enable to meet these requirements and to control the feedback signal less than a microsecond. The LLRF control system is also equipped with the Ethernet by the cPCI. The preliminary design study and modeling on the LLRF control system for PLS superconducting cavity will be described in this paper.

INTRODUCTION

The Pohang Light Source (PLS) to be upgrade consist of two superconducting cavities (SC) as well as two normal conducting cavities (NC) for getting lower emittance, and higher beam energy. The goal which we want to achieve in performance and primary parameters relative to the PLS-II storage ring is shown in table 1 [1].

Table 1: Parameters of PLS and the PLS-II Storage Ring

Parameters	PLS	PLS-II
Energy [GeV]	2.5	3.0
Current [mA]	200	400
Emittance [nm-rad]	18.9	5.9
Circumference [m]	280.56	281.82
Revolution frequency MHz]	1.068	1.0638
Harmonic number	468	470
RF frequency[MHz]	500.082	499.973
Cavity type	NC	SC+NC
No. of RF cavities	4	2SC+2NC
Accelerating Voltage[MV]	1.6	3.3+0.8

As the beam energy, beam current, and beam emittance are changed significantly, the PLS-II should have remarkable differences with respect to the beam loss power and the RF voltage compare to those of the PLS. Besides, superconducting RF cavity is very sensitive because of the high loaded Q value and the thin walls of cavity. It means that the LLRF control system which has advanced performance and high accuracy is needed to control the accelerating field of RF cavity efficiently [2].

The developing the PLS-II LLRF control system adopted the digital controller based on FPGA with analog RF board. Because digital LLRF control system is reliable and easy to change the algorithm. In addition, it can be implemented by simple circuit and it has high precision, so that we achieve to meet the requirements for good performance.

PRELIMINARY DESIGN OF LLRF CONTROL SYSTEM

The preliminary design of the LLRF control system for PLS-II is shown in figure 1. The LLRF system is consist of three main components as following.

- Two analog front end parts for RF input and output.
- Local oscillator (LO) frequency and clock signal (CLK) distribution system for RF signal conversion and ADC/DAC operation, respectively.
- Digital control board for cavity field control and communication with local PC.

The LLRF control system utilizes IQ sampling method and IQ modulation method for signal processing. IQ components have amplitude and phase information about RF signal and symmetrical characteristic, so that it is suitable to digital control system. LO and CLK generation is carried out by commercial DDS chip. The RF signal detected in cavity is converted to intermediate frequency (IF) by down-conversion, and the IF signal is changed to digital signal through ADC. So, we can control the RF signal easily and exactly by using digital signal processing technique such as digital filters, Cordic and PI control.

IF Signal and IQ Sampling

The RF signal (499.973MHz) of PLS-II is too high to control directly. So the down-conversion process from RF pick-up signal to proper IF signal, preserving information about the amplitude and phase of the RF field is needed.

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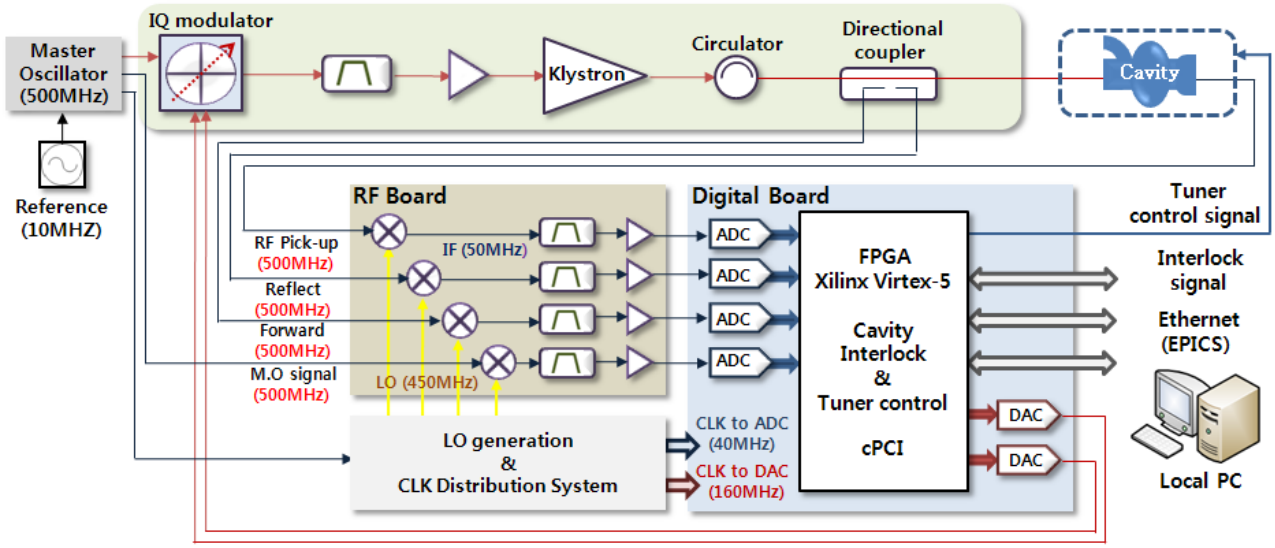

Figure 1: Digital LLRF control system of PLS-II architecture.

We set the IF signal as 50MHz, LO signal as 450MHz to take into account the mutual influences between accuracy, latency, noise and jitter vulnerability [3]. Thus, the detected RF signals (500MHz) are down-converted to IF (50MHz) signals by mixer, the IF signals flow the ADCs of the digital control board.

In order to implement the cavity field control digitally, the IF signals have to be translated to digital signals. We adopted the IQ sampling technique which has low latency characteristic. The I and Q components are represented in Cartesian coordinates and symmetric each other. So, that can be easily calculated in digital controller [4]. We set the sampling rate as 40MHz because of the limitation of ADC technology [3]. The sampling process of the PLS-II is shown in figure 2.

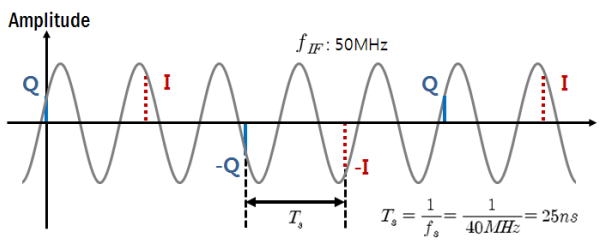

Figure 2: IQ sampling scheme .

IQ Modulation and Up-Conversion

We choose the IQ modulator (AD8345 from Analog device) for IF signal up-conversion. The AD8345 is quadrature modulator which operates in the frequency range between from 140MHz to 1GHz. As shown in figure 3, master oscillator signal is split into I component and Q component in the AD8345, and the I/Q components are mixed with those of IF signal from digital control board. Finally, the outputs of the two mixers are recombined and up-converted in the output stage [5].

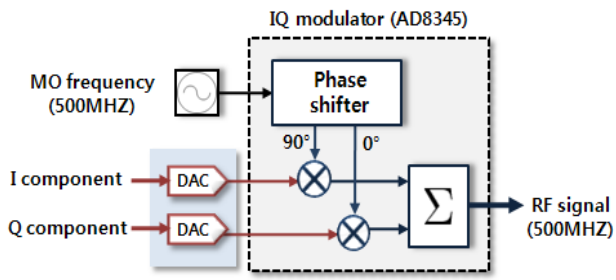

Figure 3: IQ modulation and up-conversion.

LO & CLK Generation

In this LLRF control system, 450MHz LO frequency, 40MHz CLK signal and 160MHz CLK signal are required to implement up/down conversion and ADC/DAC operation. Thus, we adopted commercial DDS chip (AD9858 from Analog device) to generate LO and CLK. The AD9858 has good harmonic characteristic compare to another commercial DDS chip (The phase noise is 82dBc when the output frequency is 50MHz) [6].

The first step for LO and CLK generation is to obtain the 50MHz signal through AD9858. The 50MHz signal is combined with the 500MHz Master oscillator (MO) frequency, so that we can generate 450MHz LO frequency. The 50MHz signal from AD9858 is used to generate CLK signal, simultaneously. The AD9510 which is 1.2GHz clock distribution IC provides 40MHz CLK signal for ADC and 160MHz CLK signal for DAC with low jitter and phase noise by using the 50MHz signal [7].

Cavity Field Control

The PLS-II will use CESR-III cryomodule which has a single cell SC cavity with the 500MHz, TM010 mode resonant, as well as NC cavity. In general, SC cavity has very high Q value compare to NC cavity. Thus, the precise control technique is required for SC cavity. The PLS-II SC cavities operate at a CW mode, so the Lorentz force detuning influence is not serious consideration. In this reason, we don't need to utilize the feedforward control technique unlike another LLRF control system for super conducting cavity [2]. The parameters of the PLS-II SC cavity are shown in table 2.

Table 2: RF Parameters of the PLS-II SC Cavity

Specification	Value
Resonant Frequency [MHz]	499.973
Normalized shunt impedance [Ω]	89
Unloaded Q (Q_0)	~1x10^9
External Q (Q_{ext})	1.37x10^5
Loaded Q (Q_L)	1.37x10^5
Maximum detuning range [Hz]	2933
Half band width (-3dB point) [kHz]	11.46

The LLRF control system of the PLS-II is based on IQ modulation technique. Thus, RF signal which has information about amplitude and phase of RF field in the cavity is translated to I/Q component signals to control. The figure 4 shows that the I/Q components variation of PLS-II SC cavity voltage depending on different detuning frequency induced by microphonics. It is simulated by matlab simulink after modelling the SC cavity as a RLC resonance circuit [4].

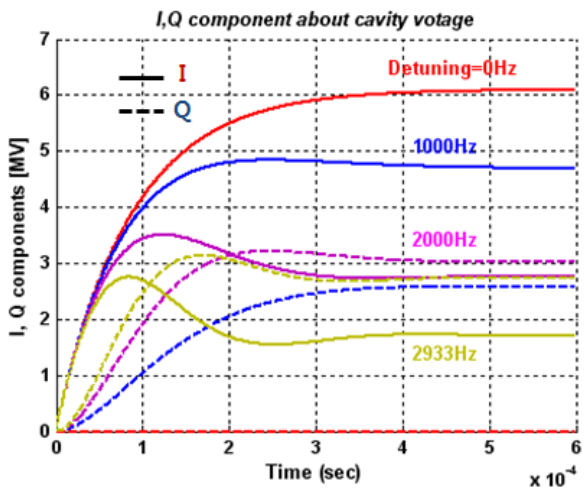

Figure 4: Cavity voltage step response represented by I, Q.

The digitized I/Q signals from ADCs are not ideal DC signals but signals with having spurious. In order to reduce the harmonics, we utilize the FIR digital filter which has no phase distortion in its signal processing period. After filtering, it is possible to acquire the exact data about amplitude and phase of RF voltage in the cavity by using CORDIC algorithm. The CORDIC algorithm performs trigonometric calculations by only addition and subtraction without multiplication, so that we can reduce the time for calculation. The obtained signals from CORDIC algorithm are compared with reference signal and provide the error signal for PI control. The PI controller enables to improve the system performances relative to response speed, bandwidth and state error. After that, the controlled signals are translate the I/Q signal by CORDIC algorithm, again and sent to IQ modulator. The digital signal processing techniques as referred above are programmed and loaded into the FPGA chip (Xilinx virtex-5). With using these control algorithms, we can achieve to maintain field stability less than ±1% in amplitude and 1° in phase. The proposed LLRF control system is also equipped with the Ethernet by the cPCI.

SUMMARY

For the proper operation of PLS-II superconducting cavity, the LLRF system which has advanced performance with higher stability and accuracy compare to the existing LLRF control system is required.

In this paper, we designed the LLRF control system based on FPGA, preliminary. The system utilizes IQ method and digital signal processing technique such as FIR filter, CORDIC algorithm and PI control. It enables to control the RF cavity voltage correctly. In the next year, the first prototype developing is completed.

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