SPALLATION NEUTRON SOURCE HIGH-POWER PROTECTION MODULE TEST STAND*

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Abstract

The Spallation Neutron Source (SNS) High-Power Protection Module (HPM) provides interlocks and fast shutdown for the radio frequency (RF) system to protect the accelerating structures and high power RF (HPRF) Distribution System. The HPM has required some functional upgrades since the start of beam operations and an upgrade to the HPM test stand was required to support these added features. The HPM test stand currently verifies functionality, RF channel calibration, and measurement of the speed of shutdown to ensure the specifications are met. The upgraded test stand was implemented in a Field Programmable Gate Array (FPGA) to allow for future growth and flexibility. Work is currently progressing on automation of the test stand to better perform the required module calibration schedule.

INTRODUCTION

The RF control system at the Spallation Neutron Source (SNS) consists of a Reference Timing System, Field Control Module (FCM), and High-Power Protection Module (HPM). The HPM monitors RF and fiber-optic arc (FOARC) signals along with other hard-/software based channels to provide rapid RF shutdown operation. Firmware updates and upgrades have been made on the HPM to support machine operation [1, 2]. Verification of the HPM prior to its installation to the SNS linear accelerator (LINAC) is done utilizing the HPM Test Stand [3]. The test stand is also used to troubleshoot the HPM and test new firmware before releasing the changes in the machine.

In this report, requirements and functionalities of the HPM Test Stand are summarized and its upgrade and further improvements are discussed.

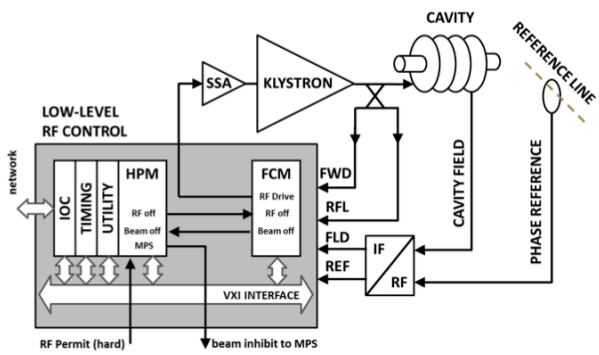

Figure 1: SNS LLRF control system [2].

* SNS is managed by UT-Battelle, LLC, under contract DE-AC05-00OR22725 for the U.S. Department of Energy.

HPM TEST STAND SETUP

HPM Test Stand is comprised of three separate functional blocks; the HPM test chassis, RF test equipment, and VXIbus crate (Fig. 2). The test chassis provides the digital stimulus/response and delivers it to the HPM through the VXI interface via the Paddle Board. The Paddle Board is an external interface card designed to provide VXI interface to the HPM test chassis and enable connectivity check of bus signals. Test equipment is utilized to provide the required RF signals for calibration of the HPM RF channels. The VXIbus crate along with the HPM test stand Paddle Board simulates installation of a HPM under test. Communication is provided to the user through an Input/Output controller (IOC) and test screens written using the Experimental Physics and Industrial Control System (EPICS) interface.

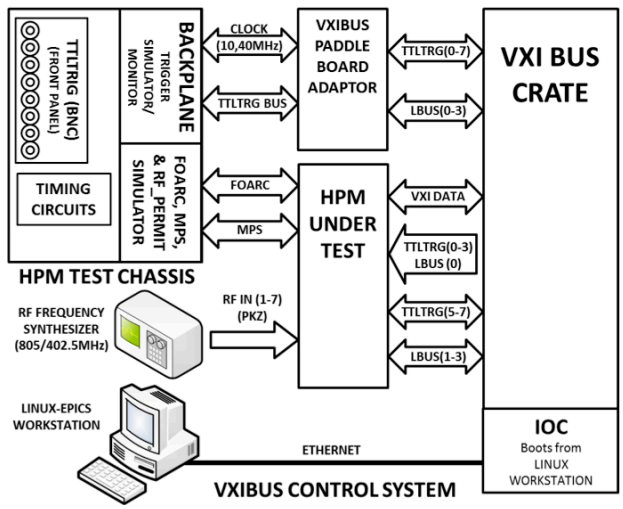

Figure 2: HPM test stand setup block diagram.

The HPM Test Chassis has four functional blocks: the Timing Circuit, Trigger Simulator/ Monitor, FOARC/MPS/RF_Permit Simulator, and VXI Interface Bus Paddle Board. The existing test chassis is implemented with discrete logic components and basic functionality tests are provided for. In order to verify updated or upgraded HPM functionality and to cover realistic machine operation scenarios, flexibility of the test stand is desirable.

HPM TEST STAND CHASSIS

The HPM Test Stand Chassis is designed and developed to generate various fault signals to simulate the operation of the system in the machine environment. The

main printed circuit board located in the chassis consists of the Timing module, Front/ Backplane interface, and FOARC module. The functionalities are implemented on a single Field Programmable Gate Array (FPGA) utilizing a Xilinx Spartan 3E PQ208 (Fig. 4). The MPS fault indicator is isolated using an opto-coupler (HCPL-2612) and is included on the board. A VXI interface is required to communicate with the HPM backplane signals and is implemented on a separate board (Fig. 5). For display and testing purpose LED indicators and BNC connectors are populated on the front panel of the chassis. Several input switches are provided to simulate operational signals, these include superconducting RF (SRF) tune, Beam permit, and RF permit.

Timing Module

The FPGA divides a 50MHz clock from an external crystal oscillator down to sub clocks (40 MHz, 10 MHz, 10 kHz, and 60 Hz) and generates the main timing signals (PREPULSE, RF_GATE, FLT) required. The PREPULSE occurs at 60 Hz with the RF_GATE being generated 4.7msec after the falling edge of PREPULSE. The current test stand scenario has the RF_GATE set to a 1msec pulse width as shown in Fig. 3. For LINAC operations, all RF accelerating activities are designed to occur during the RF_GATE window with most faults only needing to be detected during this period. The test stand has been implemented to better test these faults by being able to generate fault (FLT) signals at various times within the RF_GATE.

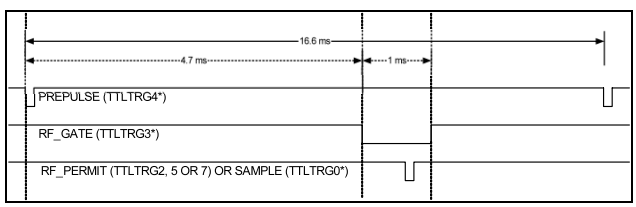

Figure 3: HPM test stand signal timing.

Front Panel and Back Panel (VXI) Interface

The front panel provides manual input switches and indicators for all major faults (SRF Tune, Beam Permit, RF Permit L/C/R), LED indicators, BNC connectors, and adaptors (HPM_MPS, HPM_FOARC, HPM_RF, and VXI crate). Timing signals and user input signals are transferred (TTL triggers/LBUS signals) to VXI Crate through VXI interface board (Fig. 5) and delivered to HPM. Responses to the inputs are visible to the user via EPICS screens loaded on the local Linux machine.

MPS and FOARC Module

The HPM monitors and detects both RF and fiber-optic arc (FOARC) signals. Once any fault is detected, the HPM shuts down the RF drive out of the FCM and signals to the machine protection system (MPS) to shut the beam down. Response time and fault detection logic are the main parameters to be verified with the test stand. The RF permit switch on the front panel simulates the RF permit input signal from the vacuum system (active high +24V) is delivered to HPM and is capable of generating a fault. The HPM MPS output then reports a fault signal to the MPS once the RF permit drops.

The FOARC (14 channels) faults must also be properly tested and are synchronized to the rising edge of the RF_GATE signal to ensure that the fault occurs within the RF on period. A fault signal is generated sequentially to all FOARC channels to verify functionality, these fault signals can be generated at various speeds and locations within the RF pulse to better check HPM Hardware. In order to support cavity filling and minimize nuisance trips during operation, cavity fill time delay and fault persistence are defined and set to each HPM. To support testing this, an RF signal (805 or 402.5MHz) is switched by the test stand to generate a fault condition. The fault is capable of having its width and location moved throughout the RF_GATE to test the fault detection logic.

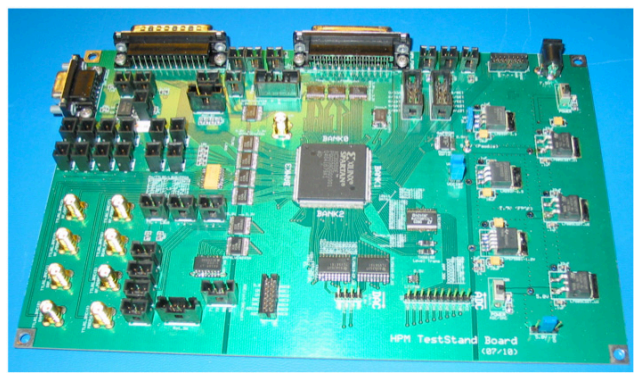

Figure 4: HPM test stand board (Xilinx Spartan 3E PQ208 FPGA) .

Figure 5: HPM test stand front panel and back panel (VXI) interface board.

Verification Procedures

Verification of the HPM requires two test procedures. The first procedure is the acceptance test procedure (ATP) using the HPM Test Stand Setup (Fig. 2). All functionality, communication tests and calibrations of the RF channels are done in this process. The second step is noise and isolation measurements among RF channels. Crosstalk, noise and linearity performances of the HPM are measured in this procedure with additional RF test equipment (Fig. 6).

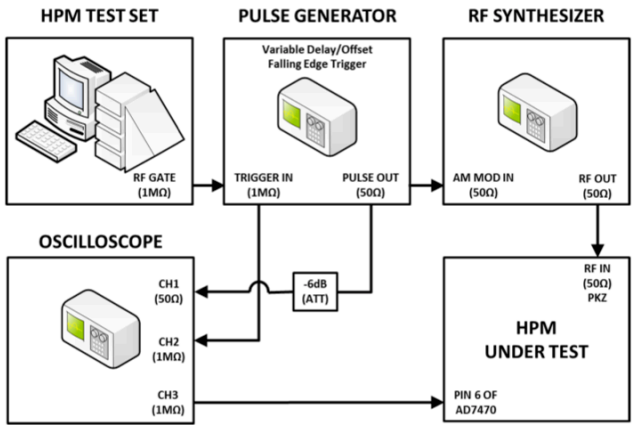

Figure 6: HPM noise isolation test stand setup.

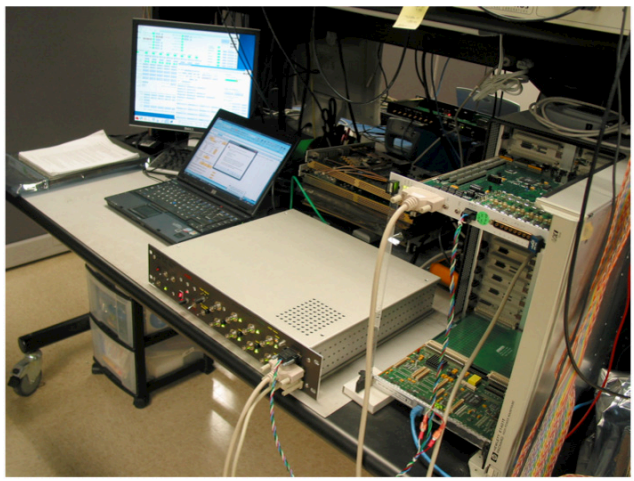
Figure 7: HPM test stand setup (HPM verification).

FURTHER IMPROVEMENTS AND DEVELOPMENTS

The previous test stand design had been implemented using discrete logic blocks and utilized for verification of the current HPMs installed in the SNS klystron gallery (96 units). Based on operational experiences, the HPM firmware has required updates and upgrades over the last few years. As the requirements change, the verification procedure needs to include more features and to cover additional operation scenarios. Flexibility and precision are required for the HPM Test Stand to prevent or minimize operational errors.

Some additional features are currently being considered to enhance the verification process to save time and increase precision of the measurements. The addition of a programmable switching pulse (variable width and location in and out of the RF_GATE) applied to the RF signals would be used for generating RF faults. The development of enhanced communication to allow for remote operation will support test stand automation. The test stand also provides 8 channels of slow 12 bit (~1MSPS) ADC channels for inputs and 2 channels of DAC outputs for future development.

CONCLUSION

The HPM Test Stand has been utilized for verification of the functionalities of the HPM modules. Over time, additional features and upgrades have been required to support accelerator operations. In order to support the testing of the upgrades, the HPM test stand has needed to be modernized. By replacing the discrete logic of the current test stand with programmable logic (FPGA) enables the convenient support for new HPM firmware updates/upgrades. Further development and upgrade of the HPM Test Stand Board is progressing with the goal of automation of verification procedures and more functionality in the future.

REFERENCES

[1] M. T. Crofford, et al, “Operational Experience with the Spallation Neutron Source High Power Protection Module,” PAC2005, Knoxville, TN, June 2005.
[2] H. Ma, et al, “Progress in RF controls at SNS,” LLRF Workshop, Knoxville, TN, October 2007.
[3] D. Thomson, “Operation and Maintenance Instruction, High Power Protection Module,” LANL/SNS internal document, 2004.