DEVELOPMENT OF INTEGRATOR CIRCUIT FOR CHARGE MONITORING

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Abstract

At the SPring-8 1-GeV linac, an electric charge of a pulsed electron beam is measured by an integrator circuit. A signal from a current transformer is processed into an integrated voltage. To improve the resolution for future use, a low-noise integrator circuit was developed whose main elements are a gate switch (SW-283-PIN, M/A-COM) and an accumulator (coaxial cable). The resolution is 0.65 pC under conditions of a range of 2 nC and a gate width of 20 ns. The resolution of the developed integrator circuit is 1/12 of the resolution of the present integrator circuit. The nonlinearity of the output voltage is small, 0.14 % rms compared to the output full scale.

INTRODUCTION

At the SPring-8 linac, eighteen current transformers (CTs) have been installed to observe macro longitudinal current structure or the electric charge of a pulsed electron beam by an oscilloscope. Beam charges are not recorded into the database except for two CTs; one is installed in the beam transfer line to the booster synchrotron, and the other is installed in the beam transfer line to the NewSubaru storage ring. These stored data are used to observe the beam charge and to calculate the injection efficiency to the booster synchrotron or the NewSubaru storage ring.

For top-up injection to the SPring-8 storage ring, about every 20 seconds the linac shoots an electron beam whose beam charge is about 1 nC. In the future the beam charge will be decreased due to more frequent beam injection to the storage ring. Presently Fast Gated Integrator and Boxcar Averager Modules (STANFORD RESEARCH SYSTEMS) are equipped as integrator circuits for signal processing. When the beam charge is decreased for the frequent beam injection, the resolution of the present integrator circuit will be worsened, too. To maintain or improve the resolution we developed a new integrator circuit to reduce the noise level to 1/10 of the present integrator circuit. The developed integrator circuits will be installed for all CTs in the linac instead of the present integrator circuits.

PRINCIPLE

The principle of the developed integrator circuit is identical as the principle of the present integrator circuit [1]. The principal elements are a gate switch and an accumulator. The gate switch determines the integration time of the measurement. When the gate is open, the signal voltage is led to an accumulator (1 and 2 in Fig. 1) that is a delay line with a characteristic impedance of 50 Ω. A coaxial cable or a pulse forming network (PFN) is used as an accumulator. The signal voltage led into the accumulator is reflected at the opposite open end and returned to the gate switch (3 in Fig. 1). If the gate is closed before the reflected signal voltage arrives, both ends of the accumulator become open ends, and then the signal voltage is stuck in the accumulator (4 in Fig. 1). The stuck signal voltage is averaged as it goes back and forward (5, 6, and 7 in Fig. 1). This averaged voltage is proportional to the integral of the signal voltage while the gate is open.

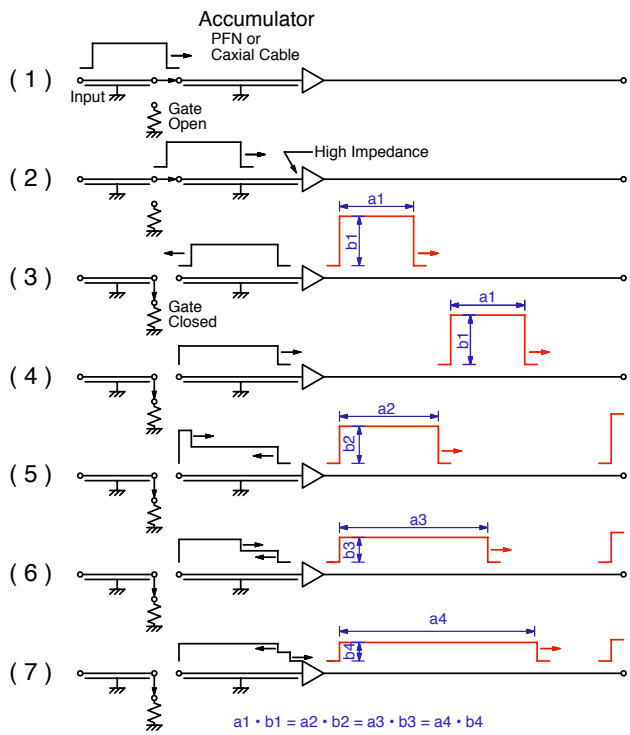

Figure 1: Principle of integrator circuit.

DESIGN

The block diagram and exterior of the developed integrator circuit are shown in Figs. 2 and 3. In Fig. 2 “a:” denotes the parameter for a short (1 ns) pulsed beam measurement,

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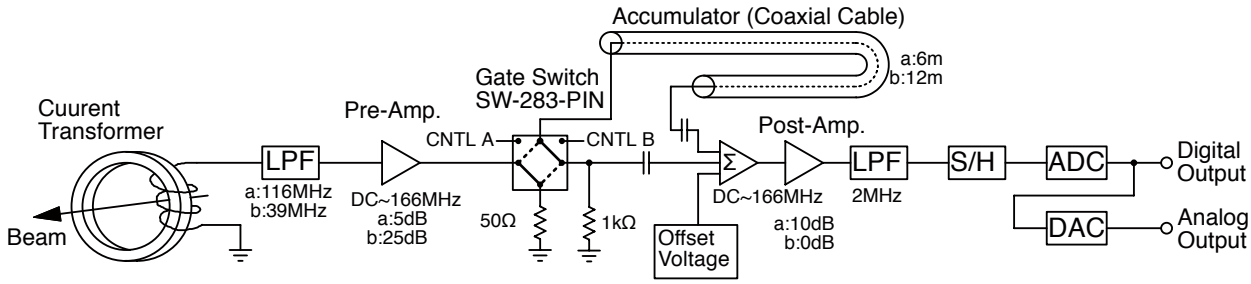

Figure 2: Block diagram of developed integrator circuit.

while "b:" denotes the parameter for a long (40 ns) pulsed beam measurement.

Two elements perform switching operations after receiving an external trigger: the gate switch and the sample-hold circuit in Fig. 2. The switching operation generates non-negligible fluctuation on its output voltage, and the typical amount of fluctuation is about 0.4 mV rms. Because this fluctuation dominantly affects the noise level of the output voltage of the integrator circuit, two amplifiers are installed to increase the input signal level to the switching elements: a pre-amplifier before the gate switch and a post-amplifier before the sample-hold circuit.

A low-pass filter, which is inserted between the CT and the pre-amplifier to avoid saturation of the pre-amplifier output, expands the pulse width and decreases the pulse height, but retains the time integral of the voltage.

The gate switch is a GaAs transfer switch SW-283-PIN (M/A-COM) (see Fig. 3). Its principal specifications are summarized in Table 1. A transfer switch was adopted to connect all ports with each other. If a port is not connected to another port, large switching noise appears in the port. The pre-amplifier becomes especially unstable due to this noise.

The SW-283-PIN has four ports and two control voltage inputs. The control voltages (denoted as CNTL A and CNTL B in Fig. 2) are complementary voltages that are inverted when the state of connection is switched. When the gate is open the ports of the pre-amplifier and the accumulator, and the ports of the 50 Ω and the 1 kΩ are connected. When the gate is closed the ports of the pre-amplifier and the 50 Ω, and the ports of the accumulator and the 1 kΩ are connected. The control voltages are -0.1 and -7.9 V, which are close to the limitation of the specified control voltage range.

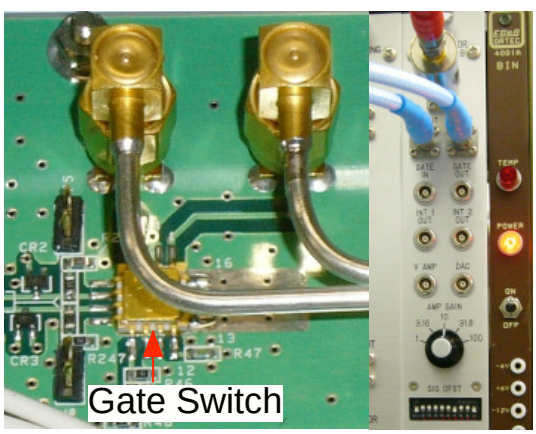

Figure 3: Gate switch on a base plate (left) and an exterior of developed integrator circuit (right).

Table 1: Principal Specifications of SW-283-PIN

Bandwidth [GHz]		DC ∼ 3
Isolation [dB]	DC ∼ 0.5 GHz	45
Rise/Fall time [ns]	10 - 90%	2
1dB Compression [dBm]	0.05 GHz	+26
Video Feedthru [mV]		30
Control Voltages (Max) [V]	Low, High	0, -8

The rise time of the gate switch is determined by the root sum square of the rise times of the SW-283-PIN and the control voltage. To avoid lengthening the rise time of the gate switch a fast circuit was developed to generate control voltages for the SW-283-PIN. The block diagram of the circuit is shown in Fig. 4. There are four fast transistor switches that consist of a bridge circuit and two kinds of DC voltages: +2 and -10 V. The control voltages are inverted instantaneously by the external gate pulse. The range of the control voltages is restrained between -0.1 and -7.9 V by clipping diodes. The merits for using clipping diodes include accuracy, stabilization , and the fast rise time of the pulsed control voltages.

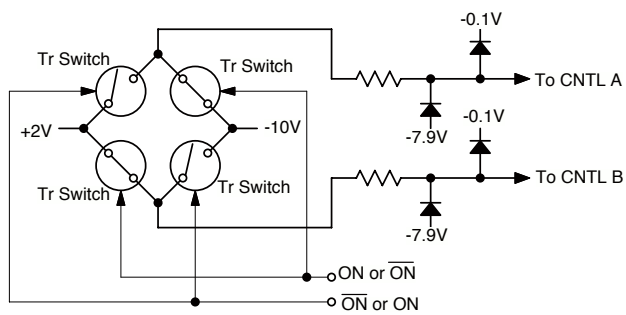

Figure 4: Block diagram of the circuit to generate control voltages for SW-283-PIN.

PERFORMANCE

The following examination was carried out to evaluate the rise time of the gate switch. Pulsed voltages that passed through the gate switch were measured by an oscilloscope. Figure 5 is superimposed drawings of 61 waveforms. The initial pulse width and height were 1 ns and -1 V, and the pulses were successively delayed at 0.5 ns intervals. The measured pulse height is smaller than the initial pulse height because attenuation was caused by the internal resistance of the SW-283-PIN. The width of the superimposed waveforms expresses the width of the external gate pulse. Before and after the shape of the gate pulse, pulsed voltages don't appear, meaning that the pulsed voltage cannot completely pass through the gate switch when the gate is closed. The rise time is measured as 2 ns (10 → 90 %), 4 ns (10 → 95 %), or 8 ns (10 → 98 %), and these values are comparable to the SW-283-PIN specifications.

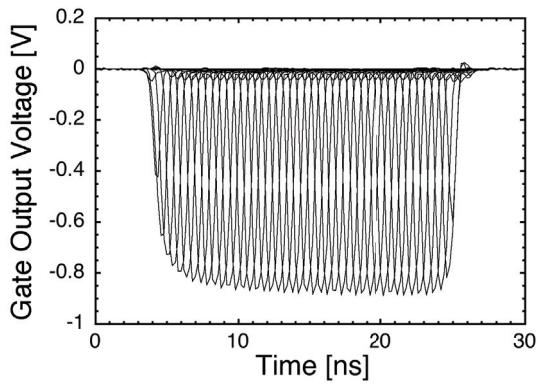

Figure 5: Superimposed 61 waveforms after passing gate switch.

When the gate is closed the accumulator is connected to the 1 kΩ termination and discharges with a time constant of $\sim 1\mu$ s. At this time the voltages that appear at both ends of the accumulator are summed by a summing amplifier. In Fig. 6 the red and blue lines express voltages that appear at the ends of the accumulator, and their pulsed voltages appear alternately. The height and width of the pulsed voltages decrease and widen as time elapses, until finally the voltages are averaged. The waveform of the 2 MHz LPF output is expressed as the green line, and the timing for the sample-hold is set around 700 ns in the figure.

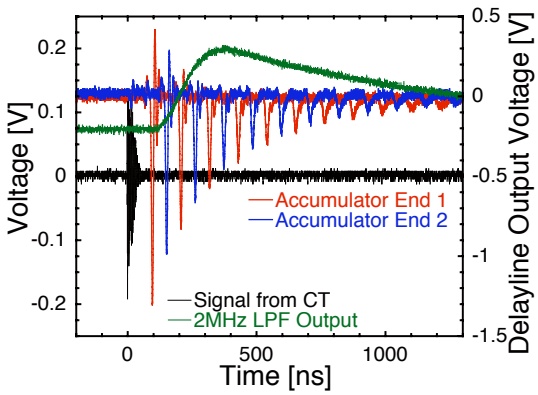

Figure 6: Voltages that appear at both ends of accumulator.

Resolution was measured as the standard deviation of the output voltage when the signal input is kept to 0 V (50 Ω termination). The resolution of the developed integrator circuit was measured as 0.65 pC under conditions of a range of 2 nC and a gate width of 20 ns, and the resolution of the present integrator circuit was measured as 2.9 pC under conditions of a range of 1.4 nC and a gate width of 10 ns. Because the resolution is proportional to the range and the gate width, the resolution of the developed integrator circuit has been significantly improved to 1/12 of the resolution of the present integrator circuit with the same range and gate width conditions.

The linearity of the output voltage to the time integral of the input voltage was measured with a gate width condition of 20 ns (Fig. 7). The output voltage shows good linearity, and its deviation 0.14 % rms, which is small compared to the output full scale (10 V).

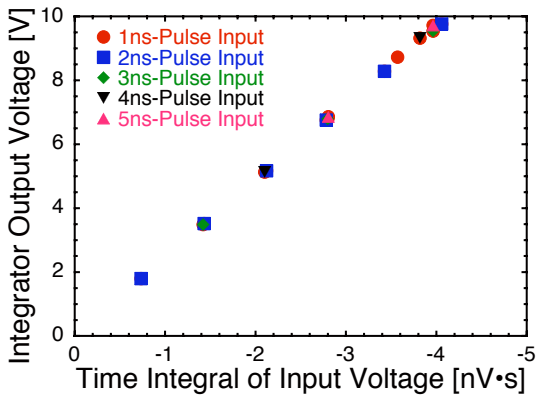

Figure 7: Output voltage to time integral of input voltage.

SUMMARY

We developed an integrator circuit for the charge monitoring of the SPring-8 linac to improve resolution for future use. The main elements of the developed integrator are a gate switch and an accumulator. The rise time of the gate switch is 2 ns (10 - 90 %); this value is fast and comparable to the SW-283-PIN specifications. The resolution is 0.65 pC under conditions of a range of 2 nC and a gate width of 20 ns. This resolution is 1/12 compared to the resolution of the present integrator circuit with the same conditions. The nonlinearity of the output voltage is small, 0.14 % rms compared to the output full scale (10 V).

REFERENCES

[1] Manual of Fast Gated Integrators and Boxcar Averagers, SANFORD RESEARCH SYSTEM S.