

A KICKER DRIVER EXPLOITING DRIFT STEP RECOVERY DIODES FOR THE INTERNATIONAL LINEAR COLLIDER

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Abstract

Diversified Technologies, Inc. (DTI), under a SBIR grant from the U.S. Department of Energy¹, is developing a driver for a kicker TEM strip-line deflector which inserts and extracts charge bunches to and from the electron and positron damping rings of the International Linear Collider. The ultimate ILC damping ring kicker driver must drive a 50 Ohm load (a 50 Ohm terminated TEM deflector blade) at 10 kV, with 2 ns flat-topped pulses at a 3 MHz rate, within one-millisecond bursts occurring at a 5 Hz rate. The driver must also effectively absorb high-order mode signals emerging from the deflector itself.

In this paper, DTI describes the design of the kicker driver involving high voltage DSRDs (Drift Step Recovery Diodes) and high voltage MOSFETs. The development system will produce 5 kV pulses, which otherwise will satisfy the ILC requirements, as a precursor to the full 10 kV system. Because of the high 3-MHz pulse rate required, this design employs an all-electronic, rather than magnetic, approach to pulse compression.

BACKGROUND

Every particle accelerator requires “kickers” – electromagnetic deflectors that pulse on to divert (kick) bunches of particles out of their trajectory onto new beam paths, targets, detectors, or other instrumentation. Kickers must reach the intended deflection field between particle bunches, control that field for a finite time, and return to zero field to avoid affecting the next bunch. The drivers for these kicker deflectors, therefore, must be capable of providing the required current pulses into the kicker impedance at demanding rates.

This effort is focused on the use of very fast Drift Step Recovery Diodes (DSRDs), driven by a MOSFET pulser, to obtain bursts of identical energetic pulses at a 3-MHz pulse rate - well beyond that attainable by magnetic pulse compression.

The pulse rate must be 3 MHz for a burst duration of one millisecond, with a bursts repetition rate of 5 Hertz (i.e. the average PRF is 15,000 Hertz). The essential objective of the project is to develop highly repetitive, high-voltage, 2 ns pulses for deflecting packets of electrons and positrons from their respective damping rings (6 km circumference rings) into the 40-km long ILC

linear collider, and for nearly simultaneous replenishing of the packets of charge in the damping rings. An increment of deflection will be imparted by a symmetric pair of shaped parallel deflection blades of 30-cm length, pulsed in opposition at 10 kV each for two nanoseconds.

(Ten stages of such deflection will be necessary to produce the overall “kick” required.) Within each guide comprised of the two 30-cm deflector blades and their environment, each TEM wave produced by the two pulse generators traverses from the entrance to the terminus of the guide. Matching 50-Ohm resistors terminate the deflector blades, to avoid creation of secondary traveling waves.

OVERVIEW OF THE APPROACH

The project itself is structured to achieve three critical milestones, (1) development of fabrication of DSRD diode stacks by an established semiconductor device manufacturer (in particular Voltage Multiplier Inc of Vaisala CA), (2) development of instrumentation and methods for characterizing the deflection pulses with sufficient accuracy, and (3) development of a reliable and jitter-free source for producing 40-to-50 nanosecond “pump” pulses at the rate of 3 MHz. These are compressed to 2 nanosecond pulses by the DSRD and one-nanosecond delay line - see Figure 2.

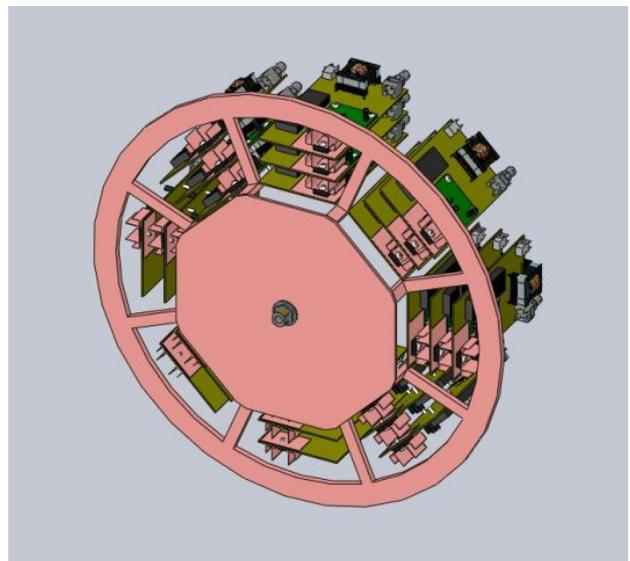


Figure 1: Basic configuration of ILC damping ring pulse generator. Unified 3MHz power/ pulse-synchronization supply and fiber-optic coupled controller are not shown. The one nanosecond delay line emerges from center of plate.

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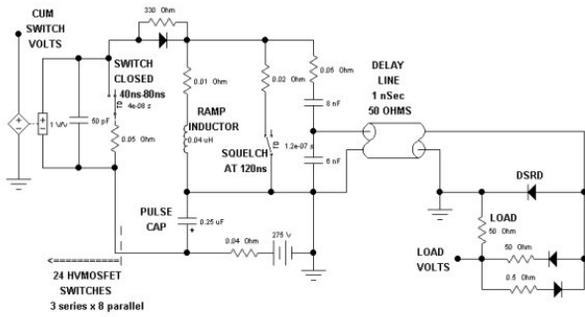


Figure 2: Schematic design of kicker driver, DSRD and load at right.

Various system designs were explored for producing desired pulse wave forms by exploiting the extremely abrupt opening of DSRD switches. The favored embodiment of the overall pulse generator, illustrated in Figure 1, is based on measurements, circuit modeling and practical considerations regarding component performance in the sub-nanosecond regime. The original design, first described at PAC07, has been changed substantially to adequately address the demanding constraint on pulse-to-pulse variation. Furthermore, the physical configuration has been revised to take advantage of symmetries. In this case an eight-fold symmetry is exploited, as shown in Figure 1. Each of the octal sections is comprised of three MOSFET switch cards arranged in series.

The overall pulse generation and compression network is presented in Figure 2. This represents the principal schema, with variants on this approach readily possible. The key components are exhibited in this figure including:

- A high voltage MOSFET switch array capable of delivering 25 ns, 400 A, 1 kV pulses at 3 MHz in one millisecond bursts, at a burst rate of 5 Hz; this switch array having a withstand capability of 4 kV or more.
- A DSRD diode stack initially capable of exhibiting 5 kV upon opening (but capable of 10 kV), able to open within 500 picoseconds, and interrupt 400 A reverse current.
- A one-nanosecond 50 Ohm delay line, together with an input circuit that presents a near-electrical-short to the line for frequencies greater than 10 MHz.

The presence of the delay line is essential. Its inductance ensures the input current pulse is maintained at the DSRD for a full two nanoseconds with little sag, and its high-frequency shorted input is expressed at the DSRD (and load) only after a round-trip of two nanoseconds, abruptly terminating the output pulse. Because this feed delay line is in parallel with the 50 Ohm load (actually a transmission line, terminated by the 50 Ohm TEM deflector) the DSRD stack must interrupt 400 A to produce 10 kV pulses.

The operation of the overall network shown in Figure 2 starts when the pump circuit to the left applies 780 V to the 25 nH transfer inductor for 25 ns. During and immediately after this brief pumping interval, a moderate forward current is established in the DSRD stack at the right, establishing narrow, highly concentrated minority carrier populations on both sides of the physical PN junctions within the DSRD diode stack. When the pump switch (the HV MOSFET array) opens, a large portion of the current that has been established in the transfer inductor must be suddenly drawn *from* the 1-nanosecond delay line, reversing the current in the conducting DSRD which, by design, opens extremely abruptly after a few nanoseconds delay (i.e. after the plasmas on both sides of the PN junctions collapse). The opening of the DSRD switch causes the reverse current of 400 A to redirect, splitting it equally between the 50 Ohm load and a reflection back into the 50 Ohm source line (i.e. the 1 ns delay line). This condition persists only for the 2 ns round-trip in the delay line, after which the pumping source appears to the DSRD - and the load in parallel with

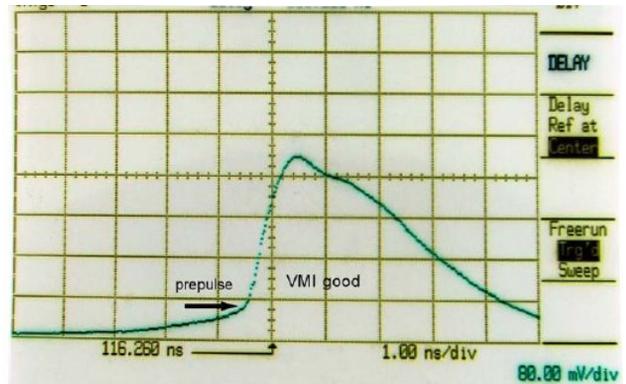


Figure 3: Reverse voltage pulse of VMI fabricated DSRD diode. Forward pumping is 100 nanoseconds in duration. Avalanche occurs above 550V. Time-axis: one-nanosecond per division.

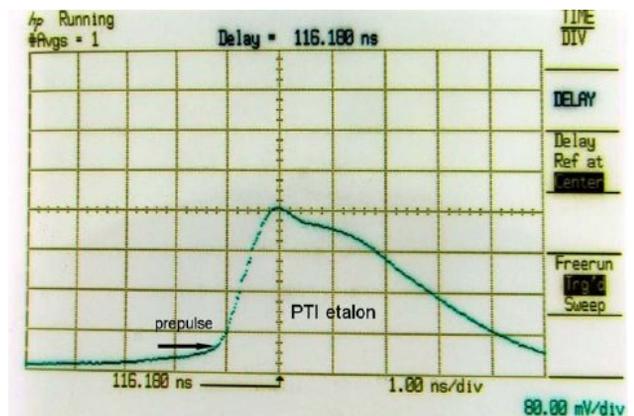


Figure 4: Reverse voltage pulse of Ioffe Physics Institute's PTI etalon DSRD diode. Forward pumping is 100 nanoseconds in duration. Avalanche occurs at 500V. Time-axis: one nanosecond per division.

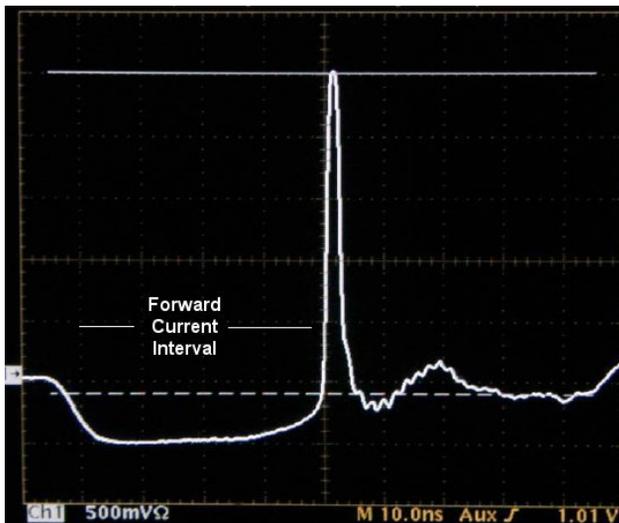


Figure 5: Pump and step recovery switching performance of DSRD stack provided by Ioffe Institute of Physics, compliments of Professor Alexei Kardo-Sysoev. Time axis 10ns/division. Peak voltage 1000V; one-nanosecond delay line employed.

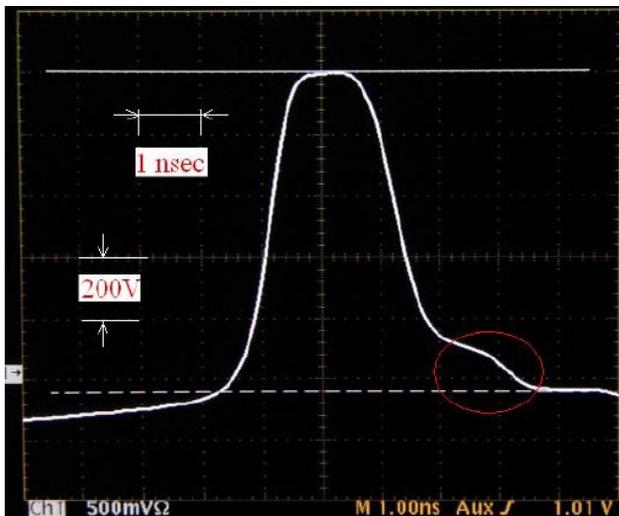


Figure 6: Step recovery switching performance of DSRD stack, time axis; one-nanosecond per division.

it - as a short circuit, which terminates the 2 ns pulse impressed on the load. Delivery of a 10 kV pulse to the load requires that the MOSFET switch array must withstand a voltage of 3.5 kV upon opening.

Fabrication of DSRD diodes at VMI has been accomplished, and these DSRD diodes have been assembled into stacks and successfully tested at Ioffe Institute of Physics in St. Petersburg Russia. Professor Alexei Kardo-Sysoev of this institute has been instrumental in developing the silicon processing at VMI and in the build and testing of the resulting DSRD modules. VMI has proven high-volume technology for producing passivated high-voltage diode stacks, and will soon be producing these from its DSRD diodes as well. Figure 3 and Figure 4 compare of the pulse properties of

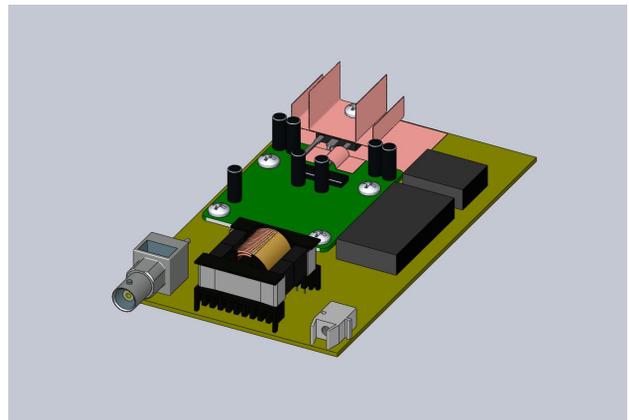


Figure 7: Illustration of individual MOSFET switching card. The pump system will employ eight parallel ranks of three (or four) of these in series. The series arrangement is required to withstand 2.5 kV opening voltage.

the VMI produced DSRD diodes with the “PTI etalon” DSRD diodes of Ioffe Physics Institute.

Development of instrumentation and methods for characterizing DSRD modules is underway. Dr. Anatoly Krasnykh, coauthor, has been employing a DSRD module provided by Ioffe Physics Institute to prove these capabilities. Figure 5 shows a complete pump and blocking cycle for this device with a 50-Ohm parallel load, and pumped via a one-nanosecond long delay line as shown in principle in Figure 2. Figure 6 shows the principal pulse in higher resolution.

The design of the pump circuitry has been revised substantially. Modeling indicated that extraordinary measures would be required to adequately prevent AC ripple from influencing pulse repeatability within the 1-millisecond bursts. Rather than employing brute force filtering techniques to accomplish this, we have chosen to adopt 3-MHz RF as means of powering the switching logic and gate drivers for the MOSFET switches. Optical fiber will only carry the signals delineating the bursts, but will not affect pulse timing. Each switch card in each series stack of three will be isolated from its neighbors by common mode chokes, which carry the 3-MHz power and synchronizing waveforms. Testing of a breadboard version of the MOSFET switching card, illustrated in Figure 7, is underway. It employs a 800V HV MOSFET as the principal switching component.

SUMMARY

Development of a fully capable DSRD kicker driving is successfully proceeding, with excellent results obtained from our first commercially produced DSRDs, and a refined circuit for the MOSFET driver. In the next year, the DSRDs will be produced in diode stacks, and combined with the MOSFET driver to demonstrate the full pulse operation required by the ILC.