DIGITALLY CONTROLLED HIGH AVAILABILITY POWER SUPPLY

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Abstract

This paper reports the design and test results on novel topology, high-efficiency, and low operating temperature, 1,320-watt power modules for high availability power supplies. The modules permit parallel operation for N+1 redundancy with hot swap capability. An embedded DSP provides intelligent start-up and shutdown, output regulation, general control and fault detection. PWM modules in the DSP drive the FET switches at 20 to 100 kHz. The DSP also ensures current sharing between modules, synchronized switching, and soft start up for hot swapping. The module voltage and current have dedicated ADCs (>200 kS/sec) to provide pulse-by-pulse output control. A Dual CAN bus interface provides for low cost redundant control paths. Over-rated module components provide high reliability and high efficiency at full load. Low on-resistance FETs replace conventional diodes in the buck regulator. Saturable inductors limit the FET reverse diode current during switching. The modules operate in a two-quadrant mode, allowing bipolar output from complimentary module groups. Controllable, low resistance FETs at the input and output provide fault isolation and allow module hot swapping.

OVERVIEW

The next linear collider will require several thousand magnet power supplies. This is a far greater number then any linear accelerator has used to date. To achieve equivalent or better availability of the beam will require improved availability of all systems. Significant increases in availability can come from improved reliability of modules, but an order of magnitude improvement can only come from redundant modules.

Power supplies will consist of parallel power modules in a N+1 redundant arrangement. Individual modules can fail without causing the power supply to lose regulation of the magnet current. Individual modules must provide for fault isolation to allow the power supply to operate with a failed module. The isolation will also allow for hot swapping of modules.

The individual modules will be autonomous so that there is no single point of failure. A digital controller will provide module control and fault detection. The controller provides a dual CAN bus interface for redundant power supply control.

POWER MODULE

The power supply architecture is based on shared central bulk AC-DC power supplies with redundant buck regulators for each load. The power supplies are assumed to be in the 5 to 50 kW range consisting of redundant 1 to 10 kW modules. The modules will provide a voltage regulated output set by CAN bus broadcast messages from redundant magnet current regulators. The modules will use buck regulators with FETs in place of free wheeling diodes. This provides lower conduction losses and eliminates the non-linear discontinuous conduction region at low current. The two quadrant operation allows two power supplies operating with complimentary outputs to drive bipolar loads.
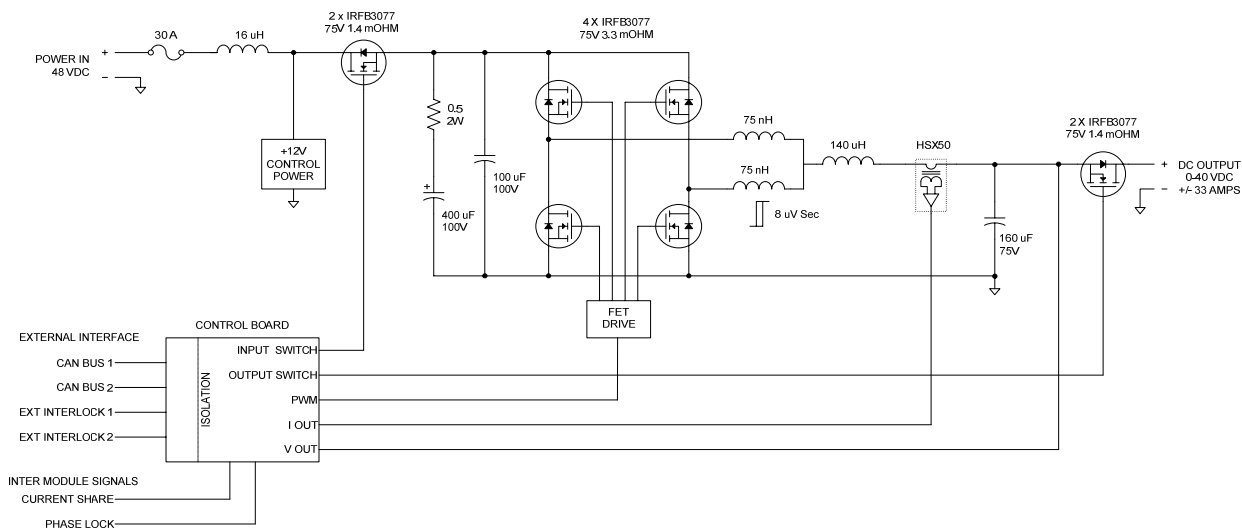

Figure 1: Two quadrant DC-DC converter with input and output FET switches.

Each module has FETs on the input and output. These allow failed modules to be isolated from the power source and load, and also allow modules to be replaced (hot swap) while the power supply is operating. Since the FETs ON resistance has a positive temperature coefficient, they can be easily paralleled to lower the conduction losses.

Ideally the upper and lower switching FETS would be driven synchronously, one turning on exactly as the other is turning off. This technology exists for low power (<100 watts) devices, but not for the high power devices. If the FETs are switched at the same time, there is a period where both are conducting (shoot through). This current is wasted as heat in the FETs. The existing FET drivers do not control the propagation delays and rise times to the extent needed for synchronous switching.

Adding a delay between turn ON and turn OFF eliminates shoot through losses, but adds losses from the FET body diode. When a FET with reverse current flowing is turned off, the current is shunted to the FET body diode. The diode has a large reverse recovery charge that increases with current and temperature.

Four FET Buck Regulator

The buck regulator topology chosen uses 4 FETs instead of the usual 2. This allows for two small saturable ferrite chokes to be included. These provide a 100 nanosecond delay to allow the FET diodes conducting reverse current to recover before seeing the full bulk voltage. This greatly reduces the reverse current and switching losses in the FETs, and reduces the snubber circuit requirements.

The power supply controller sets the FET turn on sequence according to the polarity of the output current. For positive output current, the bottom two FETs will be carrying current in the reverse direction. When a bottom FET turns off, the opposite side upper FET turns on. When a top FET turns off, the bottom FET on the same side turns on. For negative output current, the top two FETs will be carrying current in the reverse direction. When a top FET turns off, the opposite side bottom FET turns on. When a bottom FET turns off, the top FET on the same side turns on. The module controller senses the polarity of the output current with a hall effect current sensor in series with the output inductor.

Digital Module Controller

A major goal of this project is to design a power module control board that can be used with a power supplies with a large range different outputs. This will provide a common interface for most of the power supplies needed for the NLC.

The power module controller for redundant modules has to address the following requirements;

- Stability: Operate in a stable manner in parallel with other modules under all possible load conditions.
- Load Sharing: The output current of each module should be within 10% of other modules.

- Failure Detection: The controller needs to be able to sense and report a module that is not operating properly.
- Soft Start: The controller needs to be able to smoothly turn on and off a single module in a power supply without disturbing the power supply output.
- Autonomous Operation: The controller needs to be independent of all other module controllers to eliminate any single point failures.
- Redundant Communications: The controller will support dual CAN bus interfaces for redundant control.
- Module Synchronization: Each controller will provide a delay lock loop to lock the switching frequency and phase to the other modules.
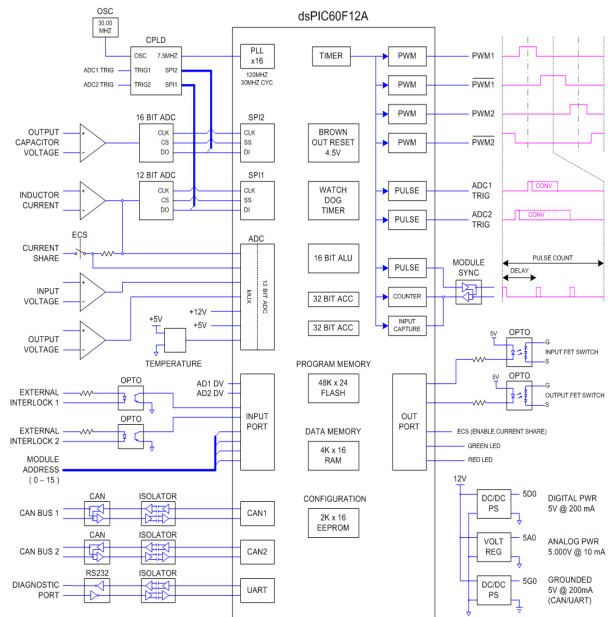

Figure 2: Power module controller block diagram.

Module Controller

The processor used for the project is a Microchip dsPIC60F12A. It offers a high performance processor with a large array of external interfaces in a small inexpensive package. The processor executes 30 MIPs, or 300 instructions per cycle for a 100 kHz switching rate. It has a Harvard architecture with a 24 bit instruction path, and 16 bit data paths. It has two 40 bit accumulators with automatic limiting (saturation) of results. This eliminates range checking of results in the PID algorithms. The external interfaces include a dual CAN bus, UART, 8 PWM outputs, 2 SPI interfaces, and a 12 bit ADC with 16 input channels.

The maximum switching frequency for the design is 100 kHz (10 μs period), but may be programmed to be as low as 20 kHz. Two external serial ADCs are used to allowing reading the output voltage and output current on each cycle. A 16 bit ADC is used for the output voltage, and a 12 bit ADC for the output current. The noise from the hall effect current transducer limits the current

resolution to less about 10 bits. The analog input to the ADCs is allows for under and over range conditions. All zero's or one's from an ADC is considered as a hardware fault.

The controller is referenced to the negative output of the power module. The CAN bus interfaces and diagnostic UART use digital isolators to provide a ground referenced control interface.
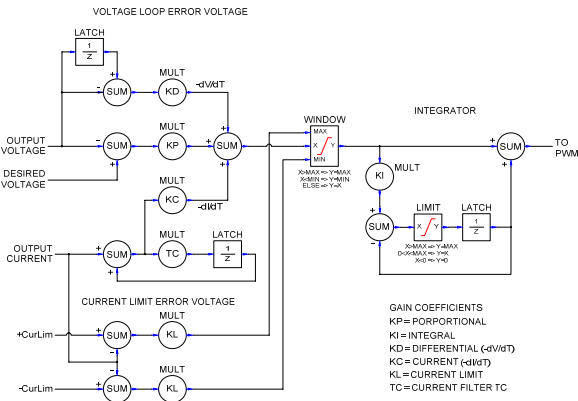

Figure 3: Control algorithm.

Controller Algorithm

The controller uses a modified PID algorithm. The Proportional and Derivative terms are combined to form an error signal. The error signal is integrated to generate the Integral term. The error signal and integral are summed to generate the PWM on time.

The current limit operates as a window function for the error signal. The controller determines the minimum and maximum error signals that will keep the output current in range. The voltage and current loops share the same integral term to allow glitchless switching between voltage control and current limit.

The controller uses two derivative terms; dV/dT and dI/dT. The main function of the derivative term is to damp the response of the output LC filter. Using two derivatives allows better response for all possible load conditions.

The PWM outputs of the dsPIC processor have a 33 ns resolution. The input to the PWM algorithm is a 12 bit integer. The actual resolution of the PWM ranges from 8 to 10 bits, depending on the frequency. The input signal is truncated before being applied to the PWM, with the remainder from the truncation being applied to future cycles. This extends the resolution of the ADC, but adds some small lower frequency harmonics to the output.

The PWM algorithm allows setting minimum and maximum duty cycles. When a value less then the minimum is requested, the PWM maintains the minimum pulse width, but skips cycles to maintain the average value equal to the requested value. The on time remains constant, but the frequency changes to provide the correct average value.
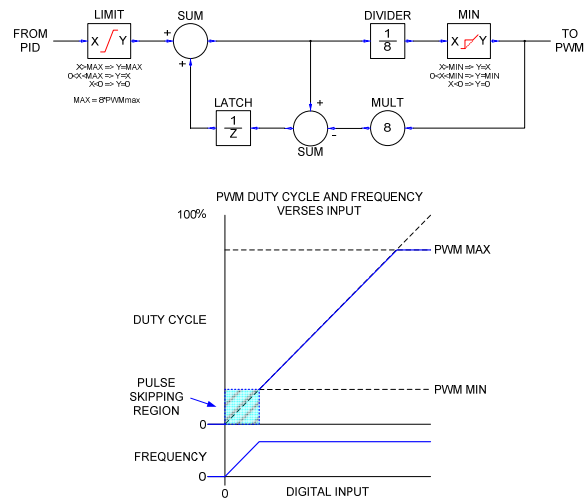

Figure 4: PWM algorithm.

TEST RESULTS

To date, 5 test power modules have been built. They have been tested with using Microchip development boards that use the internal 12 bit ADC. The losses in the module were less then 22 watts for a 33 amp output. This puts the full load efficiency of the power section at better then 98%. The unit requires 3 watts of control power, and another 3 watts for the input and output FET switches. The complete module full load efficiency should be better then 97%. More then half of the losses are due to the resistance of the inductors, PCB traces, and FETs. The FET switching losses are a minor contribution.

The circuit design and PCB layout of the controller has been completed. When the controllers are built, they will allow testing of the parallel and redundant operation of the power modules.

CONCLUSION

Power supplies with high efficiency and reliability that support redundant operation are technically strait forward. There are additional costs involved with additional hardware for redundant operation, and over sizing of components to improve efficiency and reliability.

Redundant power supplies are becoming available for high availability computer systems, but these fixed output voltage and low power make them inappropriate for powering magnets. There is currently not adequate demand for redundant 1 to 100 kW power supplies to have commercial sources available.

This project will continue to develop the power supply controller to demonstrate a power supply made from redundant modules. This will provide a better understanding of the issues involved in providing ultra reliable power supplies for the next linear collider.