

LLRF CONTROL SYSTEM USING A COMMERCIAL BOARD*

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Abstract

The requirements for the field amplitude and phase stability of the PEFP linac are 1% and 1 degree, respectively. To achieve the requirements, a digital LLRF control system has been developed using a commercial digital board for general purpose (FPGA). The feedback with PI control and feedforward are implemented in the FPGA. The LLRF control systems are currently used for the linac test. In this paper, test results and discussion on the advantage and disadvantage of the LLRF system based on a commercial board are presented.

INTRODUCTION

In the 100 MeV proton linear accelerator for PEFP (Proton Engineering Frontier Project), the RF source will power an RFQ cavity and DTL tanks operated at a frequency of 350 MHz [1]. The low level RF(LLRF) system for 100 MeV proton linear accelerator provides field control including an RFQ and DTL tanks at 350 MHz. In our system, an accelerating field stability of $\pm 1\%$ in amplitude and ± 1 deg. in phase is required for the RF system. The digital RF feedback control system using the FPGAs and PowerPC Embedded Processor is adopted in order to accomplish these requirements and flexibility of the feedback and feed-forward algorithm [2]. The analog front-end also developed which contains the IQ modulator, RF mixer, attenuators etc. To check the performance of the digital feedback control system, low power test with a dummy cavity has been performed with an intentional perturbation and has shown that the feedback system rejected the perturbation as expected. High power RF test with 3 MeV RFQ and 20 MeV DTL has been performed and the accelerating field profiles were measured and the pulse-to-pulse stability was checked by pulse operation with 0.1 Hz repetition rate. In addition, the LLRF system can be used for resonant frequency observer. Measured frequency offset from resonance condition is converted to analog voltage signal, which can be used as an error input signal for RCCS (Resonance Control Cooling System).

LLRF SYSTEM DESCRIPTIONS

The main hardware components of the digital RF feedback system are ADC for sampling of the RF signal, FPGA for the signal processing and DAC for driving the IQ modulator. A ICS-572B commercial board which is shown in figure 1 is adopted for the ADC/DAC and FPGA board. ICS-572B is a PMC module with 2-channel 105 MHz ADC, 2-channel 200 MHz DAC and with 4 million gate onboard Xilinx FPGA.

The board uses two 14-bit ADCs (Analog Devices AD6645) with a maximum sampling rate of 105 MHz. The sampling clock can be either internally or externally generated. The minimum ADC sample rate is 30 MHz. Both input channels are simultaneously sampled and transformer-coupled with turn ratio of 4:1.

The outputs of the ADCs are connected to a Xilinx FPGA for direct processing of the ADC data. The ICS-572B includes a Xilinx Virtex-II FPGA (XC2V4000) that can be programmed by the user via a JTAG port or PCI communication.

On the output side, the ICS-572B uses two 14-bit high speed DACs (Analog Devices AD9857). The maximum simultaneous conversion rate is 200 MHz. The DAC has a built-in quadrature up-converter that allows the user to provide complex baseband input which is up-converted to a programmable IF (up to 100 MHz). The DAC also provides a programmable clock multiplier.

The communication between the ICS-572B board and host system is made using PCI bus. The QL5064 QuickPCI chip from QuickLogic is used for PCI interface solution. The performance of the QL5064 is 64 bit/66 MHz and automatically backwards compatible to 33 MHz or 32 bit

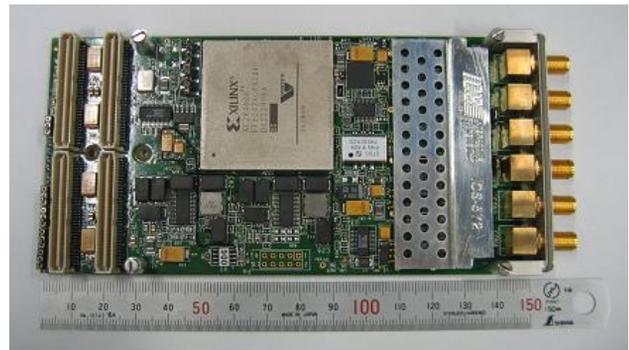


Figure 1: ICS-572B PMC Board.

For the host system of the ICS-572B FPGA board, a Motorola VME processor module, MVME5100, is adopted. The main roles of the host system are the configuration of the FPGA board and the data acquisition.

The feedback logic based on the PI control is implemented in the FPGA by using VHDL. The I and Q component of the cavity field signal is fed into the FPGA using the ADC, which samples the RF signal four times during one period. The sampled I and Q components of the cavity signals are compared with the set value, which generates the error signal. The calculated proportional and integral control values are added then converted to an analogue signal by using DAC.

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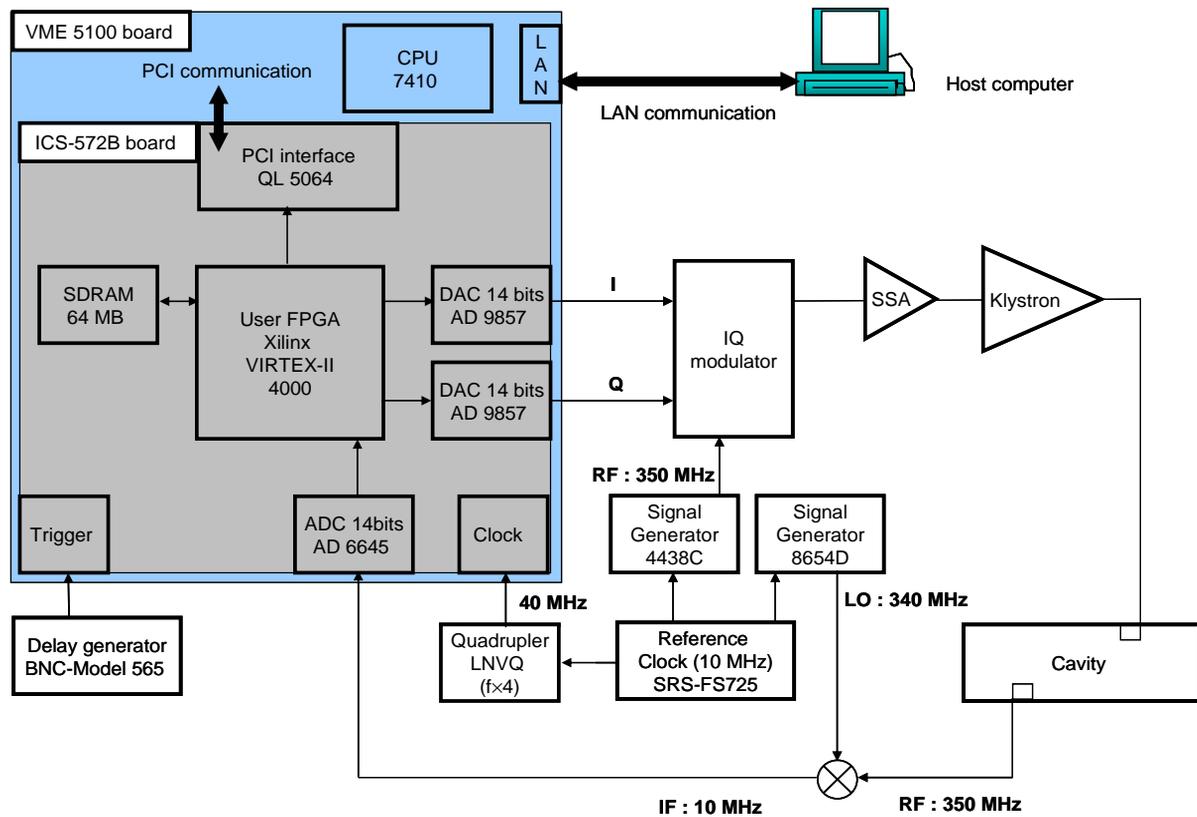


Figure 2: Schematic of the overall control system and experimental set-up.

The analogue signal from the DAC drives the IQ modulator. The set values and each gain value are written into the register in the FPGA by the host processor through a PCI communication. Therefore the set values and gains can be changed during the operation. The measured I and Q components of the RF signals are uploaded to the host board by using a PCI communication.

We performed a test for monitoring the frequency offset from the resonance by using the developed LLRF system and dummy cavity. Figure 5 shows the measured results for frequency offset as a function of the dummy cavity temperature. We analyzed the results by linear fitting. The error bars represent the maximum and minimum values at given temperature.

PERFORMANCE TEST RESULTS

The schematic block diagram for the overall LLRF control system is shown in figure 2. The shot-to-shot RF stability was measured and we found that the feedback control improved the shot-to-shot stability by an order of a magnitude compared with an open loop control [3].

For the high power RF test, the RF system was operated in pulse mode with 200 μ s duration and 0.1 Hz. The measured RF amplitude variation and phase variation during a single RF pulse without beam were less than 0.2% and 0.3°, respectively as shown in figure 3. The RF amplitude and phase of DTL cavity for 600 shots are recorded and the results are summarized in Table 1. For 600 shots, the RF amplitude and phase were kept within $\pm 0.7\%$ and $\pm 0.9^\circ$ respectively, which meet the RF requirements of the LLRF control system.

For the feedback and feed-forward test, we established the experimental setup by using a dummy cavity. As can be seen in figure 4, the PI control has shown a good performance in perturbation rejection. In addition, the feedback control with feed-forward could improve the transient response significantly.

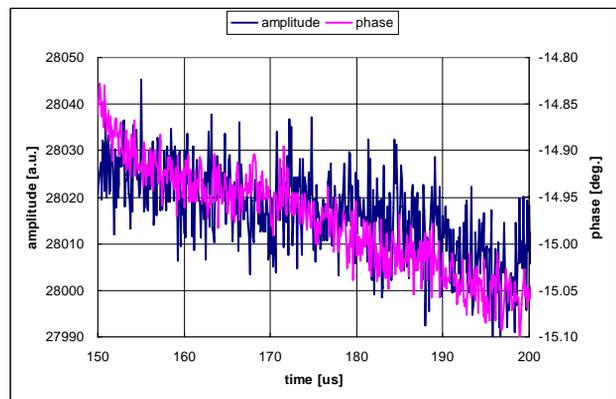


Figure 3: RF amplitude and phase in DTL cavity.

Table 1: Statistics for 600 shots measurements results.

	amplitude	phase [deg.]
average	28139.1	-14.109
sigma	121.2	0.323
max error	0.79%	0.904
min error	-0.63%	-0.744

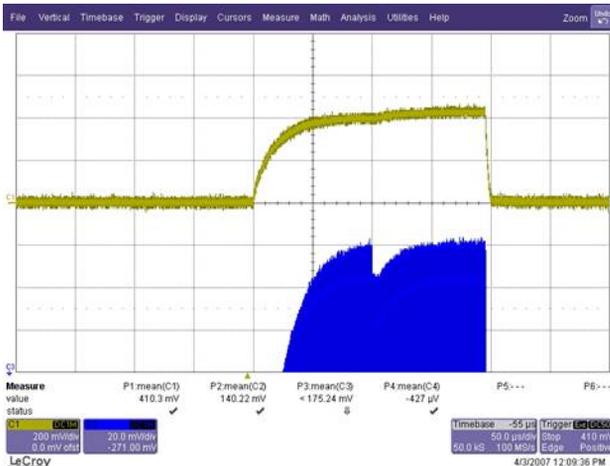


Figure 4(a): Cavity field response for feedback control. (upper: Forward RF power, lower: Cavity field)

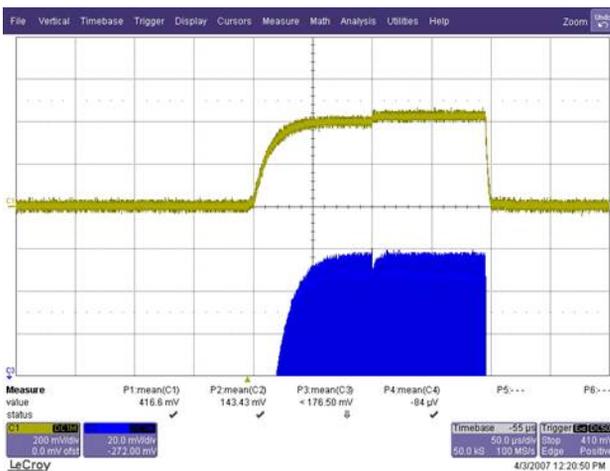


Figure 4(b): Feedback control with Feed-forward. (upper: Forward RF power, lower: Cavity field)

One of reasons for large scatter in measured data by network analyzer is that the dummy cavity has a low quality factor. In addition, the fluctuation in temperature measurement system is another reason for data scatter shown in figure 5. The frequency offsets measured by network analyzer and by LLRF were slightly different by about 6 kHz, which is about 3 % of bandwidth of the dummy cavity. This discrepancy is still under investigation. However, the gradients are almost same, which means that the frequency sensitivity to the temperature measured by using LLRF system is reliable.

The measured frequency offset is converted to analog voltage signal through the DAC in the multi-functional IO board mounted on the VME host board, which will be used for the error signal input for RCCS. The DAC was programmed to have output ranging from -10 V to +10 V for frequency offset from -20 kHz to +20 kHz. The DAC output behaved as expected as shown in figure 6, which shows the recorded DAC output during the frequency offset measurement experiment.

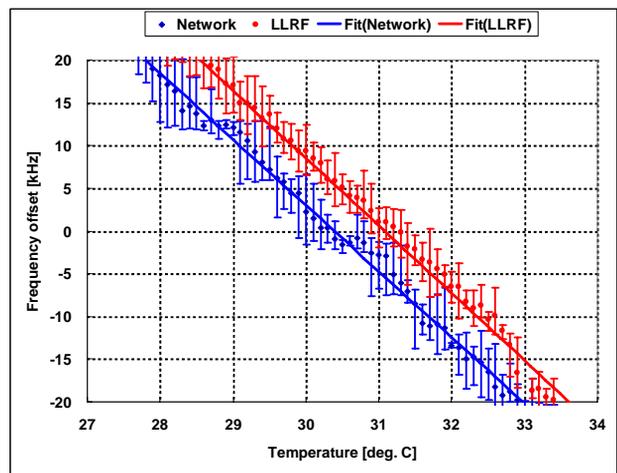


Figure 5: Frequency offset from resonance measured by network analyzer and LLRF system.

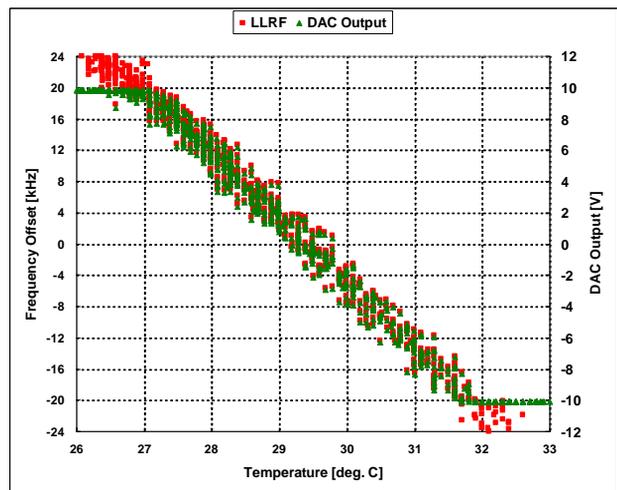


Figure 6: DAC output based on the measured frequency offset from the resonance.

CONCLUSIONS

The digital LLRF control system has been developed and tested by using a commercial FPGA board. The test results showed that the control system meets the requirements. In addition, the frequency offset from the resonance can be monitored by using the LLRF system. Use of the commercial board can reduce the development time considerably. But the limitations in flexibility such as fixed IO channel number and the operation mode are main drawbacks.

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