DEVELOPMENT OF ALL SOLID STATE BOUNCER COMPENSATED LONG PULSE MODULATORS FOR LEP 1MW KLYSTRONS TO BE USED FOR LINAC4 PROJECT AT CERN*

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Abstract

CERN is building a 352.21 MHz 3 MeV RFQ based test stand as first part of LINAC4. Extending its earlier collaboration with RRCAT, India, CERN had approached it to design and develop a high voltage pulsed modulator for 1 MW LEP klystrons, planning their reuse. RRCAT proposed three design schemes out of which an all solid state bouncer compensated modulator was chosen for follow up development work. The main considerations for the design were to avoid gas tube crowbar on the HV side, to have low rise and fall times and to realize high voltage stability of the flat top. The output voltage and current are rated up to 110 kV/24 A, with pulse duration 800 µs, repetition rate of 2 Hz, <1% droop and <0.1% ripple on pulse top with energy restricted to 10 J in case of klystron arc. Based on these principles, a modulator has been developed and constructed at CERN and is currently undergoing tests with a klystron while another one with similar development is in the final stages of integration/evaluation at RRCAT. The present paper describes the topology, simulation results, protection strategy and briefly summarizes the results achieved.

INTRODUCTION

The 3 MeV test stand will enable to explore the beam dynamics issues at the low energy end and comprises of 352.21 MHz, 3 MeV, 3-meter long RFQ, (part of SPL Front End) as the first part of the LINAC4 [1], a new PS Booster injector proposed to improve the proton beam quality and availability for CERN users in the LHC era.

LEP 352.21 MHZ, 1 MW CW klystrons will be operated in pulsed mode with maximum average power up to 2 kW, to feed the RF sections of the linear accelerators. This requirement necessitated the development of new high voltage pulsed modulators tailored for operation at duty cycle of 0.1%.

Design Considerations

The following issues were considered in the design:

- Crow-bar-less (no ignitron or thyratron) protection of klystron against arcing. The protection is assured by a) switching-off the main series switch very swiftly b) absorbing and dissipating the maximum of energy stored in the parasitic elements (stray capacitances, inductances, etc) inside the damping networks
- Low rise and fall time to limit the amount of wasted power
- High voltage stability of the flat top to assure the necessary phase stability of the RF output
- High reliability, minimum maintenance efforts and high lifetime due to solid-state construction.
- Modular structure to facilitate higher repetition rate up to 15 % duty at a later stage.
- The power supply interlock system able to be integrated into the CERN control and interlock system

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*work supported by DAE of India under aegis of DAE CERN NAT Protocol

TECHNICAL SPECIFICATIONS

The major requirements are listed in Table 1.

Table 1: List of modulator main parameters

Parameter	Design Targets
Klystron modulator type	Bouncer
High Voltage pulse amplitude	-10 kV to -110 kV
High Voltage pulse width measured at 70% to 70 % of peak.	800 µsec
Minimum Flat top available	600 µsec
Maximum current during pulse	24 A
Pulse repetition rate	2 Hz
Acceptable voltage drop	≤ 1.0%
Allowed ripple on flat top (≥ 10 kHz)	≤ 0.1%
Rise time/fall time	<100 µsec
Energy dissipated in klystron during klystron arc	<10 J

TOPOLOGIES CONSIDERED

At RRCAT we have designed and commissioned several modulators for klystrons based on the PFN topologies with step up pulse transformers, which have peak pulse power up to 15 MW and mean power up to 90 kW[2]. Few solid state switched modulators were also developed using RRCAT built stacked MOSFET/IGBT solid state switches, operating at 5 kV/0.5 A@10 µsec/ 1 Hz and 50kV/2A@10µsec/300Hz for pulsing driver klystrons and LINAC electron guns respectively. Looking into large reservoir of experience gathered on various topologies RRCAT took up the present project for CERN. Out of several schemes three options were found to be suitable and therefore an initial evaluation was restricted to: 1) Hard switched klystron modulator with high voltage programmable power supply for droop correction (active

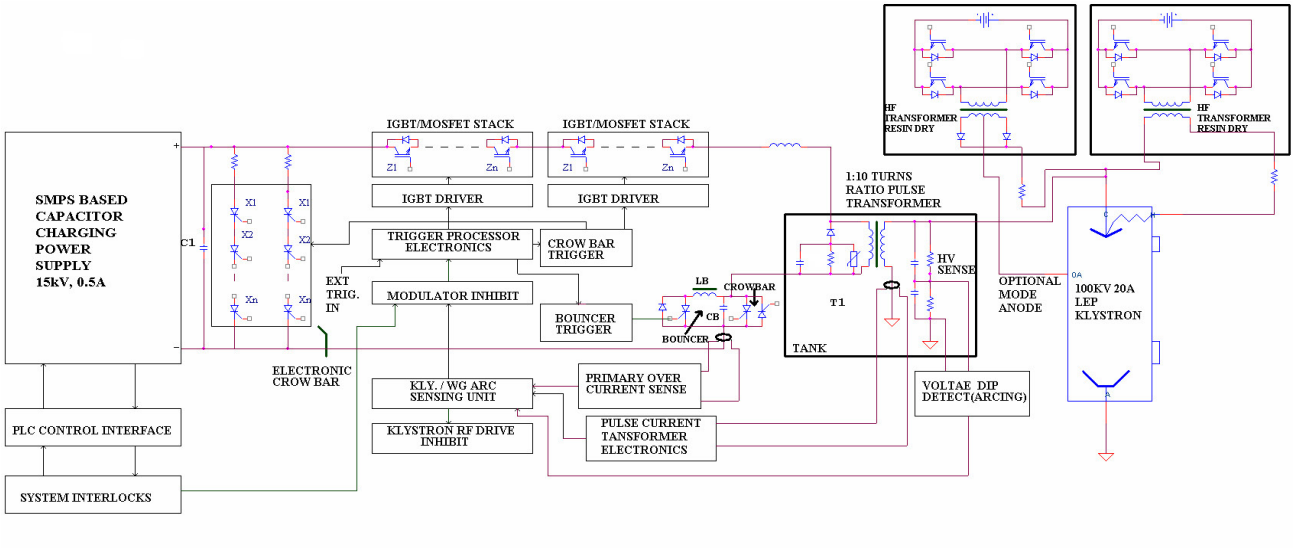

Figure 1: Solid state bouncer compensated pulse modulator schematic for LEP klystrons.

droop compensation) with step up pulse transformer; 2) Hard switched klystron modulator with bouncer circuit for droop compensation with step up pulse transformer [4][5]; 3) Pulse forming network based line type pulse modulator with step up pulse transformer. Finally option 2 was chosen for further development of the modulator.

ADOPTED TOPOLOGY USING SOLID STATE TECHNOLOGY

To meet the specifications, we have chosen a bouncer compensated all solid state klystron modulator (Fig. 1). The main capacitor bank C1, is charged to ~10% higher voltage than required for the nominal output voltage. The bouncer capacitor C_B is charged to ~10% of the required output voltage. During the generation of output pulse the pulse transformer sees the difference of main capacitor and bouncer voltage at its primary[4][5]. As the two voltages fall at the same rate due to proper designing and setting, the output voltage is constant during the pulse with <1% droop. The use of Capacitor switching with droop compensation overcomes the difficulties as normally encountered with PFN topologies and also reduces the size of energy storage device. The low loss LC bouncer circuit is chosen for better efficiency over other droop compensation techniques. The solid-state construction avoids bulky energising supplies and also improves the reliability and lifetime.

To assess the performance of this scheme a full simulation study was conducted at RRCAT whose results are shown at Fig. 2. The circuit simulation was done with basic elements of Pulse Modulator. In our actual simulation the series switch was modelled using IGBT devices in series and an ideal Pulse transformer has been connected along with equivalent circuit components transformed to primary side. As a step further a proof of principle a solid state bouncer modulator was assembled at RRCAT to demonstrate the droop compensation of 20% to 1% at a pulse width of 50 microsec with 12 kV, 0.5A output. This modulator used RRCAT made MOSFET Switches and 1:10 pulse transformer.[3][6]

Details of the Main Components

The modulator comprises of charging supply, main storage capacitor, series switch, 1:10 pulse transformer and crowbar switch. A 15 kV DC capacitor charging supply with 7500 J/s is used for linear charging of storage capacitor comprising of 4 Nos. of 50 MFD, 20 kV capacitors. For series switch IGBT/IGCT based stacked assembly with 20 kV operating voltage rating and 300 A peak current is chosen.

Droop Compensation (Bouncer) Design

The droop compensation is produced by series resonant LC circuit made of L_B and C_B bouncer inductor and capacitor respectively (Fig. 1). This bouncer circuit is triggered ON to start its cycle before the start of the main pulse of the modulator. Values of both components can be chosen to account for any variations in practice and to tune the pulse shape. To achieve the desired 1% droop the linear part of the bouncer cycle is subtracted from the drooping main capacitor bank. It has been considered to allow the main capacitor bank voltage droop to 20% so as to reduce capacitance value further. We start the bouncer waveform earlier than the modulator pulse, by triggering the bouncer switch SB1 first at a predetermined time with respect to that of the main modulator switch SW, such that the net positive energy is stored in the bouncer.

The Bouncer Switch SB1: Since we expect a 10% of nominal primary voltage across the bouncer capacitor this leads to the 1 kV voltage at the capacitor. A 3 kV switch with peak current of 1500 Amp is used.

The Bouncer Crowbar BCB1: The bouncer crowbar switch is rated for 4 kV and 2 kA.

Klystron Arc Protection

The limit of the energy to be dissipated in an arc is <20 J. We limit it to 10 J in our design. During arcing the

primary current will rise, limited only by the leakage inductance of the pulse transformer. The series switch is opened and the crowbar at the main capacitor bank as well as the bouncer circuit are fired simultaneously. A series back up switch is provided in case the main switch fails to open up due to any reason. The energy stored in the leakage inductance is 36 J and this energy is removed before it is dissipated in arc. The dip in the output pulse voltage as well as increase in the primary current above a threshold value is detected and the series switch is opened and the primary crowbar is triggered. The main switch and the back up switch are opened simultaneously to assure the removal of the voltage from the pulse transformer in few microsecond. Due to this there is an inversion of voltage at the primary up to few hundred volts, which is controlled by a circuit connected to the primary of the pulse transformer. This circuit has been realized with a parallel combination of resistor, capacitor and a MOV-resistor assembly, all connected to a back diode. The values of the capacitor and resistor are 100 µF and 50Ω.

RESULTS

Figure 2 shows the results of the simulation. Modulator built at RRCAT is shown in Fig. 3 & 4. The preliminary test was done for modulator up to 5 kV output pulse. The waveforms of tests are shown in Fig. 5. Both the simulated and tested results show <1% droop in output voltage.

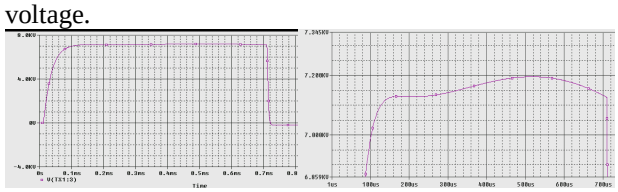

Figure 2: Simulated waveforms (referred to primary) (left) full pulse and; (right) Zoomed at flat-top.

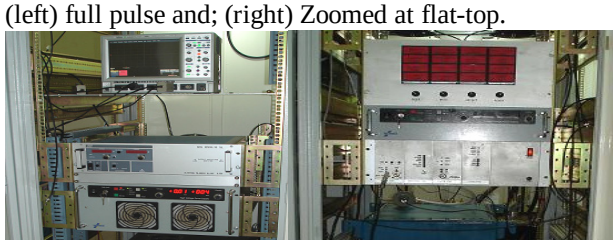

Figure 3: (left) Photo of Charging/Filament; (right) photo of trigger, controls and interlock system of modulator at RRCAT.

Figure 4: (left) resistive load in oil tank (@110kv) connected to modulator; (right) bouncer circuit elements pictures at RRCAT

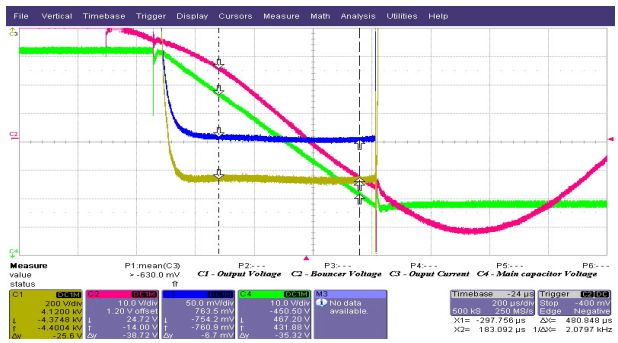

Figure 5: Obtained output during initial run, at resistive load, representing klystron impedance. Waveforms represent C1:Output voltage C2: Bouncer voltage C3: Output Load current C4: Main Capacitor voltage

CONCLUSION

We have presented design of an all-solid state bouncer compensated modulator evolved at RRCAT for LEP klystrons to be used in LINAC4 project. One modulator has been assembled at RRCAT and another at CERN and testing has been started on a dummy load at RRCAT, equivalent to klystron impedance. The performance of the systems built agrees with simulation results. After further evaluation and tests on resistive load the systems will be integrated for final use in 3 MeV test stand of LINAC4.

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