Industrial Applications of Free Electron Lasers: Extreme Ultraviolet Lithography

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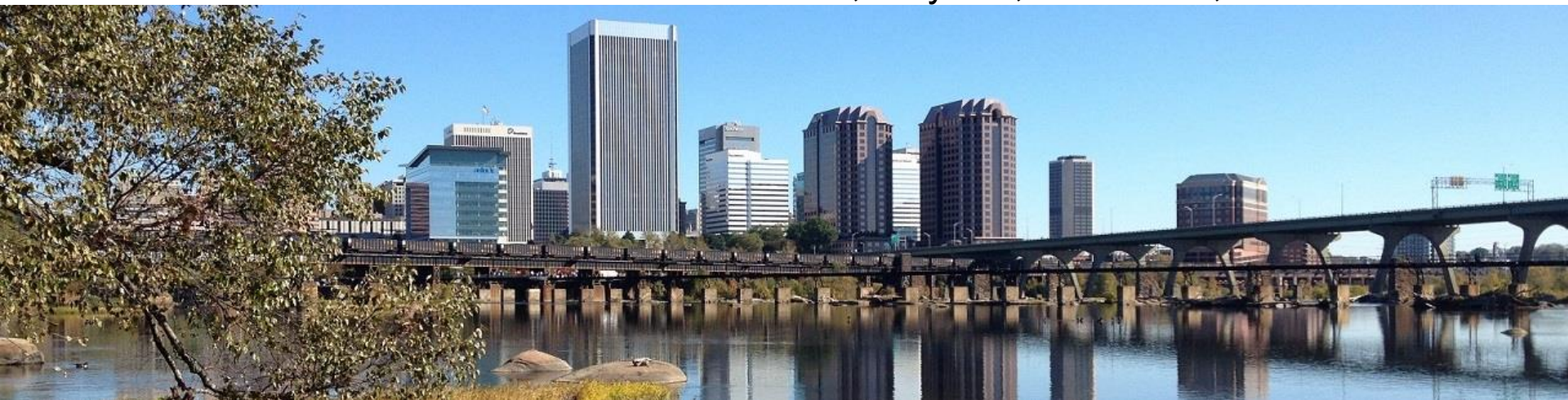
6th International Particle Accelerator Conference, May 3-8, Richmond, VA



Outline

- Semiconductor industry trends
- Overview of EUV Lithography
- Future power needs
- Key FEL source requirements

Semiconductor industry is huge economic driver

$56 Billion

Semiconductor R&D and Cap Ex (2013)

$336 Billion

Semiconductor device market (2014)

$2.3 Trillion

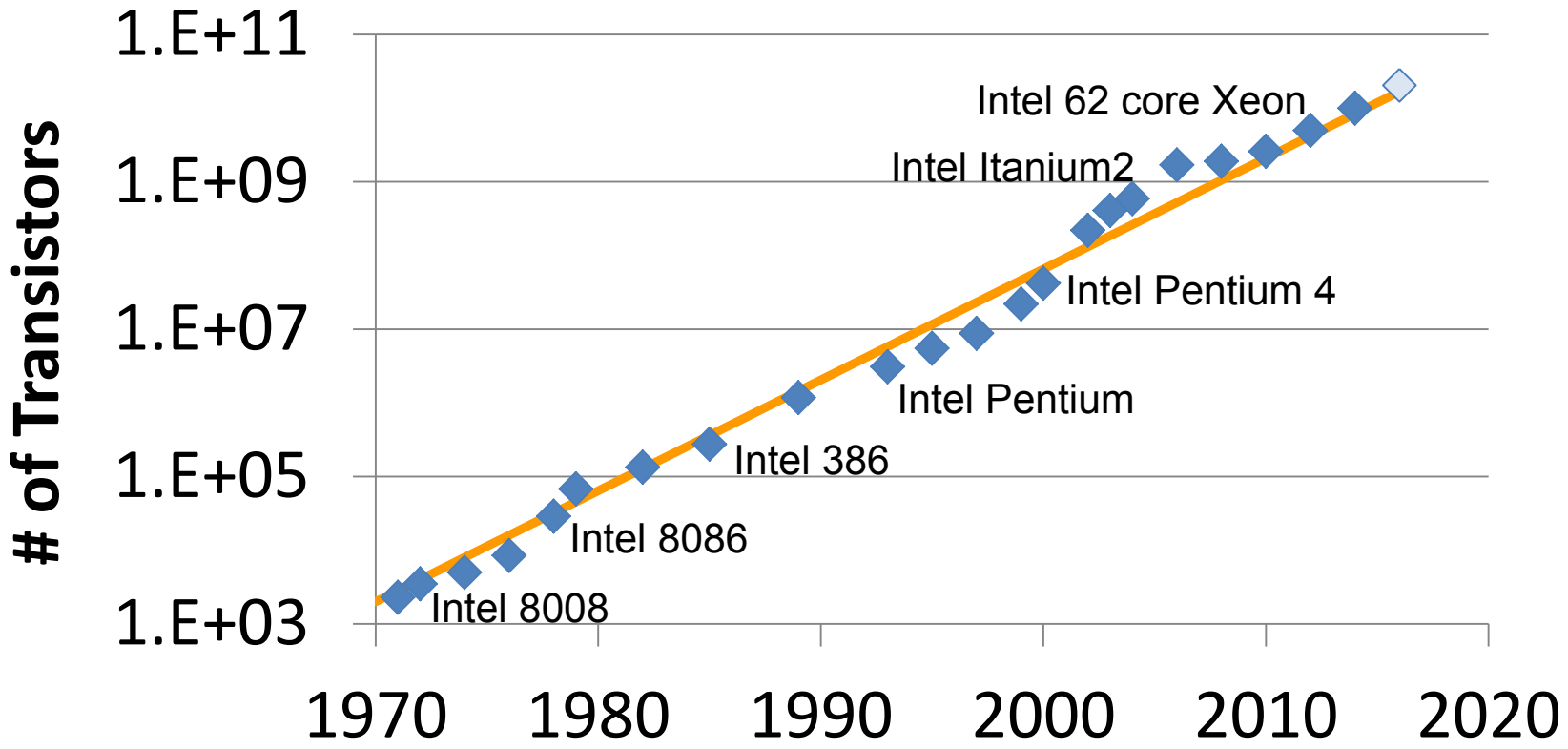
Global electronics market (2014)

SIA, www.globalsmt.net

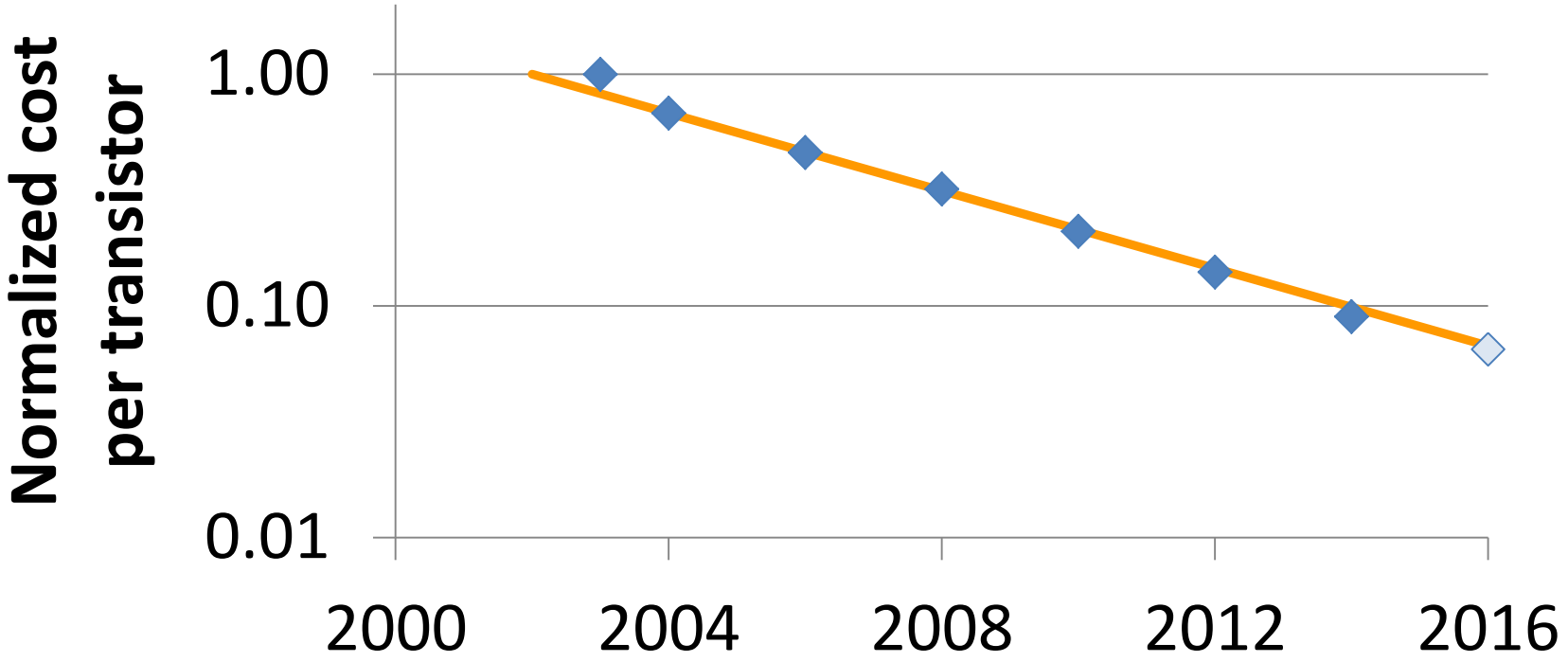
“By 2020, [expected] cost of between $15 and $20 billion for a leading-edge fab”

EE Times

Industry growth enabled by Moore's Law:
transistors double every two years



The other half of Moore's Law:
density increase at shrinking cost



Data from Intel (http://www.pcworld.com/article/2887275/intel-moores-law-will-continue-through-7nm-chips.html)

iPod nano 16 GB
$139.99

Would have cost
$32 billion in 1970

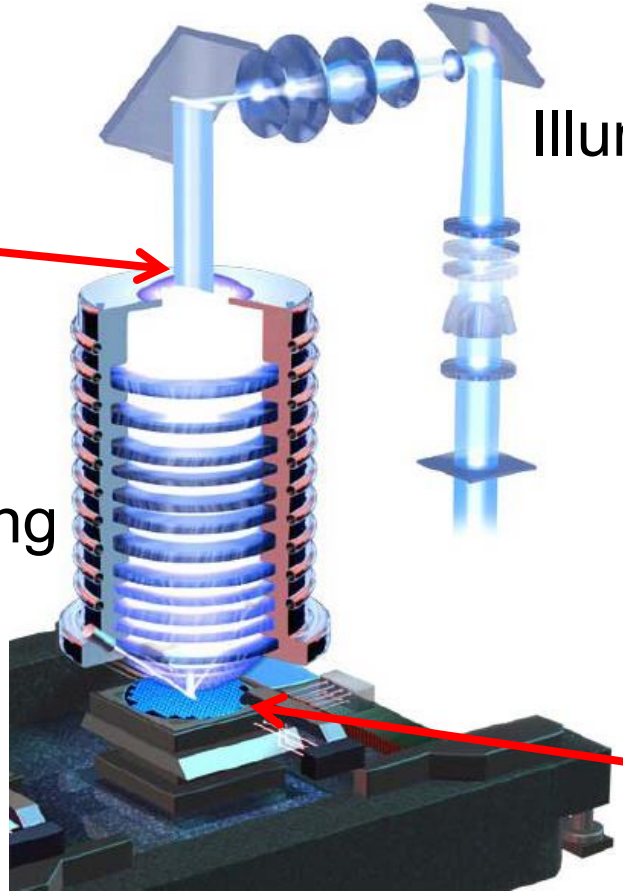
Source: www.archivebuilders.com 22045v006

Lithography drives shrink

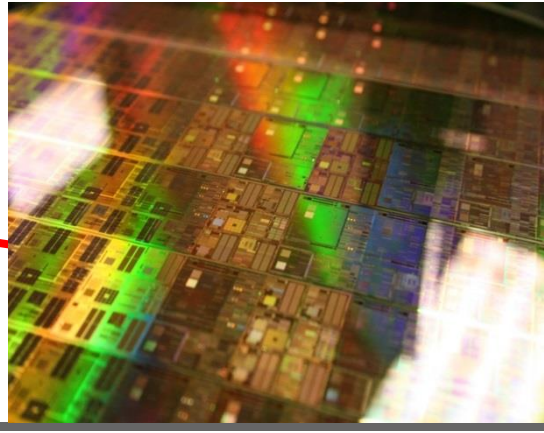
Mask

Illumination

Demagnifying lens

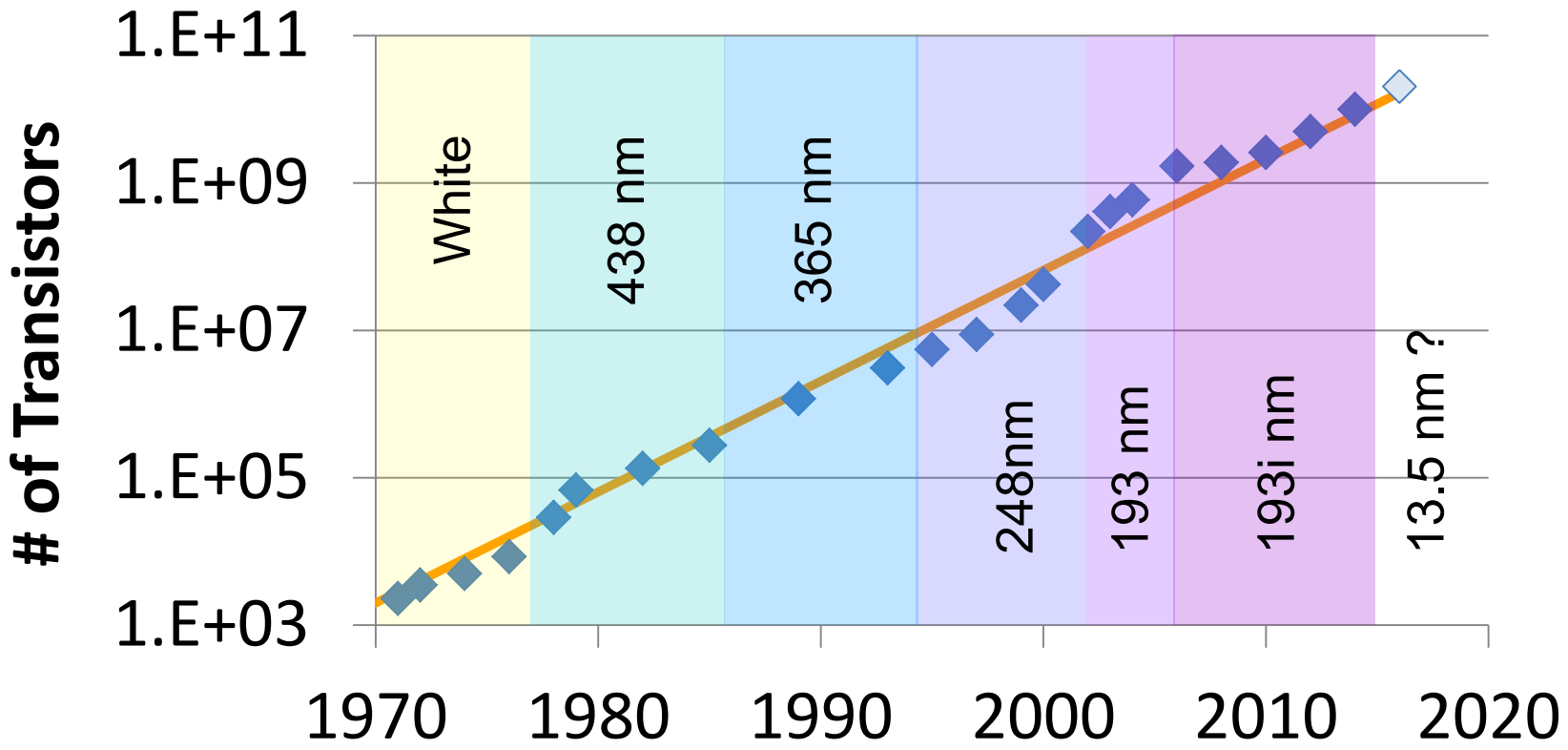


Wafer

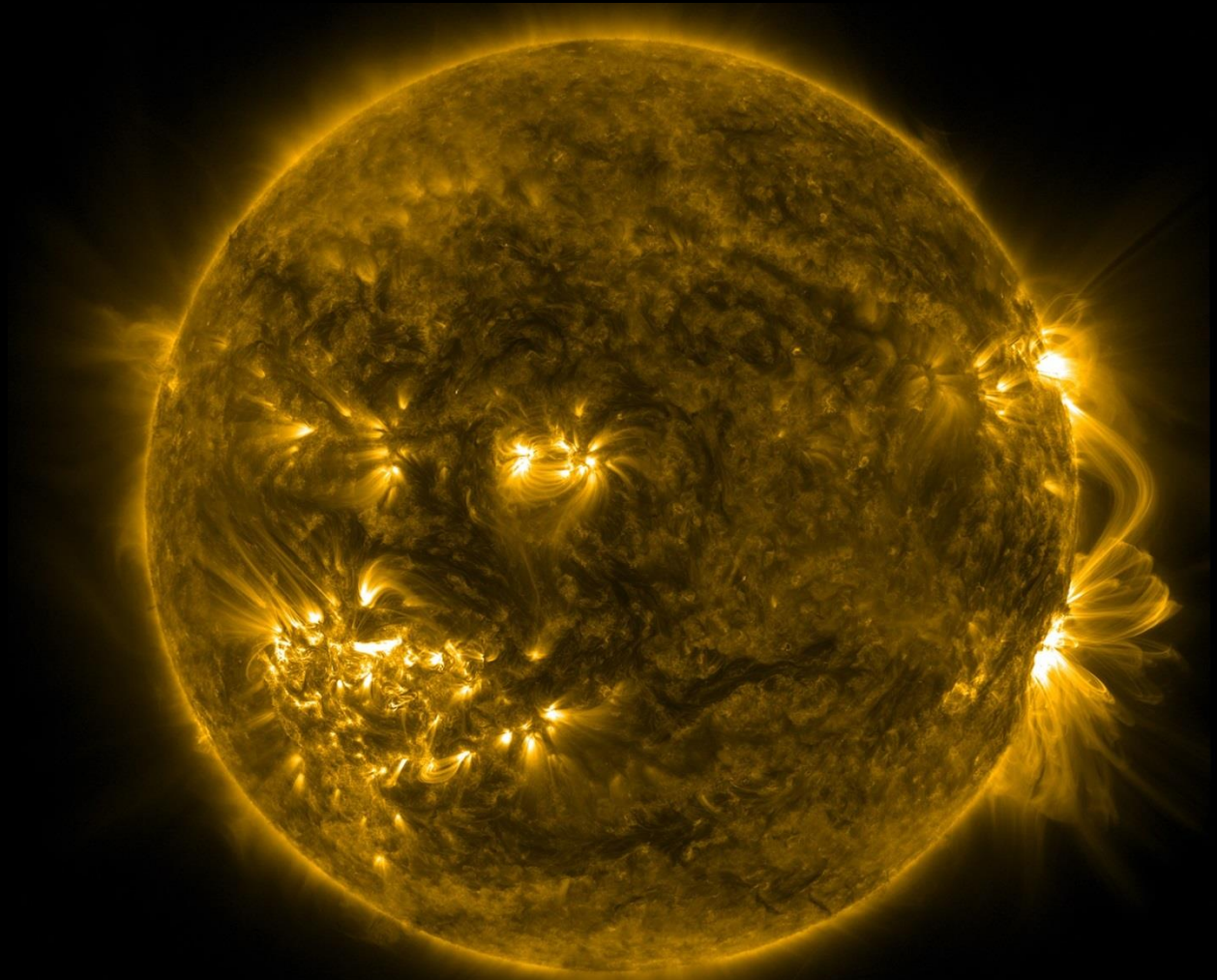


$Res \propto \lambda / NA$

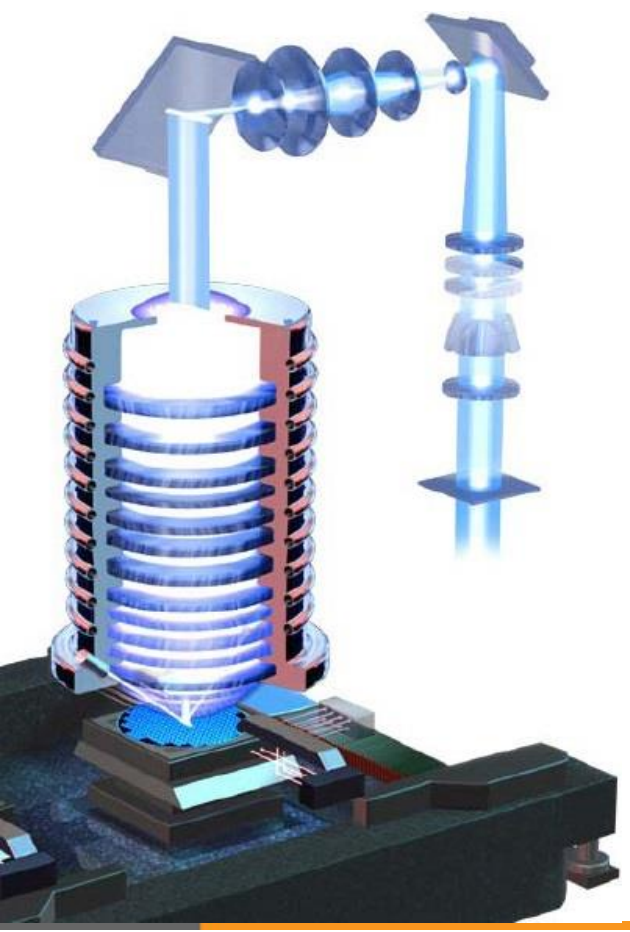
Moore's Law driven by wavelength shrink

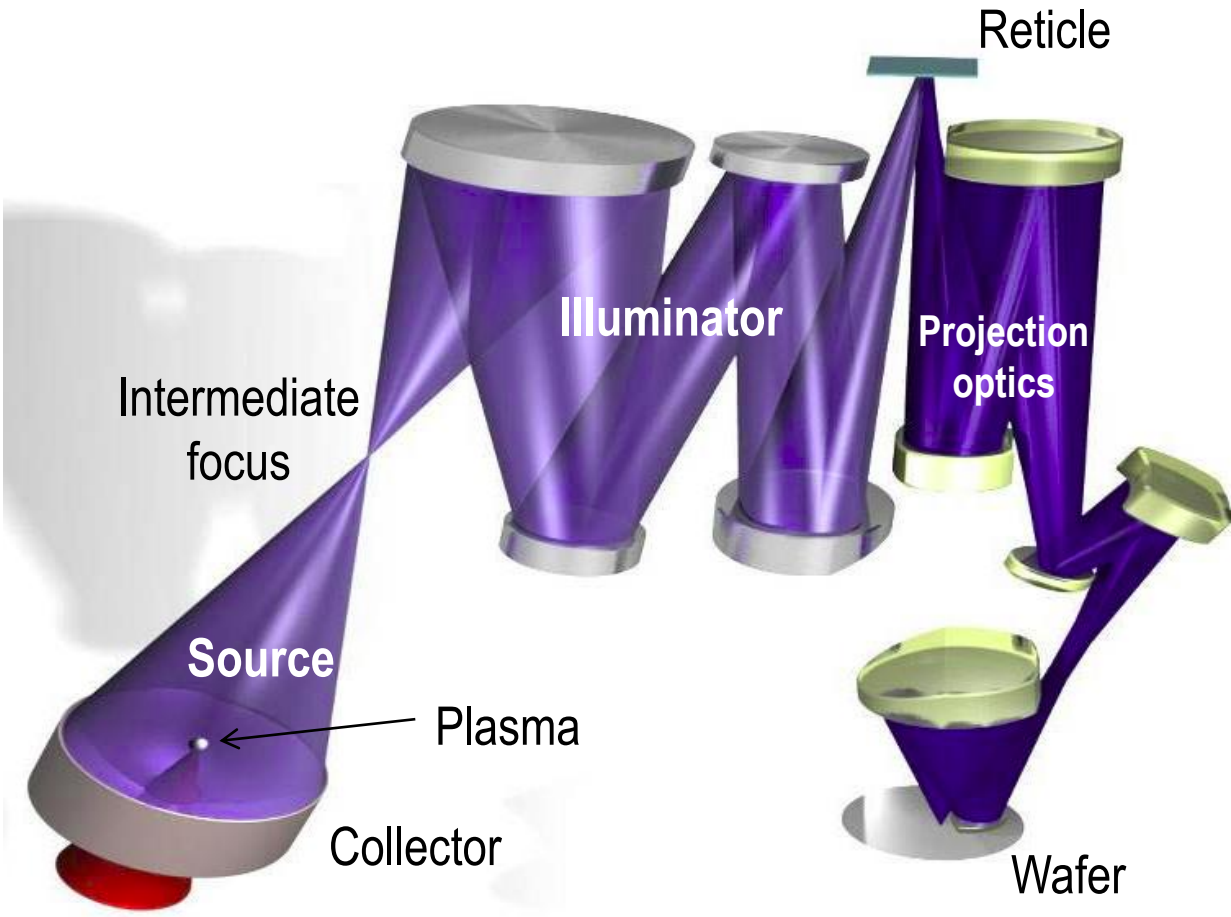


How does EUV lithography work?



EUVL: optical lithography at λ = 13.5 nm



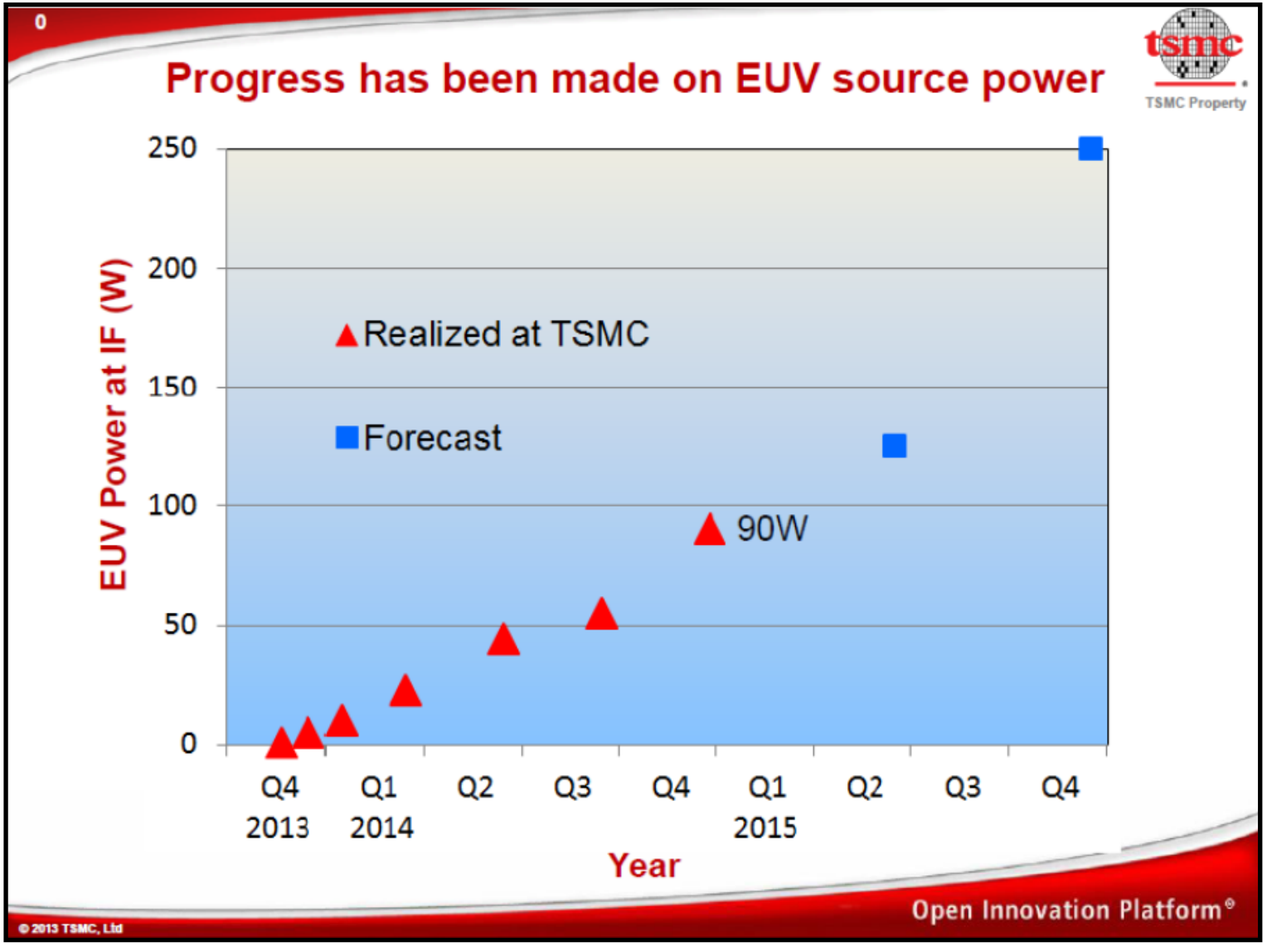


Near term source power requirements

Wafer Throughput	wafer/h	145
Total wafer time	sec	24.8
Stage motion overhead	sec	18
Wafer exposure time	sec	6.8
Wafer diameter	mm	300
Wafer fill factor	%	89%
Resist Sensitivity	mJ/cm^2	15
Required Power at Wafer	W	1.38
POB reflectivity (0.66^6)	%	8.27%
Mask reflectivity	%	62%
Illuminator reflectivity (0.66^4)	%	18.97%
Overfill efficiency	%	75%
Pellicle efficiency	%	76%
Total Optical Efficiency	%	0.55%
Required collected source power	W	250

Required source power = 250W

Tony Yen, TSMC, SPIE Advanced Lithography Symposium 2015



Intel Corporation (INTC) Said To Buy 15 Next-Gen Chip Machines From ASML For $1.5 Billion

http://www.bidnessetc.com/40602-intel-corporation-intc-said-to-buy-15-nextgen-chip-machines-from-asml-for-1/

Future source power needs?

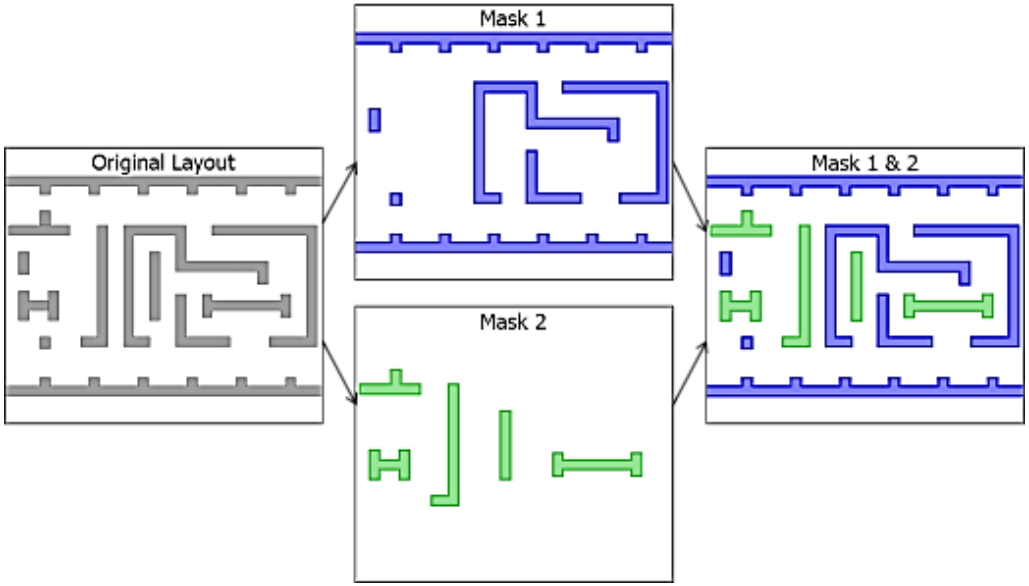
Key variable assumptions in 250W number

- Throughput = 145 Wafers/hr
- Wafer size = 300 mm
- Dose = 15 mJ/cm^2

Source power requirements expected to grow significantly in the future

Double patterning

- Throughput
  = 220 wafers/hr
- Stage overhead
  = 12 seconds

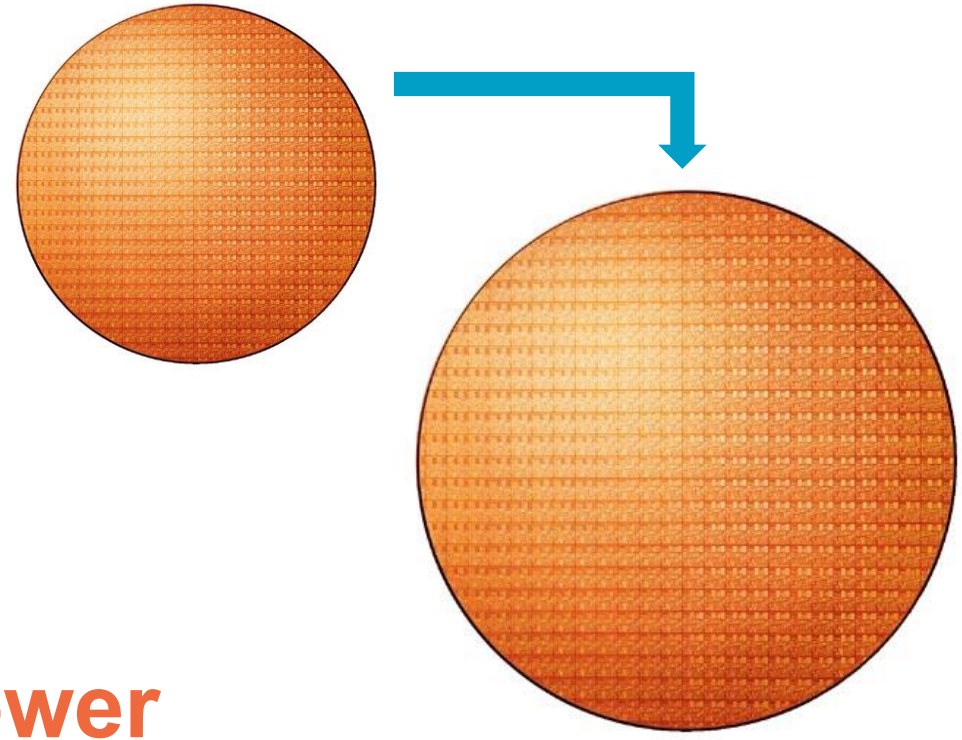


1.6x more power

Source power requirements expected to grow significantly in the future

450-mm wafers

- Throughput
  = 105 wafers/hr
- Stage overhead*
  = 12 seconds



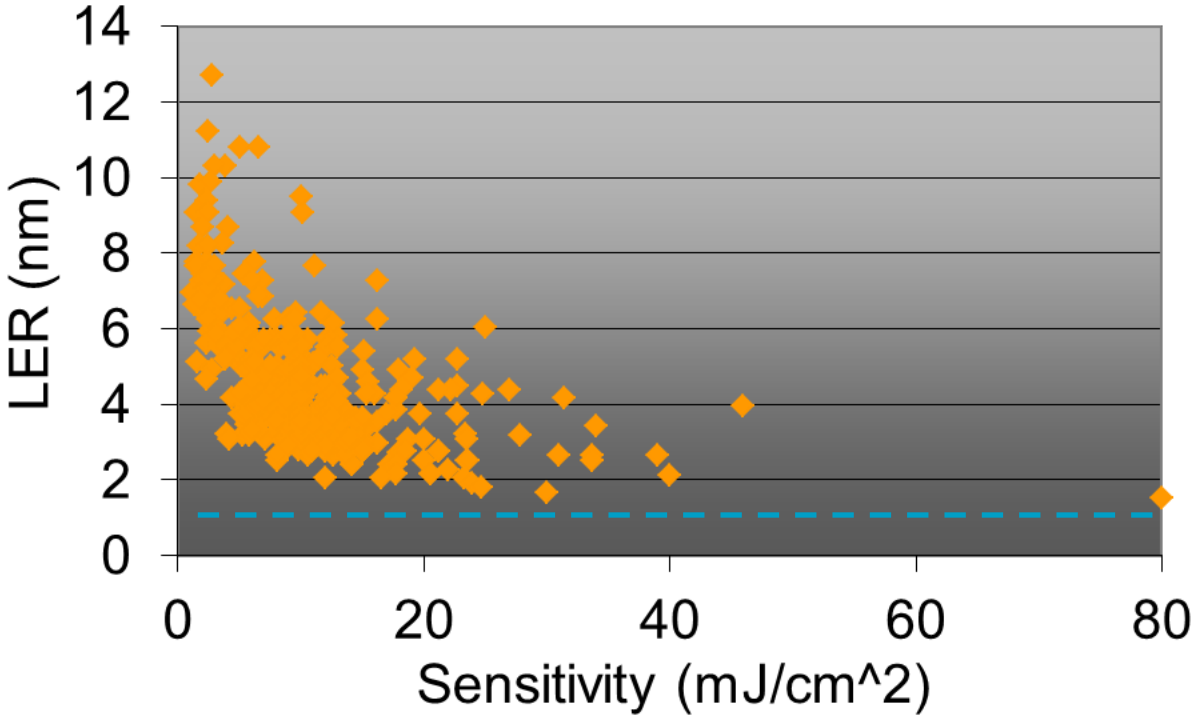
1.5x more power

* Normalized to 300-mm wafer

Source power requirements expected to grow significantly in the future

Dose

- 15 mJ/cm^2 likely not enough in the future



Source power requirements expected to grow significantly in the future

Dose

- 15 mJ/cm^2 likely not enough in the future

	Resist CA-C	Resist CA-A	Resist NCA-A
Resolution (nm)	15	16	15
LWR (nm)	3.8	3.1	1.5
Dose (mJ/cm^2)	22	30	80
Shot noise scaled dose (mJ/cm^2)	162	147	92

2-4x more power

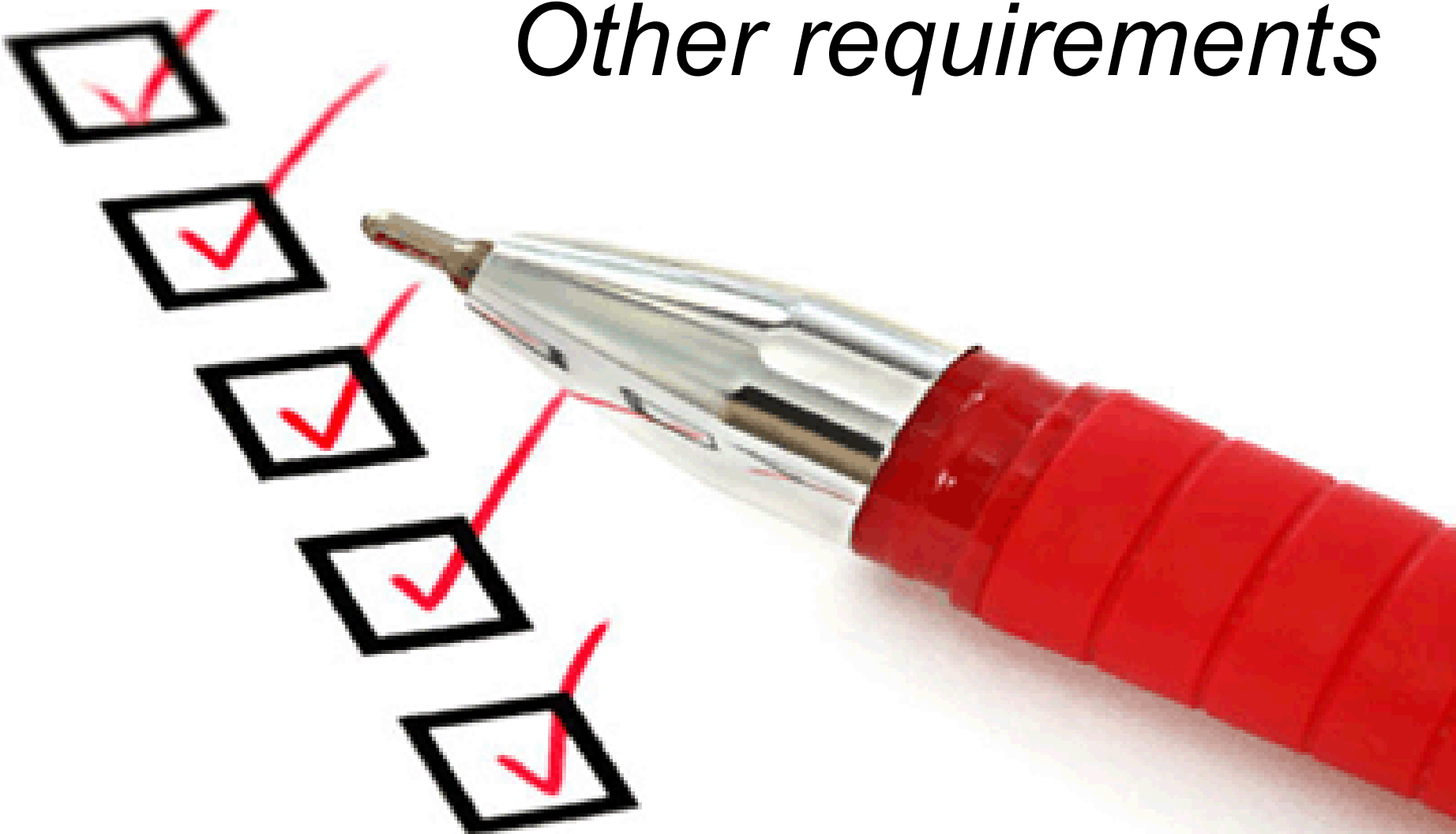
$$LWR \propto 1/\sqrt{dose}$$

Depending on resist performance, future power needs could range from 500W to 2000W

Required FEL power and size

- 20-40kW to power multiple tools
- On the order of 150 m size should be OK

Other requirements

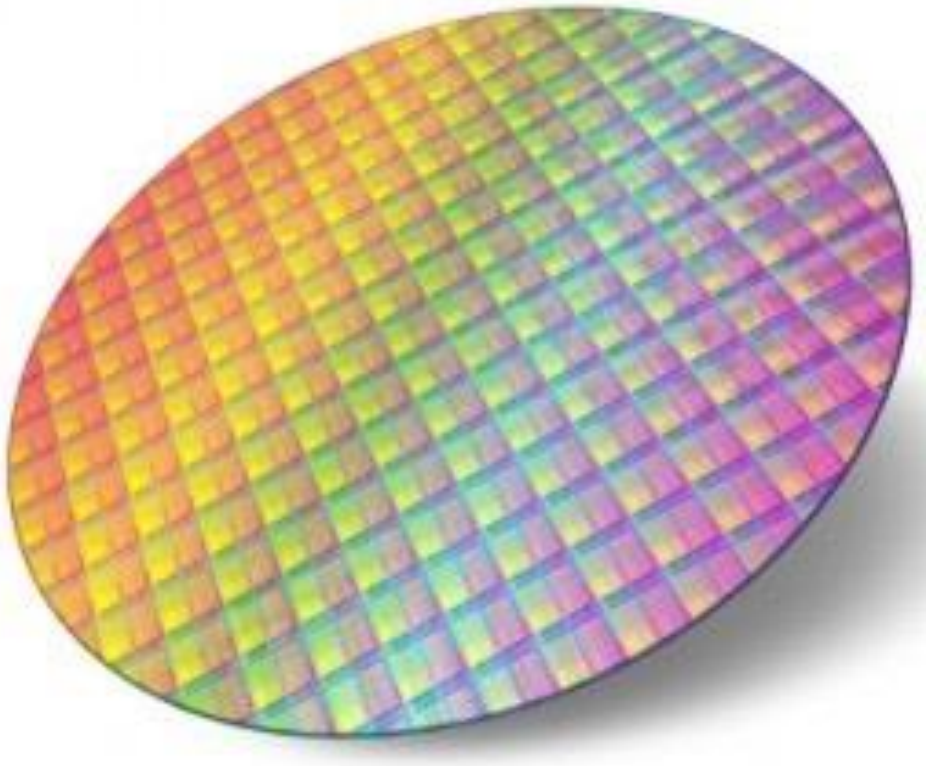


Reliability: Require > 99% uptime

Source power stability

Need <1% with 1 ms integration window

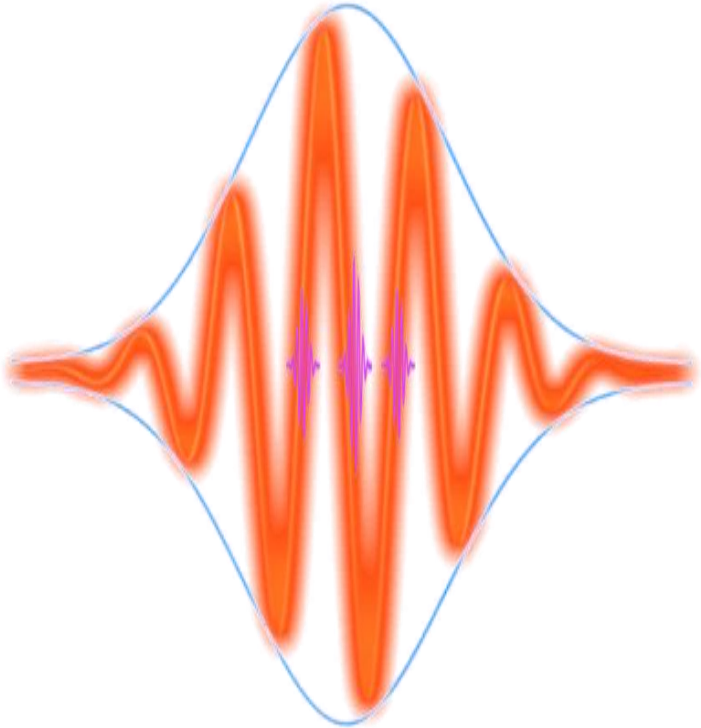
- Implies rep rate >1kHz x FPN^2
- 30% pulse noise => rep rate > 900kHz



FPN = fractional pulse noise

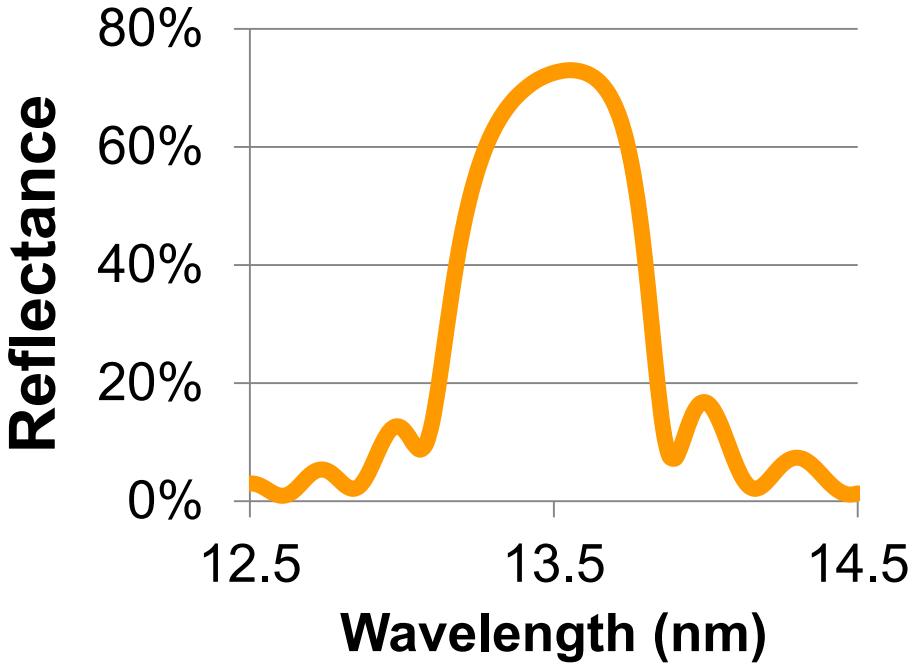
Pulse length

- Multilayer BW limits require pulse > 2.5 fs
- Longer is better to avoid optics damage issues



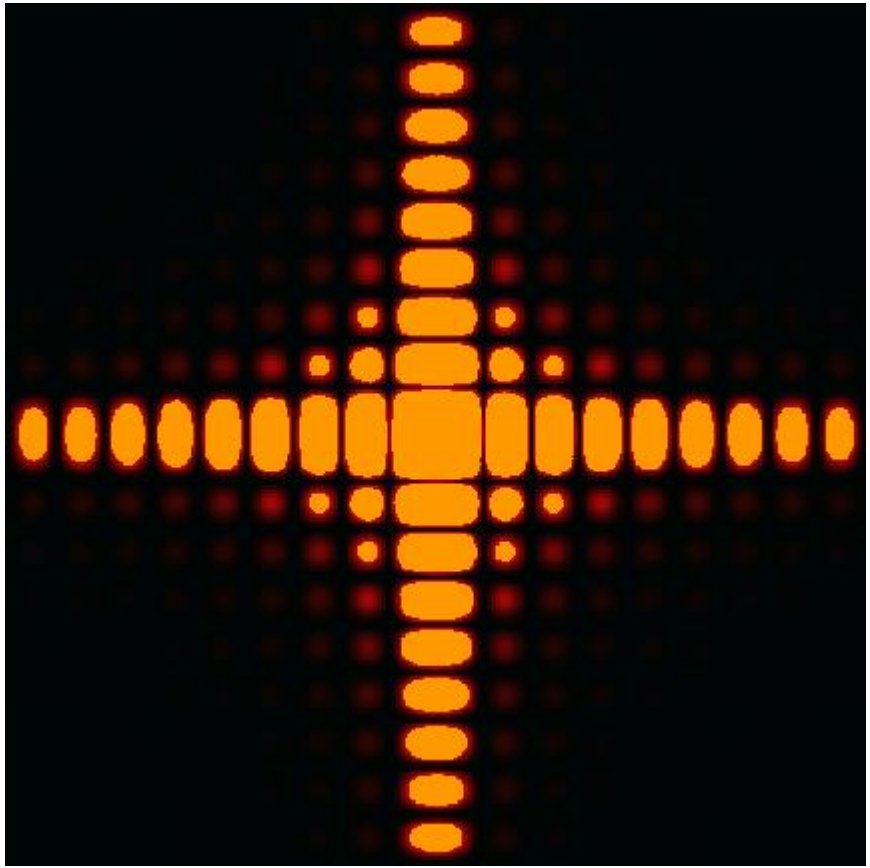
Bandwidth

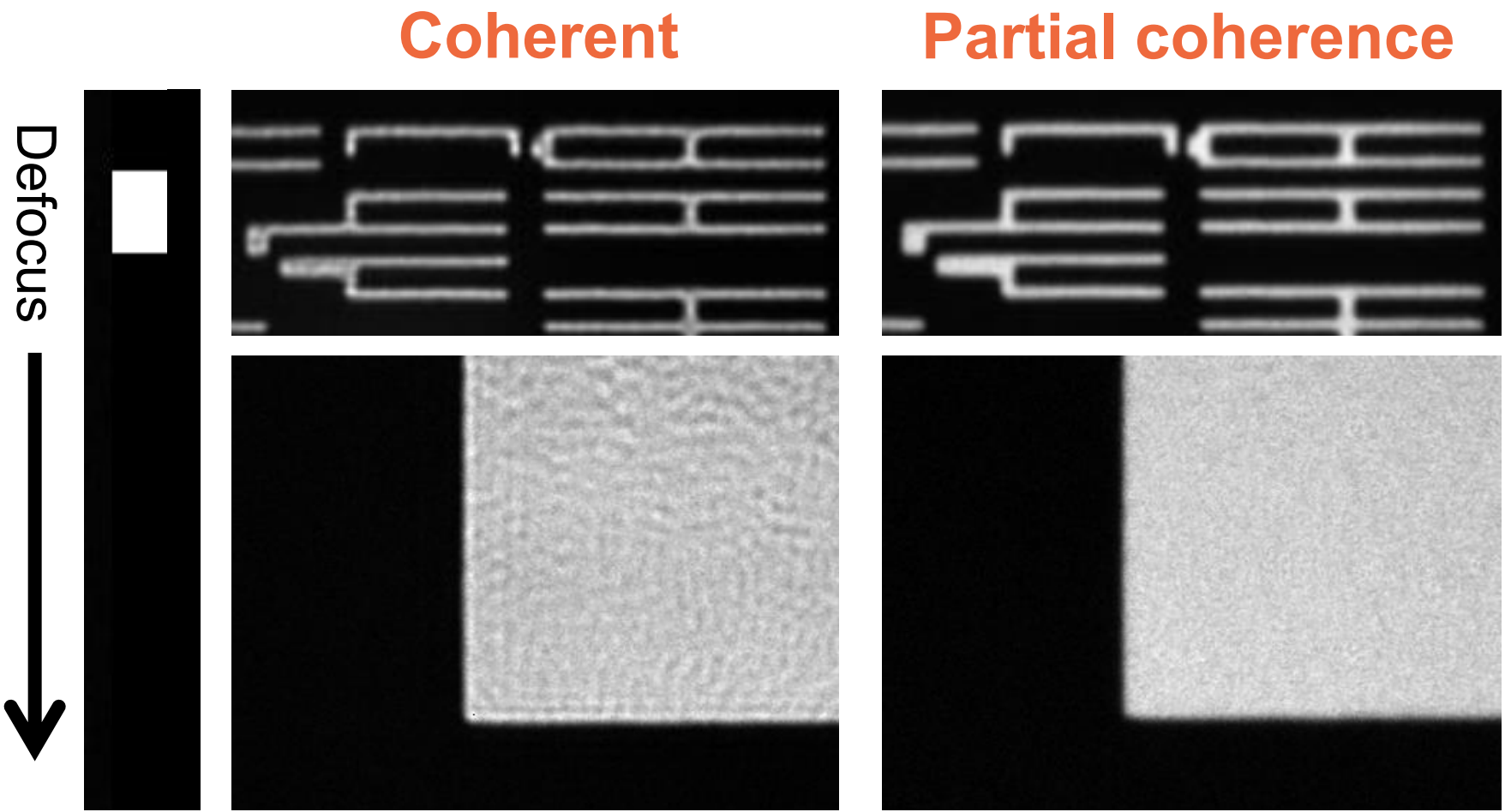
- Multilayer mirrors require bandwidth < 2%
- Narrower bandwidth = greater effective optical throughput
- Ideally < 0.6%



Coherence

- No longitudinal coherence needed
- No lateral coherence needed (coherence must be destroyed)





Data courtesy of K. Goldberg, A. Wojdyla, LBNL

Summary

- EUV is on its way
- We need creative solutions to carry the technology well into the future

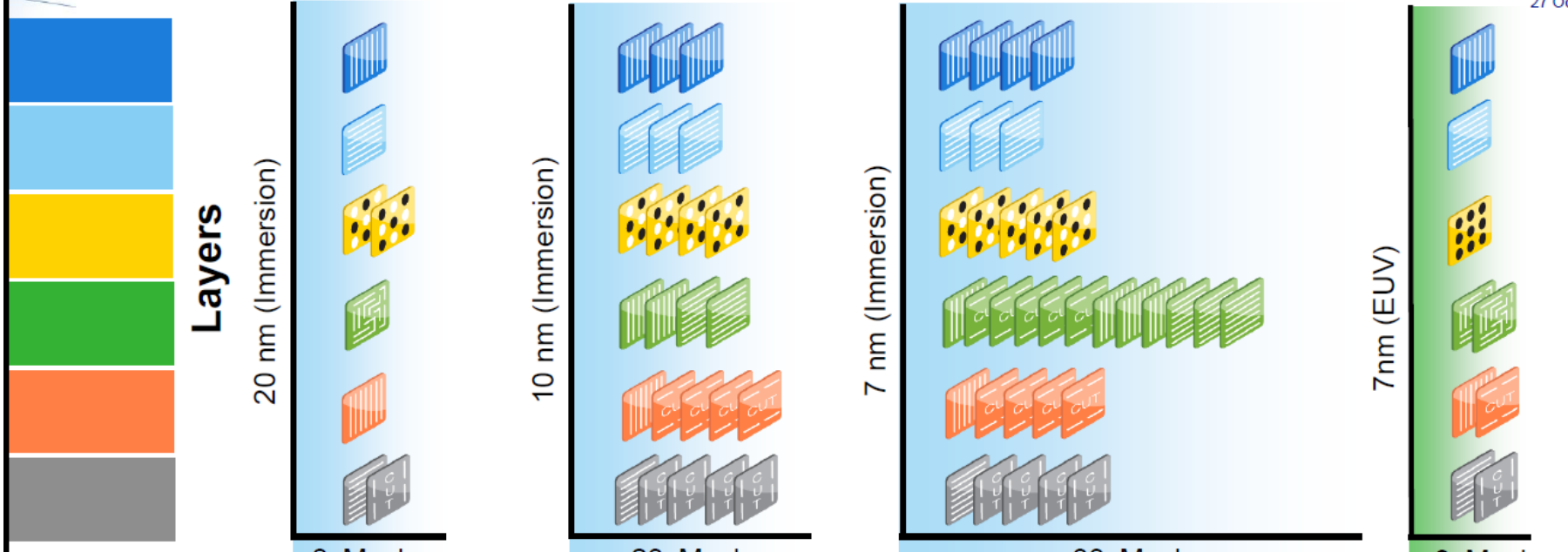
Thank You

Multi-patterning complexity drives need for EUV

EUV Lithography will stop the strong increase of litho steps/masks needed

ASML

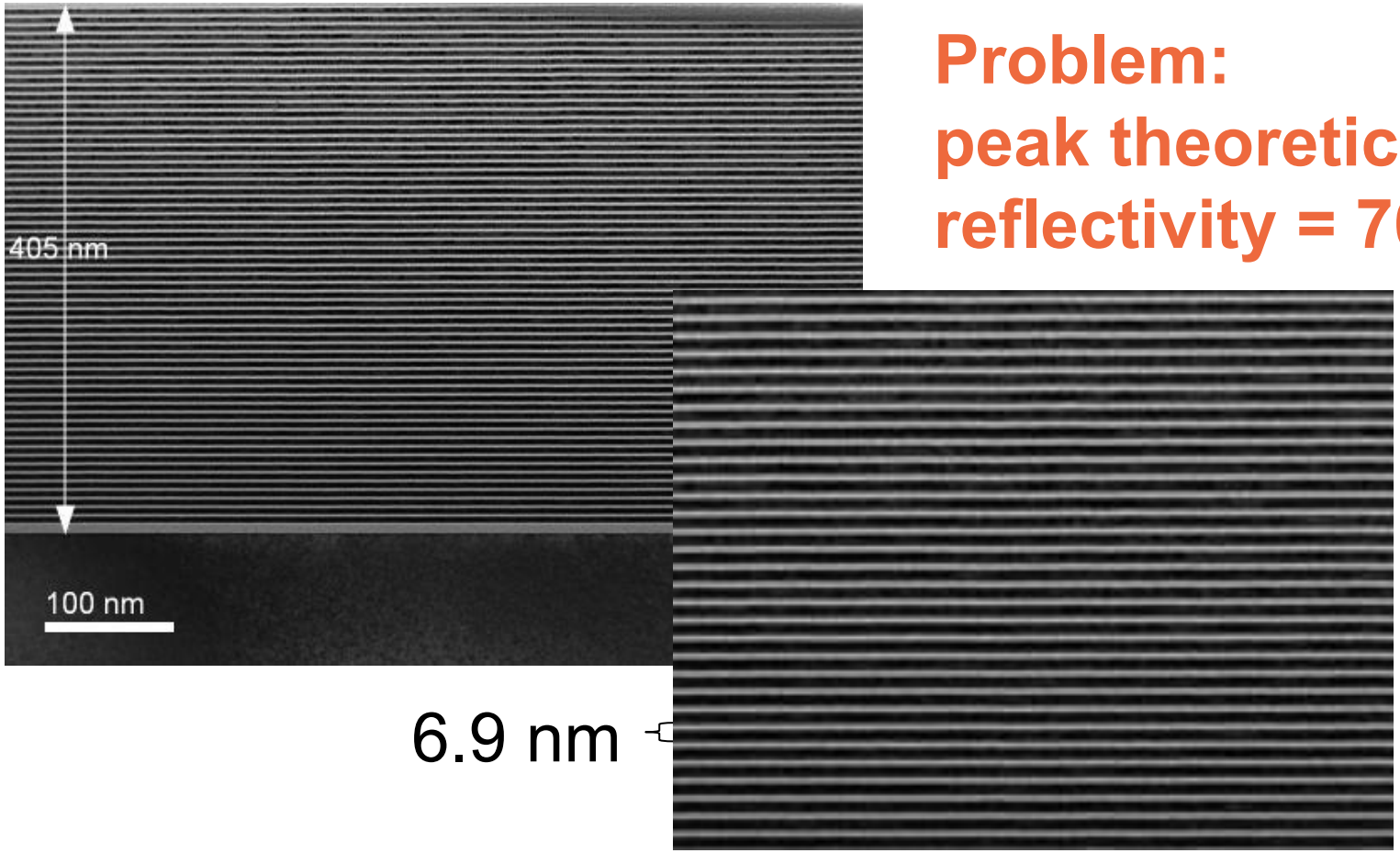
Public
Slide 4
27 Oct 2014



Node	20 nm	10 nm	7 nm	7 nm
# of litho steps	8 (Immersion)	23 (Immersion)	33 (Immersion)	9 (EUV)
# OVL Metrology	9-11	36-40	59-65	12
# max metrology / litho steps	2	3	4	3

Rudy Peters, EUVL Symposium , Oct. 2014

Mo/Si mirror: key to EUV lithography

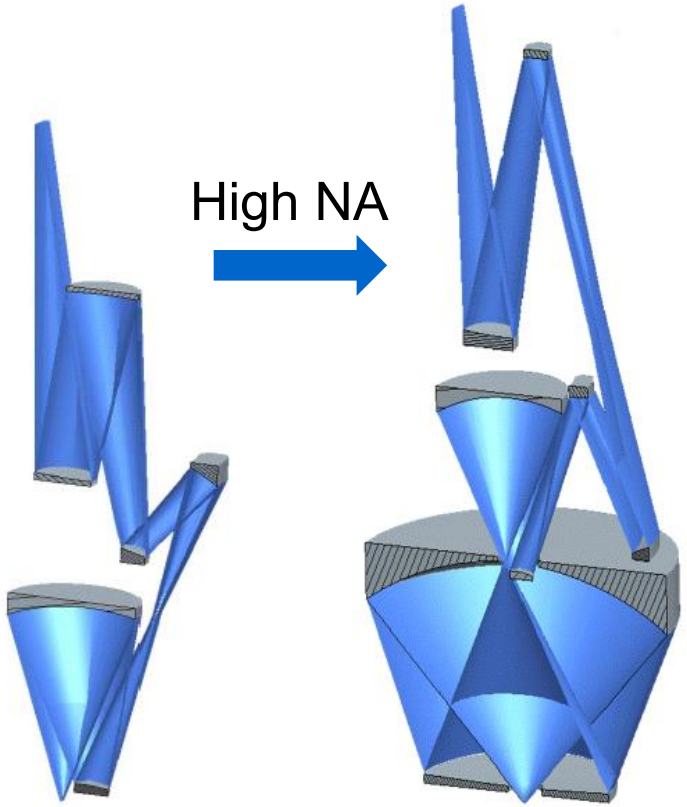


Problem:
peak theoretical reflectivity = 70%

Source power requirements expected to grow significantly in the future

8 mirrors

- Assume simple multilayer losses (no additional angular bandwidth related losses)

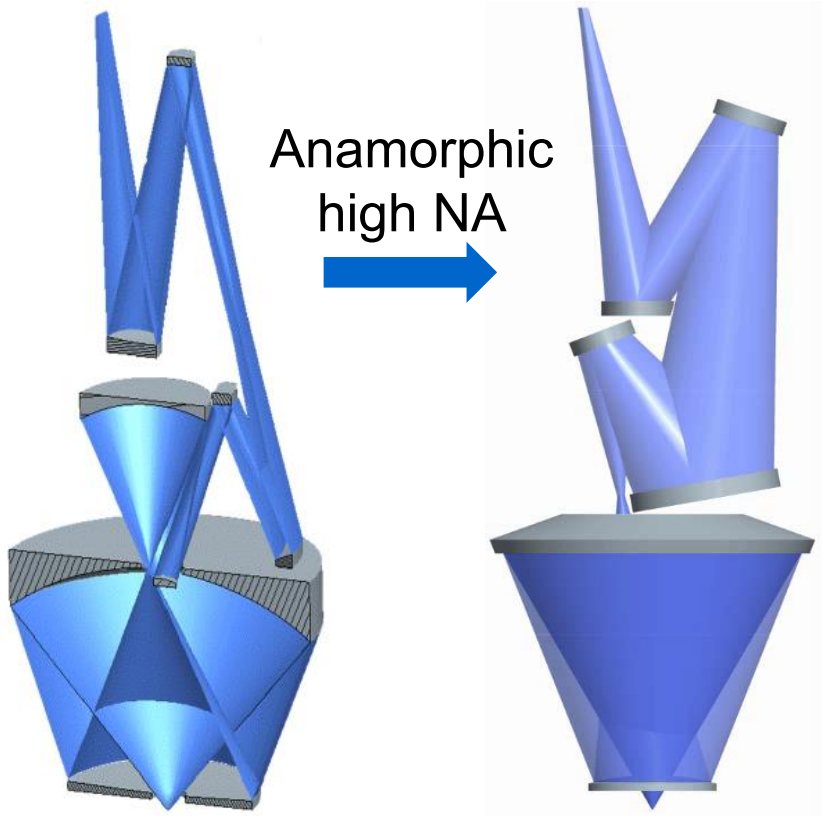


2.4x more power

Source power requirements expected to grow significantly in the future

8 mirrors

- Anamorphic design enables high NA with 6 mirrors eliminating optics as a power risk factor



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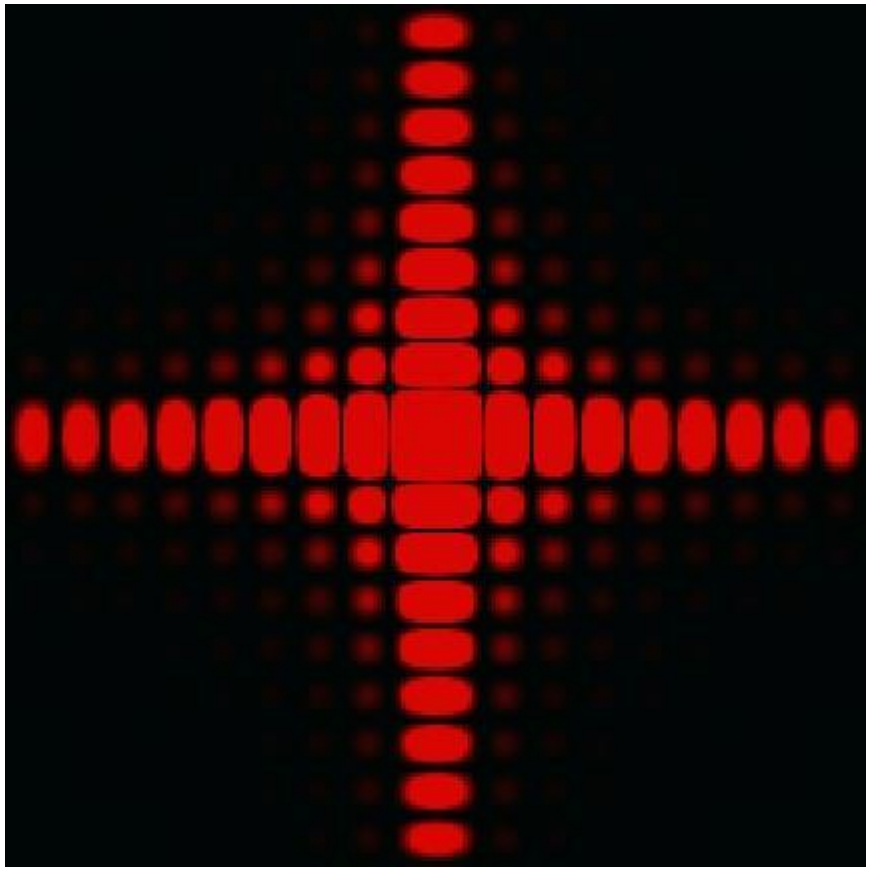

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