THE RF STABILITY OF PLS-II STORAGE RING RF SYSTEM

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Abstract

title of the work, publisher, and DOI. The RF system for the Pohang Light Source (PLS) storage ring was greatly upgraded for PLS-II project of 400 mA, 3.0 GeV from 200 mA, 2.5 GeV. Three superconducting RF cavities with each 300 kW maximum klystron amplifier were commissioned with electron beam in way of one by one during the last 3 years for beam current of 400 mA to until March 2014. The RF system is g designed to provide stable beam through precise RF phase and amplitude requirements to be less than 0.3% in amplitude and 0.3° in phase deviations. This paper describes the test results. describes the RF system configuration, design details and

INTRODUCTION

must The final quantitative goal of PLS-II is a top-up userwork service operation with beam current of 400 mA to be g completed by the end of 2014. The RF accelerating voltage of PLS-II RF system was set to 4.8 MV(1.6 g MV/cavity), which was estimated using the maximum available beam current that works as a function of RF voltage, and the top-up operation test with the beam current of 400 mA was successfully carried out. The PLS- \geq II has increased the beam energy from 2.5 GeV to 3 GeV; the number of IDs has been increased by a factor of two $\widehat{\mathfrak{L}}$ (20 IDs); and the beam current has been increased from R 190 mA to 400 mA. The beam emittance has been © reduced to below 10 nm while retaining the existing PLS

tunnel as well as the existing injection system [1]. The radio-frequency (RF) system of the electron The radio-frequency (RF) system of the electron SR for \overline{o} the light source generates a sufficient RF accelerating BY 3. voltage and transfers RF power to the electron beam to compensate for the beam energy loss due to synchrotron Oradiation from the bending magnets and IDs. Three g superconducting RF systems are installed in the PLS-II ъ storage ring.

The schematic diagram of a KI survey is storage ring is shown in Fig. 1. The PLS-II RF system components: (1) low level RF b control system(LLRF) with EPIC IOC, (2) a continuous wave (CW) klystron with a rated output power of 300 kW at the frequency of about 500 MHz, (3) a 300 kW circulator which isolates the klystron to protect the þ klystron form reflection power from cavity, (4) a 300 kW water cooling ferrite load which terminates the RF power by converting the RF power to thermal loss at the ferrite panel and (5) a CESP P territ panel, and (5) a CESR-B type cryomodule produced by RI (former ACCEL).

The RF power generated by klystron is incident to the from superconducting cavity (SC) through WR1800 waveguide, the ceramic RF vacuum window and the RF coupler to

build a RF field at the SC RF cavity. The LLRF system gets the amplitude and phase information of the RF field from the signal at the cavity RF pickup and keeps the RF field stable by controlling the amplitude and phase of forward power in the presence of various external noises such as beam loading effect, mechanical vibrations, changes in the electrical length of the waveguide between the klystron and the cavity, and the pressure fluctuation in the Liquid He vessel [2].

Each cavity consists of a cell elliptical type. The cavities are tuned to 500MHz, and individually controlled by a mechanical stepper motor with tuner. Each cavity is powered and controlled by a single klystron and LLRF system. The klystrons produce 300 kW Maximum. The RF controls use a traditional heterodyne scheme and digital down conversion at an intermediate frequency (50 MHz). Each cavity field and resonance control PI algorithm is contained in two FPGAs. One FPGA is in the field control chassis (FCC manufactured by JLAB RF Group), controlling a single cavity. The resonance control chassis contains the other and controls three cavities simultaneously. Controls and interfaces for the most of RF system devices are provided through EPICS [3].

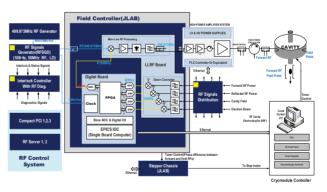


Figure 1: The schematic diagram of the RF station for PLS-II Storage Ring.

RF SIGNALS MEASUREMENT & FEEDBAK CONTROL HARDWARE

Each cavity is controlled by a single LLRF system, called here FCC. an FCC contains five fast ADC channels (receivers), although one receiver channel has no heterodyning frontend in order to direct sample 10 MHz external clock reference. All RF signals, once downconverted and digitized, are processed in an FPGA. The FCC requires an external 20 dBm LO (450 MHz) and external 3 dBm clock reference (10 MHz). The clock system has a programmable digital PLL and can work with different references as well as produce assorted sampling frequencies. A fast DAC channel produce 50

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MHz IF signal with fast DAC using non-sampling. The 50 MHz IF signal up-converted with LO signal using a mixer and drive the high power amplifier in order to feed the proper RF power in the cavity.

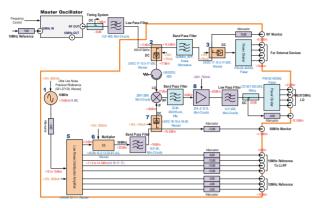


Figure 2: The schematic diagram for RF, LO generation.

Figure 2 shows producing the synchronized precision RF signals as LO, RF and distribution from 10 MHz ultra-low noise precision reference (501-07128, Wenzel). Advantage of this design scheme is maintained the same clock (4/5 xIF : 40 MHz) and IF(50 MHz) signals during the RF frequency changing because of the SR frequency feedback control.

The FCC is equipped with a number of slow (1 MS/S) ADCs and DACs as well as digital (opto-isolated) I/Os, which will be used for cavity resonance control and machine protection. The five 16-bit ADCs(LTC2205) operated at 40MS/s, and one 16-bit DAC(MAX5885) operated at 40MS/s. ALTERA CYCLONE3 FPGA EP3C55 provides signal processing path, and connects to an PC104 EPICS/RTEMS IOC(MOPSlcdLX AMD 500 MHz SBC, KONTRON). The LLRF system relies on FPGA (Field Programmable Gate Array) and digital signal processors optimized for real-time signal processing. The digital feedback RF control system performs feedback algorithm on the field signal, resulting in control in phase and quadrature (I/Q) outputs, which are processing DSPs (Digital Signal Process) for slow and complicate processing. The total feedback loop delay is considered to be less than 1uS, including all of the RF components, cables, ADCs, DACs and FPGAs [4]. The digital feedback RF control system is relatively complex as shown Fig. 1. The phase lock loop circuitry, based on a low skew clock synthesizer (CDCM7005, Texas Instruments) can lock the on-board voltage controlled crystal oscillator (VCXO) to an external source. In our case, that source is a 10MHz master oscillator signal. A synchronized clock PLL signal with (40MHz LVPECL) generation is serially-programmed to accommodate the optimized clock signal frequency. The RF amplitude and phase resolution depend on the ADC sampling clock jitter relative to the various RF sources in the system.

The developed firmware supports mainly GDR (Generator Driven Resonator) mode of operation although other modes like tone or SEL (Self Excited Loop) are also available [5]. The communication with PLS-II EPICS

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and control system via the LLRF server is accomplished by an work, publisher, embedded PC104 board (EPICS I/O controller). All systems were brought into operation using an EPICS operator screen.

BEAM OPERATION AND RF FEEDBACK CONTROL RESULTS

Figure.3 shows a measurement set-up for the RF stability verification. This setup could vary depending on the specific measurements requirements. There are two types of communication used for testing: Ethernet for EPICS software, and JTAG with Altera/Quartus software for basic hardware troubleshooting. The phase noise measurement was made using a Rohde & Schwarz Source Signal source analyzer. Dynamic range and linearity measurements were characterized with an HP Vector Voltmeter. Spurious measurements were made with a Spectrum Analyzer.

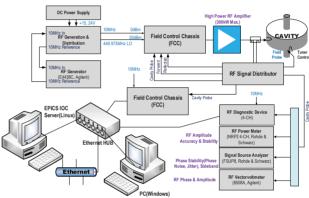


Figure 3: Set-up for RF Stability measurement.

The stability of the amplitude and phase of the cavity fields plays an important role in the beam energy spread, a critical figure of merit for nuclear physics experiments. Table 1 shows cavity field maximum allowable errors and the measured rms.

Table 1: Cavity Field Requirements and Measured Value

Electron	Amplitude(rms)		Phase(rms)	
Beam	Spec.	Measured	Spec.	Measured
direction		(FCC)		(FCC)
Cavity1	< 3.E-0.3	1.E-03	< 0.3°	0.31(0.16)
(1^{st})		(2.E-03)		
Cavity2		4.E-04		0.18(0.07)
(2^{nd})		(7.E-04)		0.18(0.07)
Cavity3		9.E-04		0.20(0.04)
$(3^{\rm rd})$		(6.E-04)		

In our case the digital LLRF system met these requirements with some margin. In fact the phase error would be much better, but it is dominated by the phase noise of the local oscillator.

Cavity frequency control is provided by a mechanical stepper motor. The stepper motor provides coarse tuning and can tune the cavity to ± 1 Hz of the reference. The control bandwidth (speed) is 1 Hz and is limited by the mechanical resonances of the cavity. The connection was

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the of The used between the field control chassis and the stepper is motor driver chassis. This eliminated the lag between the second and actual tuning, allowing for tighter and faster tuner control.

Figure 4 and 5 show the field accelerated RF voltage and phase variations during 1 hour.

maintain attribution to the author(s). title of the 1650 1645 1635 1655 1640 1630 1650 Acc. Voltage(kV) @SRF1 1635 1625 1645 Acc. Voltage(kV) @SRF2 1640 1630 1620 Acc. Voltage(kV) @SRF3 1625 1615 1635 1620 1610 1630 1615 1605 1625 1610 1600 1620 1605 1595 1615 1600 1590 1610 1595 1585 1605 1590 1580 1600 1585 1575 1595 1580 1570 1590 1585 1575 1565 1570 1560 1580 1555 1565 1575 1560 1550 - 1570 1555 1545 1565 1540 L 1560 1550 50000 100000 150000 200000 250000 300000 350000 Sampling Data(373,261/hr)

Figure 4: Accelerated RF voltage variation during 1-hr at 340mA stored electron beam.

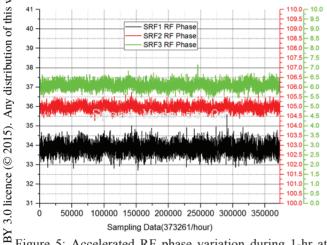


Figure 5: Accelerated RF phase variation during 1-hr at 340 mA stored electron beam.

With the loop closed we optimized proportional and integral gain by minimizing amplitude and phase noises. The optimized power spectral density of phase noise signal and its integrated RMS value measured for the superconducting cavity with 340 mA electron beam in the PLS-II storage ring. Figure 6 shows phase noise values between 500 and 800 fs were measured for three RF stations. Spurious signals at 60 and 120 Hz were also observed between -60 to -65 dB relative to RF carrier. But Spurious at 26Hz observed about -50 dB in cavity 1(1st). RF phase noise and phase variation range in cavity 1 as shown Fig. 5 is larger relative other cavities because of 26Hz spurious. We will solve this problem in the near future. Residual phase and amplitude was the

Residual phase and amplitude was measured using FSUP8 signal source analyzers and NRP-Z11 USB RF power meter. For 4.8 MV (1.6 MV/cavity) at 340mA at

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3GeV in PLS-II storage ring the RF system performance was better than the required control specification.

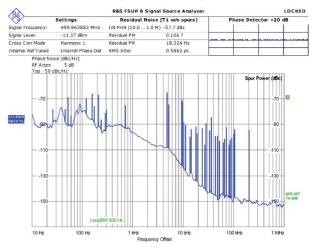


Figure 6: measured RF phase noise in cavity 3(3rd).

SUMMARY

The RF accelerating voltage of PLS-II RF system was set to 4.8 MV(1.6 MV/cavity), which was estimated using the maximum available beam current that works as a function of RF voltage, and the top-up operation test with the beam current of 400 mA was successfully carried out. The RF system performance was satisfied the required control specification. But it is need to solve the present problem and improve the RF stability continuously.

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