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ALGORITHM AND CIRCUIT TO IMPROVE ZERO-CROSSING STABILITY OF BIPOLAR TPS TRIM COIL POWER SUPPLY

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Abstract

In TPS (Taiwan Photon Source) project, 58 home-built small form factor bipolar power supplies are used to fine-tune the trim coil of booster ring bending dipole magnets. With the preliminary analog PI control loop design version, current output will tend to behave with poor linearity around zero current. By employing DSP chip, a full digital PI control loop design together with optimal MOSFT switching algorithm and 13bits PWM output capability is capable of improving the output current performance around zero current. Before the final realization, MATLAB SIMULINK is utilized to find out the optimal MOSFT switching algorithm, and then physical circuit is implemented and tested. The result and design will be demonstrated in this paper to show significant improvement around zero current.

INTRODUCTION

In TPS the sextuple and trim coil magnets converters of booster ring under operation are made by NSRRC and ITRI, the output current behaves nonlinearly at zero crossing with the analogy regulation control loop. In this paper, the original analog regulation loop is replaced by the fully digital regulation control one.

NI sb-RIO board is selected to implement digital PID controller and PWM command generation. NI sb-RIO board has FPGA built inside. All the digital control circuit are designed and written in VHDL code, thus design can be downloaded on the fly to the board for rapid verification.

The development of this NI sb-RIO board-based digital regulation control circuit of TPS's storage sextuple and corrector magnet power converters is based on the framework of NSRRC-ITRI CPS converter with a shunt as a current sensing component that could reduce the cost and less compromised performance to fulfill the fully digital regulation control implementation.

During the preliminary design phase, Matlab simulink is used to simulate the characteristic of the full bridge construction, the function of compensator and the PWM regulation algorism, and the accuracy of the control policy is confirmed.

With the NSRRC-ITRI CPS converter with the full bridge architecture as the test platform, the original analog regulation control loop circuit is replaced by the home-made digital regulation control circuit, including NI sb-RIO Board, Analog to Digital converter, Digital to Analog converter, gate drives of MOSFETs.

With digital regulation control is implemented, the long and short term output current stability and low current tracking error is largely improved.

THE STRUCTURE OF CORRECTOR MAGNET POWER CONVERTER

The full digital corrector magnet power converter could be roughly divided into six functional blocks: 1) Power regulation and L-C filter, 2) high resolution AD7767 24-bits analogy to digital converter, 3) four channel DA8734 16-bits digital to analogy converter, 4) high performance NI sb-RIO 9606 board controller, 5) DIO control trigger port and 6) USB, RS232, RS485, Ethernet and control page transmission interface. The functional blocks are shown in Fig. 1.

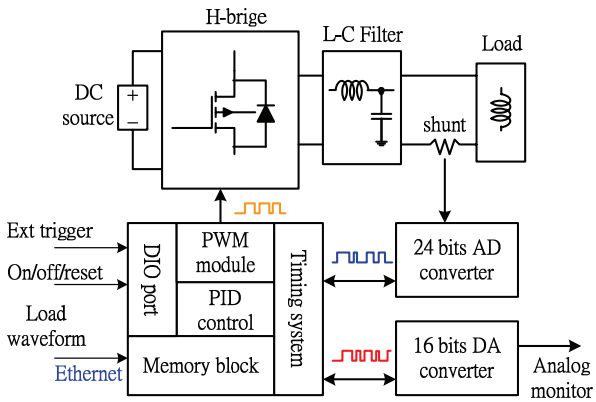

Figure 1: The structure of corrector magnet power converter.

PWM REGULATION METHOD

The PWM computation algorithm is done in the FPGA on the NI sb-RIO 9606 board. The compensated current command output from the PID block is exported to this PWM generation block, where the MOSFET switching signals S1, S2, S3 and S4 are generated by comparing the current command to two saw-tooth waveforms with 180 degree phase difference as illustrated in Fig. 2. It is shown in Fig. 2, the left waveforms are the MOSFET switching waveforms while the current setting is positive, while the waveforms when current is set to negative is depicted in the right [1].

The MOSFET Switch Modes with various load current flow are plotted in Fig. 3. There are 6 modes of load current flow. Mode Ⅰ ~ Ⅲ are positive current flows through the load, while in ModeⅣ~Ⅵ are modes when negative current occurs.

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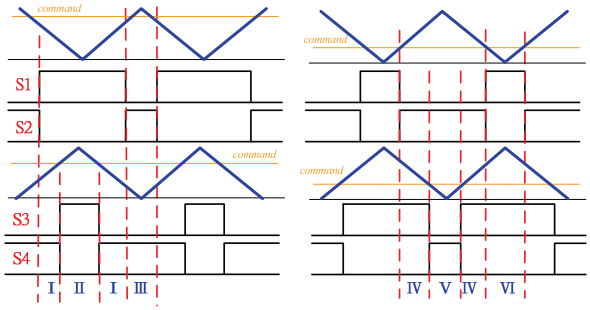

Figure 2: MOSFET switching waveforms.

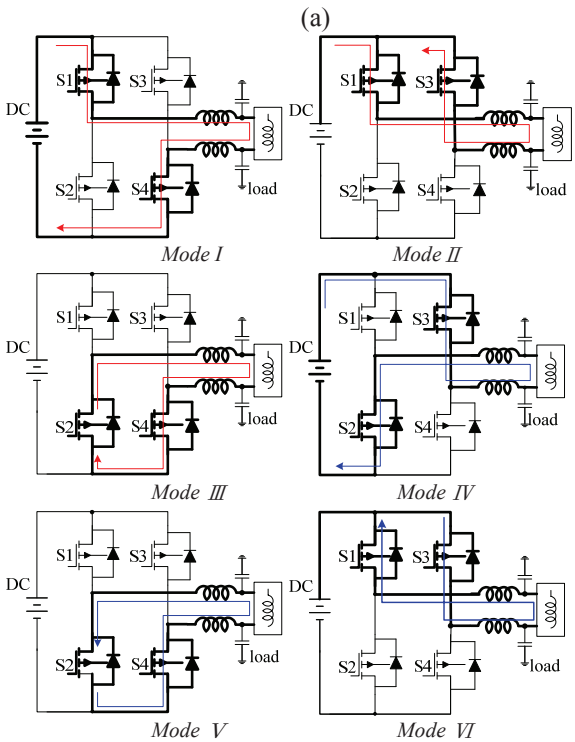

Figure 3: Different MOSFET switch modes.

SIMULINK SIMULATION

To ensure the functional correctness and accuracy of the new control scheme that will be applied to the digital regulation control circuitry, the characteristic of circuitry, the P-I compensator and the PWM regulation algorithm are simulated with MATLAB SUMILINK. Fig. 4(a) is the functional block diagram of power converter circuit for simulation, this diagram includes the full bridge power stage, the output L-C filter, the P-I compensator and PWM regulation blocks.

The block diagram of P-I compensator and PWM regulation are shown in Fig. 4(b), the P-I compensator will generate an error signal, which is proportional to the difference between current command and current feedback signal, import into the PWM block to compare with the 180 degree phase difference triangle carrier signals and the PWM signals are generated and output to drive MOSFET switches.

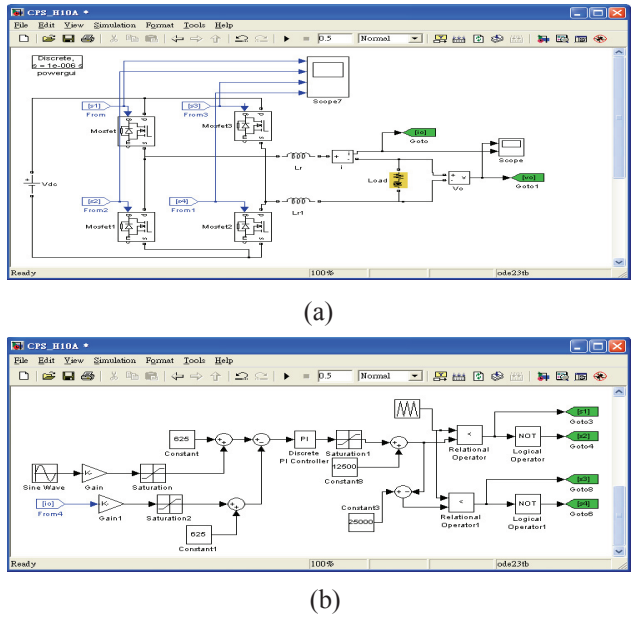

Figure 4: Simulation diagram (a) power converter scheme (b) internal block of compensator.

The zero-crossing performance of CPS is illustrated in Fig. 5. The current command ramps from -0.25 A to +0.25 A and then back -0.25 A for numbers of cycle with small steps. It is observed that the tracking is very accurate and close to current command in red.

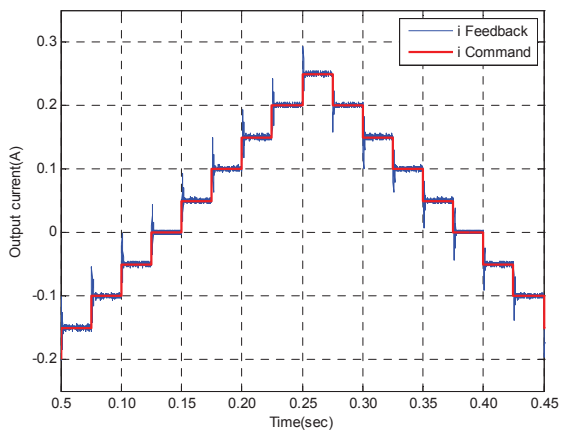

Figure 5: Simulation results around zero.

DATA ACQUISITION INTERFACE

Not only the PI regulation loop and PWM generation are implemented in NI sb-RIO board, to which a DIO board can be attached. The DIO can provide IO pins to or from FPGA to control and access the supporting circuits including 24bit delta-sigma high precision ADC, 16bit DAC and detect converter interlock signals. The SPI timing control signal to communicate with the ADC and DAC respectively is shown in Fig. 6[2].

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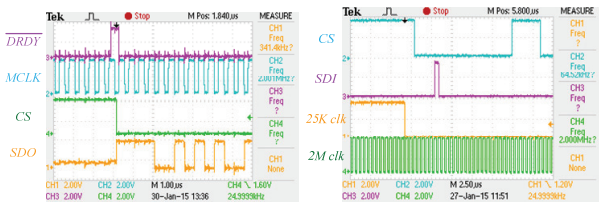


Figure 6: the timing pattern (a) AD7767 EVM (b) DAC 8734 EVM.

EXPERIMENTAL RESULT

Several tests have to be examined to determine the final performance of the full digital regulation implementation: step response, nonlinearity of output current around zero current, long-term stability and re-productivity. .

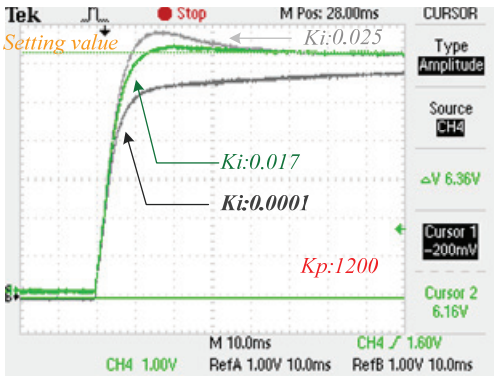
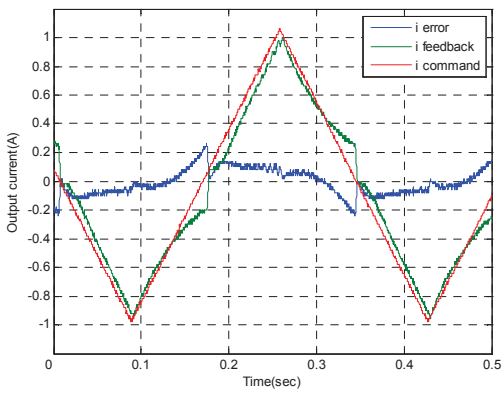


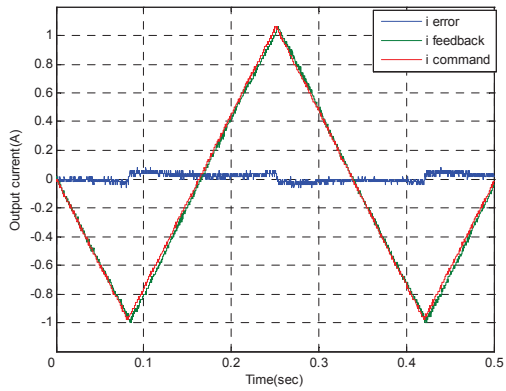
Figure 7: Step responses of the CPS with various PI gain.

The PI parameters can be easily adjusted through a virtual interface developed with NI LABVIEW. Figure 7 shows the various step response curves with different PI gains.

The current output linearity error about the zero point is test and measured as depicted in Fig. 8. The current output linearity error about the zero point of the analogy regulation version is shown in Fig. 8(a), the linearity error can be as large as ±0.25 A. While in Fig. 8(b), by employing the digital regulation and dual phase PWM scheme, output linearity around zero is greatly enhanced and the error is within ±0.02 A, which is about 20 dB improvement.



(a)



(b)

Figure 8: Output linearity error around zero.

The long term current output stability is also measured to test if the ripple can stay stable within 10 ppm as required. The output current drift of the corrector magnet power converter within 16 hours is shown in Fig. 9. The stability is well within the 10 ppm criteria.

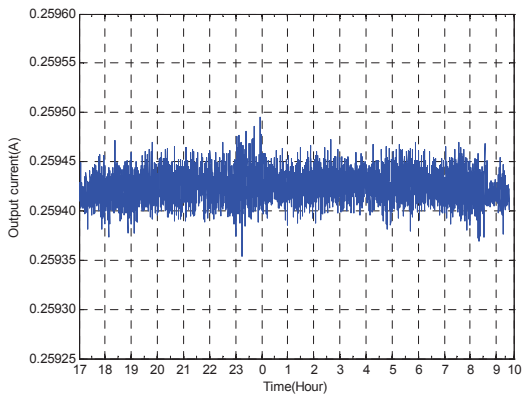


Figure 9: Stability of output current within 16 hours.

CONCLUSION

With digital regulation control implemented as shown in this presentation, the long and short term output current stability and ripple are well controlled within ±10 ppm, satisfying the specification requirement of TPS sextuple and corrector magnet power supply.

The digital control method has been proven to exhibit better performance of output current and the current tracking error at low output current is greatly reduced.

This full-digital power converter architecture will later be employed in the near future for all the power converters in the TPS ring for performance upgrade.

REFERENCE

[1] B.S. Wang et al., "Development of Digital Controlled Corrector Magnet Power Converter with A Shunt as A Current Sensing Component", IPAC'12, New Orleans, USA.

[2] http://taiwan.ni.com