UPDATE ON THE DEVELOPMENT OF THE NEW ELECTRONIC INSTRUMENTATION FOR THE LIPAc/IFMIF BEAM POSITION MONITORS*

Angel Guirao[†], David Jimenez-Rey, Luis Miguel Martinez Fresno, Eduardo Molina Marinas, Joaquin Molla, Ivan Podadera, CIEMAT, Madrid, Spain

Ignacio Rivera, UCM/CIEMAT, Madrid, Spain

Abstract

Among all the LIPAc/IFMIF accelerator diagnostics instrumentation, the Beam Position Monitors (BPM's) are a cornerstone for its operation. An electronics system centered on self-calibration and extraction of beam phase information for Time-Of-Flight measurement is proposed for the twenty BPM stations distributed along the accelerator. The system under development is a fully digital instrumentation which incorporates automatic calibration of the monitors' signals and allows monitoring of both fundamental and second signal harmonics. The current state of the development and first experimental results of the system on the test bench will be presented.

INTRODUCTION

The team of the International Fusion Materials Irradiation Facility (IFMIF) prepares the installation and operation of the Linear Prototype Accelerator (LIPAc), which is currently under commissioning in Rokkasho, Japan [1]. An important non-interceptive beam instrumentation for the machine operation is provided by the BPMs diagnostic array system or stations, for beam commissioning and accelerator tuning and operation. It provides to the Central Control System (CCS) the variation of the beam centroid in the transverse plane (position) and the longitudinal plane (phase). A total of 20 BPM stations are distributed on the two transport lines –Medium Energy Beam Transport line (MEBT) and High Energy Beam Transport line (HEBT)-, plus the superconducting accelerating sections (SRF linac) and the essential locations defined by beam dynamic requirements in order to obtain an exhaustive feedback for steering and transporting the beam from the RFQ to the Beam Dump.

However the BPM stations located at the Diagnostics Plate will be committed to carrying out energy measurements inside HEBT as well, and not only beam position, as such information is crucial for the tuning of the cavities and a proper validation and characterization of the output beam in each beam commissioning stage. The energy is measured through phase measurement in order to extract the Time-Of-Flight (TOF) estimation for beam dynamics. In the previous years a series of evaluation on commercial options and a prototype for the electronics based on analog processing

were evaluated [2] and the decision to undertake a custom design was promoted.

BEAM POSITION MONITOR ELECTRONICS

The current prototype for the electronic system is based on the CompactPCI (cPCI) architecture. The BPM system is integrated into the EPICS control system of the accelerator facility via Ethernet and the EPICS Channel Access, and the position and phase information is sent to the CCS updated at a rate of 2 Hz approximately. Likewise, it is required to make a database system based on EPICS Channel Access in order to save the most recent position and phase information at a rate of 0.5 Hz [3].

The BPMs requirements during the accelerator operation are summarized in Table 1.

Table 1: Main LIPAc BPM Parameters

Parameter	Value
Beam Parameters	
Beam energy	5 MeV..9 MeV
Beam current	90 mA..126 mA
RF pulse width	200 μs..CW
Duty cycle	0.1 %..100 %
Resolution and precision requirements	
Position resolution	10 μm
Position accuracy (ABS)	100 μm
Phase resolution	0.3 deg
Phase precision (ABS)	2 deg
Signal levels at the Front-End electronics input	
Max. input power	22 dBm
Required Input dynamic range	50 dB

General Layout

The full system is estimated to comprise of two cPCI racks [4], mounting a variety of boards as depicted in Fig. 1.

The current prototype, designed to demonstrate operation and provide service to the Medium Energy transport line (MEBT), sports the following hardware:

- A Central Processing Unit (CPU) running linux flavour CentOS as Operating System (OS) with kernel 2.6, integrated into the IFMIF control system via EPICS.
- Two Nutaq RF Digitizers [5] with 16 ADC channels of 14-bit with a sampling rate of 100 MHz with an

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on-board Virtex-4SX Field Programmable Gate Array (FPGA).

- Two custom designed analog Front-End boards, performing basic filtering and a direct conversion to a lower frequency intermediate frequency (IF) in the analog domain. This board also reroutes RF signals for self-diagnostics.

- One Clock distribution board, the ADAC-SYNC cPCI also from Nutaq, for distributing the sampling ADC master clock to all the digitizers and the different local oscillator (LO) frequencies for down-conversion to the Front-End cards.

- One RF Switch board for distribution of the self-monitoring and calibration signals to all channels from the diagnostics generator.

- Two Timing cards to buffer and distribute both Trigger and Gate signals from the IFMIF Timing Distribution system.

- A commercial RF signal generator (Rohde&Schwarz SMB100-B) with a high power module and a power lever loop control for accurate self-check and calibration of the electronics.

(a) Digitizer board.

(b) Timing board.

(c) Clock distribution board.

(d) Front-End board.

(e) Calibration signal distribution board.

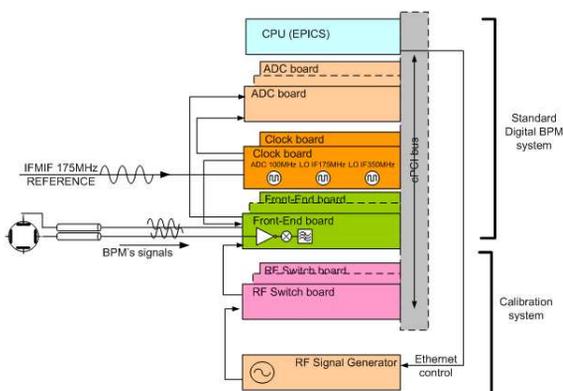Figure 2: Electronic cards comprising the BPM system.

Figure 1: General layout of the BPM electronics.

All other components are custom designed and the system partitioning is such that they can be replaced by equivalent components easily with the only cost of redesign, but without altering their programming nor functionality.

Electronics System

Digitizer   The digitizer is a commercial board from Nutaq (the VHS-ADC, Fig. 2a), with a total number of 16 ADC channels of 14-bit sampled at 100 MHz, feeding data to an on-board Xilinx Virtex-4SX FPGA.

Each one of these 16 input channels is processed in parallel, as each one is based on a standard software digital receiver (SDR) architecture. The signal is bandpass filtered in the digital domain, and the CORDIC algorithm [6] is used to extract the amplitude and phase for each signal. Even after decimation and averaging, the data output rate is more than needed by the CCS. A detailed post-mortem information is a requirement of the system, all the extra data is stored on

the system's archive and the CCS only receives an averaging of the measurements at the predefined rate.

The main problem with this solution is its obsolescence, low memory available for the post-mortem buffer and also its limited capacity to arrive with more than one external timing signals. The only way is through the custom GPIO connector placed inside the board, forcing the customer to make his own mezzanine board.

Timing board   The Timing board (Fig. 2b) is the simplest of all the cards installed in the rack. It only relays and buffers both Trigger and Gate signals coming from the experiment.

The timing system for LIPAc/IFMIF inherits its main architecture from the J-PARC facility in Japan [7], and to the date no update is foreseen.

A 12 MHz master oscillator is used to derive the Trigger pulses for the accelerator's systems. These pulses are distributed through a low-noise buffer tree to each of the installation stations, one of them the BPM system itself.

6: Beam Instrumentation, Controls, Feedback, and Operational Aspects

T03 - Beam Diagnostics and Instrumentation

The BPM system then relays the Trigger and Gate (Gate follows a similar distribution) to each of the digitizer boards. The BPM timing board also generates a timing slot ID based on the 12 MHz master clock and the trigger signals received, to help in the time stamping of the data in the buffer.

This timing information is relayed to the digitizer board through the custom GPIO connector on the front-pannel, as cPCI has no means of Trigger nor Clock distribution, being this one a serious limitation present in the system.

Clock distribution board   Using as a frequency reference a Rohde&Schwarz SMB100 generator with its high quality oven timebase locked to the accelerator master clock itself, the clock board generates the acquisiton frequency for all the ADCs and the two beats for translating the bands of 175 MHz and 350 MHz to the intermediate frequency (IF). The board is the ADACSync from Nutaq (Fig. 2c), with a phase noise for the first local oscillator (LO) frequency of 155 MHz measured with a Rohde&Schwarz FSW Signal and Spectrum analyzer of -111.8 dBc/Hz. Detailed measurements performed at CIEMAT are shown in Table 2.

Table 2: Phase noise measurements for a generated 155 MHz output with the ADACSync card for CLK0 out Measured with a Rohde Schwarz FSW Analyzer, locked to an external source (Rohde&Schwarz SMB100-B)

Off-set	Value
1.0 kHz	−88.31 dBc/Hz
10.0 kHz	−111.88 dBc/Hz
100.0 kHz	−142.26 dBc/Hz
1.0 MHz	−159.78 dBc/Hz
10.0 MHz	−163.81 dBc/Hz

The measurement conditions are equivalent to those to be installed in LIPAc/IFMIF: The SMB100 generator, equiped with an high-stability oven is locked to a very high stability reference, and the ADACSync is feeded from the SMB100 reference output.

The card has also an optional GSP Pulse-per-second (PPS) input which may improve phase-noise even further.

Calibration board   This card is of custom design (Fig. 2e). It implements the switching of the calibration signal coming from the level-controlled RF signal generator to any of the Front-End boards for rerouting the signal either to the cables for failure detection or injection of a known calibrated signal to the digitizer.

This allows to inject a RF tone controlled in frequency and amplitude into the electronics chain. The self-calibration routine measures for each setting point of the Front-End and the digitizer amplifiers the response, calibrating each channel automatically.

It is capable of hot-switching the signal in less than 200 ns (real) for a maximum RF power of 32 dBm, with an insertion loss of -8.28 dB at 175 MHz and -8.71 dB at 350 MHz (Fig. 3) for each of the 16 available outputs.
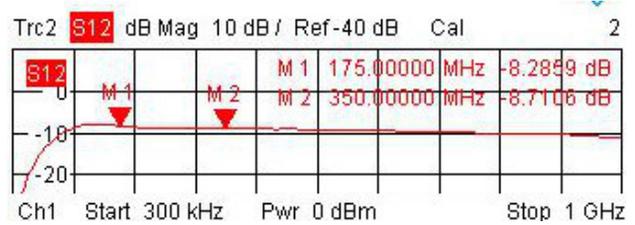

Figure 3: |S21| response of the switching board, for any channel.

The card also has a front-end connector to synchronize it with the timing board and program the switching accordingly to the Trigger operation.

As the integration with the accelerator requires a complete characterization of the system, a full Automated Test Equipment (ATE) system is already integrated through this card.

Each of the RF channels can be measured and characterized with an stimuli of the corresponding RF signal to get the table of correct gains for the front-end boards, along with an error analysis, at any time.

Front-End board   The Front-End card is the most complex of all the custom designed electronics (Fig. 2d). It packs together eight RF paths -two complete BPM stations- in a single 6U card.

Each channel has a set of RF switches to inject a calibrated signal into the BPM buttons for isolation and cable failure tests or into the electronic path in order to detect problems or calibrate the digitizer automatically, even with the accelerator on-line. These procedures are described in depth in [4].

The signal path has digitally programmable gains prior and after the mixing stage. In order to reduce intermodulation noise, the LO spine arriving in LVDS from the Clock card is buffered and filtered low-pass with an independent gain control per channel, so the heterodynation is done at maximum LO power with minimum harmonics. LO leakage is also addressed with a programmable attenuator before the mixer.

The Intermediate Frequency (IF) is arbitrary placed at 22 MHz, and a low distortion, constant impedance filter is placed after the mixer, although this configuration makes that its bandpass region is too wide and smooth. Its presence helps to equalize the impedance more than filtering, being this function addressed by the digital processing on the digitizer card.

In order to allow for versatility, both LO inputs for the 175 MHz and 350 MHz bands are injected into the card, and the LO source selection is controlled via software. The on-board FPGA performs a function of frequency counting to check that the selected LO source is the proper one.

A detailed look of the RF channel can be seen in Fig. 4. Each one of the channels is isolated with a trench of grounded vias to guarantee minimum noise and is independently powered with its own filtered power rail.
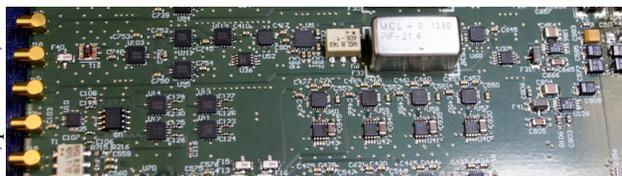
Figure 4: Detail of RF signal path and local oscillator spine.

The on-board FPGA stores the corrected gain coefficients for the different stages into an on-board flash memory, and thermal drifts are taken into account with a digital thermometer per channel, placed next to the mixer.

In spite of all this, the Front-End card is still nothing more than a single direct conversion with a input band too wide, hence accepting noise at the input. The architecture corresponds to a simpler case to the one presented at [8], where a simple conversion stage feeds the ADC input. Later, the signal is filtered, translated to another IF and demodulated always in the digital domain.

This is why to reduce input noise a previous stage of filter banks for either 175 MHz band-pass, 350 MHz band-pass or full-band (no filter) is introduced after the coaxial lines coming from the accelerator, helping to reduce the input noise to the channel.

Future Work and Conclusions

The successful design of several custom boards based on the cPCI architecture have been carried out with good results on the signal's quality and noise.

A more stable clock source is going to be designed, improving the quality of the system, prior to the manufacturing of all the remaining boards needed for the total 20 BPM stations.

On the software side, a server code allows to perform simple PCI operations (read and write) from TCP. The posterior integration into EPICS will undergo the creation of a socket for each hardware card, as an asyn channel to EPICS.

Integration of the software will allow to automate the measurements to fully characterize the complete BPM system for the 80 channels before shipping the system.

REFERENCES

[1] J. Knaster *et al.*, "IFMIF: overview of the validation activies", Nucl. Fusion 53 (2013) DOI 10.1088/0029-5515/53/11/116001

[2] I. Podadera *et al.*, "Test of the Front-end Electronics and Acquisition System for the LIPAc BPMs", IPAC'11, San Sebastian, Spain, 2011, paper TUPC125, p. 1311

[3] J.M. Carmona *et al.*, IFMIF-EVEDA Beam Instrumentation Detailed Design Report, June 2012, DMS ID 23CQT3.

[4] A. Guirao *et al.*, "Development of the New Electronic Instrumentation for the LIPAc/IFMIF Beam Position Monitors", IBIC'13, Oxford, UK, 2013, paper MOPC12, p. 71.

[5] http://www.nutaq.com

[6] J.E. Volder, "The Cordic Trigonometric Computing Technique", IRE Trans. Elect. Comp., vol. EC-8, No. 3, p. 330 (1959).

[7] F. Tamura, M. Yoshii, J. Chiba, T. Katoh, "Timing System for J-PARC", PAC'05, Knoxville, TN, USA, 2005, paper FPAT071, p. 3853.

[8] H. Tsurumi *et al.*, "Broadband RF Stage Architecture for Software Defined Radio in Handheld Terminal Applications", IEEE Communications Magazine, February 1999, pp. 90-95.