NSLS-II DIGITAL RF CONTROLLER LOGIC AND APPLICATIONS*

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Abstract

The National Synchrotron Light Source II (NSLS-II) accelerator consists of the Storage Ring, the Booster Ring and Linac along with their associated cavities. Given the number, types and variety of functions of these cavities, we sought to limit the logic development effort by reuse of parameterized code on one hardware platform. Currently there are six controllers installed in the NSLS-II system. There are two in the Storage ring, two in the Booster ring, one in the Linac and one in the Master Oscillator Distribution system.

INTRODUCTION

The NSLS-II accelerator consists of the Storage ring, the Booster ring and Linac along with their associated cavities. NSLS-II is committed to the use of digital RF controllers for controlling these cavities. The first generation of the digital RF controller was designed and built at Brookhaven National Laboratory (BNL) and successfully tested at the Canadian Light Source (CLS) [1]. Since that time a second generation controller was built that takes the original hardware, firmware and software and expands on their previous capabilities to make the controller versatile enough to be fielded into multiple NSLS-II subsystems (i.e., Storage ring, Booster ring, etc.). Some of the modifications made in the newest revision of the controller will be briefly described along with examples of its different uses and functions.

HARDWARE MODIFICATIONS

Figure 1 is the block diagram of the latest version of the controller showing its functionality. An explanation of the theory of operation will not be given in this paper as it has been written about in earlier publications [1], [2]. The main attributes of the hardware from the initial design are largely unchanged in this version but there are significant differences in terms of I/O and diagnostic capabilities. See Table 1 for a comparison of I/O capabilities between the original controller and the latest revision. As can be seen in Table 1 there is an increase in the number of opto-isolated and TTL inputs. The increase in inputs gives us the ability to handle more interlock triggers as well as more timing triggers going forward. Additionally, there is a small increase in the number of diagnostic LED indicators. In the latest version, the indicator LEDs are much more flexible because each is driven by a Field Programmable Gate Array (FPGA) pin instead of fixed signals external to the FPGA. Figure 2 illustrates the layout of the I/O on both the front and rear panels of the controller. The added extra I/O flexibility came at a cost, however, in that a second DAC output channel was eliminated, which was available in the original design. This channel was underutilized and was not imperative to the design. The seven channel slow ADC input circuit was scaled down to six channels. The slow DAC output circuit was removed to make room for an RS-232 channel that is used to control a tuner PLC.

Tuner Logic Addition

Tuner logic was developed in this latest revision to control the Storage ring cavity tuners. Located inside the FPGA, the tuner logic takes as its inputs the cavity field phase, the forward channel phase and a user supplied Phase Offset variable and computes an error signal for each tuner to act upon. This error signal is serialized, averaged and sent via the RS232 channel from the controller to the tuner PLC that then controls the tuner motors and moves them to drive that error signal to zero.
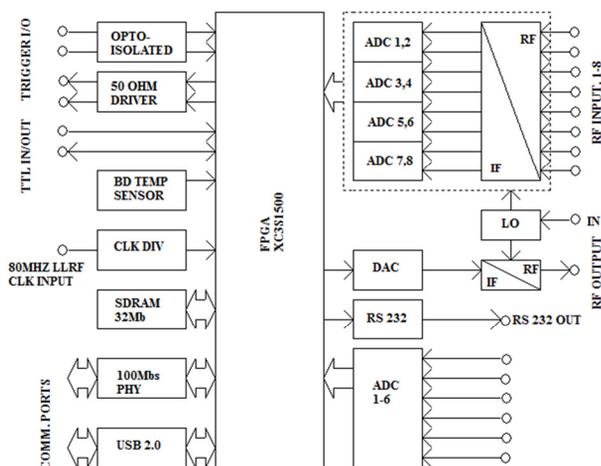

Figure 1: Functional diagram of the revised cavity field controller.

Table 1: Comparison of I/O

I/O Type	Original Rev	Latest Rev
OptoTrig-ins	2	4
TTL inputs	1	4
TTL outputs	3	4
F/P LEDs	6	7

Figure 2: Front and back panels of the cavity field controller.

EPICS INTERFACE

In addition to the hardware modifications, an EPICS interface was developed by the Controls group that allows for high level command of the controller through an EPICS GUI. An important function handled by the EPICS software is the Autoset Loop Phase rotation. This function shifts the loop phase for negative feedback and writes the appropriate settings to the controller before the feedback loop can be closed. In addition, it matches the feedback amplitude and phase set points to those that existed in the feed-forward mode prior to the closing of the loop.

FPGA CODE MODIFICATIONS

With the new controllers given the number, types and variety of cavities that they are to control, modular FPGA code and conditional compilation was used. For example, instantiation of feedback, interlock components and ramp generators are conditional depending on the needs of the RF system towards which the build is targeted.

Common Functions across the Build Types

There are a handful of functions in logic that are universal across the different build types. These functions include ADC signal acquisition, demultiplexing, scope diagnostics and the host interface. These functions can be found in all the builds of the FPGA firmware.

Specific Features of Each of the Build Types

In addition to the common functions that each build contains, there are specific logic functions that are contained only in specific builds. Some of these are described below.

Storage Ring Build The Storage Ring build contains the feedback logic with set-point generation and feedback gain control. It also contains a ramp down logic block that upon detection of an external trip interlock signal input, ramps the fixed field set point to a low enough value to dump the beam. This provides a gentle RF shutoff in response to non-critical trips.

Booster Ring Build In response to a cyclic external trigger, provides a ramped set point output from a feedback ramp table in logic that linearly interpolates between 512 pairs of I/Q waypoints. This table is user modifiable in EPICS and is loaded by block transfers from the host interface.

Linac Build In response to a cyclic external trigger provides a ramped set point output from a feed-forward table in logic that outputs 1024 discrete points. This table

like the feedback ramp table mentioned above is user programmable in EPICS and is loaded by block transfers from the host interface.

Master Oscillator Build This build is loaded into the Master Oscillator controller to make phase corrections to the clock signal driving the injector system in response to thermal phase drifts that occur along the distribution path. The cavity, forward and reverse channels all monitor and report averaged (unlike other builds) values back to the host in order to reduce noise on the phase measurements. The bulk of the Master Oscillator functionality resides in the EPICS high level control software which measures the phase error between the cavity input (returning MO signal) and the fwd input (outgoing MO signal) but only corrects for half the difference of the two since the signal location it is compensating for is at the halfway point of the two monitor pickups. This is done with a PID controller function in the EPICS software.

Due to the many different build code types with many different functional logic block instantiation combinations possible, the firmware logic and host level software are designed to report back to the user the particular build configuration that has been programmed into the FPGA as an aide in the troubleshooting process.

DIAGNOSTIC LOGIC

Circular Buffer

The Opal Kelly daughter board that houses the FPGA also contains a 32Mbyte memory that is continuously written to in a circular fashion. After an event trigger, the memory continues to be written for about half the memory capacity in order to capture data both before and after the event. This maps to a 0.43 second acquisition time. This data can then be imported into the host computer and displayed in a waveform window. Up to five channels of input can be displayed with this diagnostic tool.

Network Analyzer

The network analyser module provides precision measurements of system response functions in logic, including open and closed loop response functions. It generates a direct digital synthesized (DDS) sine wave with 10 Hz resolution for excitation of a system being measured, and performs a Fourier analysis on one or more signals from the system for their response functions from the point of excitation. This function can be chosen to be instantiated or left out through the use of Verilog

compiler directives. The number of network analyser input channels is selectable as well. Currently, the Network Analyzer has four scripted measurements available:

1. Open-loop response: Measures the open-loop response of the controller using a closed-loop measurement.
2. Measuring delays: Measures delay between points that have no other frequency response other than delay.
3. Open-loop delay: Measures the open-loop delay through the proportional–gain branch.
4. Proportional gain plot: Plots proportional gain plots while varying gain and phase on separate plots.

The Network Analyzer can also be used in its manual mode which works then works in similar fashion to an analog network analyser.

EXAMPLE OF CONTROLLER FLEXIBILITY

In addition to its primary use as a cavity field controller, the digital RF controller can be used as an experimental tool as well. A description of how the controller was used to help in the commissioning of the RF Beam Phase Monitor in the Storage ring is described. In order to test the Beam Phase Monitor the cavity field controller was configured with a feed-forward table that modulated the RF cavity phase at the synchrotron frequency (see Figure 3 for the EPICS GUI page). The feed-forward signal was summed to the normal feedback operating point which drives the klystron and subsequently cavity field. Since the feed-forward table is of a fixed number of points (512 I/Q pairs) and must contain an integral number of RF periods in order to be continuous, the modulation frequency cannot be arbitrarily set but will have some offset, usually small (few percent). In order to match the beam response to the modulation frequency the RF voltage can be slightly increased or decreased to match the synchrotron frequency to the modulation frequency.
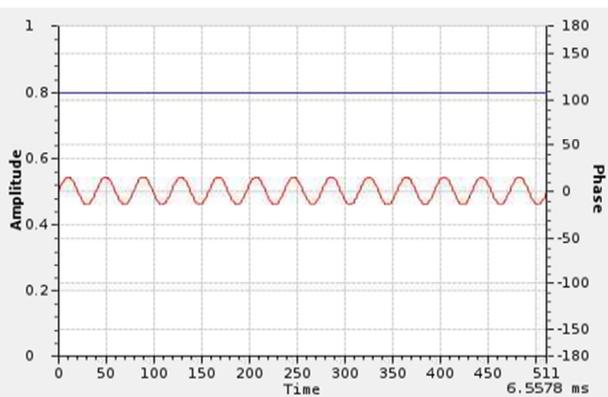

Figure 3: Feed-forward table page showing phase modulation created for this study.
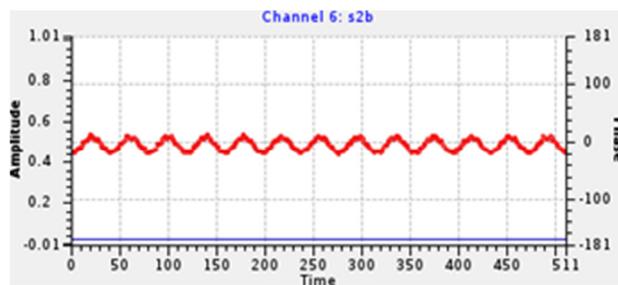

Figure 4: CFC scope trace in EPICS showing phase modulated beam pickup signal at synchrotron frequency.

Figure 5: Picture of modulated beam during study.

Figure 4 shows the phase oscillation on the scope trace of the beam monitor phase output being captured by the controller at the Channel 6 input. A picture of the actual beam can be seen in Figure 5. Note the modulation of the beam that is accomplished during this study.

CONCLUSION

With just minor modifications to the original cavity field controller hardware design, implementing modular code, and making use of Verilog compiler directives during the FPGA code development cycle, a highly versatile, highly expandable cavity field controller capable of handling many different tasks with within the NSLS-II system has been developed.

ACKNOWLEDGMENT

The success of the newest cavity field controller is a result of the entire RF Group as well as Jueri Tagger and the NSLS-II Controls Group. A special appreciation goes out once again to our colleagues at the Canadian Light Source for their support and assistance during testing of the latest version of the controller during a second visit to their facility.

REFERENCES

[1] H. Ma. "The Low-Level Radio Frequency System for Superconducting Cavities of the National Synchrotron Light source II", PAC 2011.
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