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# DESIGN AND TEST OF PROTOTYPE OF LLRF SYSTEM FOR KIPT NEUTRON SOURCE LINAC

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*Abstract*

A 100 MeV/100 kW electron LINAC is being constructed by IHEP, China for the NSC KIPT Neutron Source project in Ukraine [1]. A LLRF system is required to produce the driver RF input of the klystron and maintain the accelerating phase and amplitude stability of the machine. The LLRF system consists of an RF reference distribution system, six identical control units, and the fast RF interlock module. The main part of control unit is the PXI-bus crate implemented with PXI9846 - 4 ADC digitizer board and ICS572 - high speed 2 ADC/2 DAC signal process board. An EPICS IOC based on WinDriver as the PCI device driver is developed and tested. Preliminary results show phase detect resolution of 0.03 degree (rms) of 2856MHz signal has been achieved.

## INTRODUCTION

The 100MeV electron LINAC includes a triode-type gun, a 2856 MHz pre-buncher (PB), a 2856 MHz travelling wave buncher (B) and ten 2856 MHz travelling wave accelerating tubes (A0-A9). The layout of the LINAC is shown in Fig. 1. The pre-buncher, the buncher and the first accelerating tube are powered by one klystron. The second accelerating tube is powered by one single klystron to obtain a higher accelerating gradient. For the following accelerating tubes, each two are powered by one klystron. The Low-Level RF (LLRF) system is needed to control the phase and amplitude of each accelerating sections. The reference signal from master oscillator (MO) is distributed to each LLRF module by phase-stabilized coaxial cables.

## REQUIREMENT ANALYSIS

In order to maintain the stability of the LINAC, the LLRF system must include the following requirements:

- The phase and amplitude stability of the accelerating field are ±2° and ±2% according the beam dynamic analysis [2]. The phase reference signal of each LLRF station must be stabilized.
- The LLRF system should generate drive waveform for the klystron and compensate the beam loading effect.
- The LLRF system should provide signal monitoring and some fast interlock functions such as loss of power protection and reverse power over-limit protection, etc.
- The LLRF system should provide the access point with the control system and the graphic user interface to the operators.

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## SYSTEM DESIGN AND TEST

One typical control unit of the LLRF system is shown in Fig. 2. The hardware can be divided into two parts: the RF front-end module and the data acquisition (DAQ) module. The front-end module includes a frequency generator which provides the LO signal for the down-converters and up-converters as well as the Clock for the DAQ module. The DAQ module consists of three boards: ICS572F, PXI9846 and PXI3950, which are inserted in the same chassis with the PXI-bus connection.

The PXI9846 board from ADLINK has four 16-bit 40MSPS ADCs. It is used to digitize the down-converted IF signals of the forward/reverse signals of the klystrons and the accelerating tubes.

The ICS572F board from GE has two 14-bit 105 MSPS ADCs and two 14-bit 250 MSPS DACs. It is used to generate the drive signal of the klystron, detect the phase and amplitude of the pickup signal and implement PI and feed-forward control algorism in order to maintain the stability of the accelerating field.

The PXI3950 board from ADLINK is an embedded controller with an Intel x86 CPU and runs on the Windows XP 32-bit version operation system. The EPICS IOC which includes the device support of PXI9846 and ICS572F is built on this controller. The records that hold the waveforms of the signals and the control registers of the LLRF system are supported by these devices. So these records can be accessed by any Channel Access tools in EPICS through the Ethernet.

The version of EPICS base is R3.14.12.3 and the EPICS_HOST_ARCH is chose to be cygwin-x86.

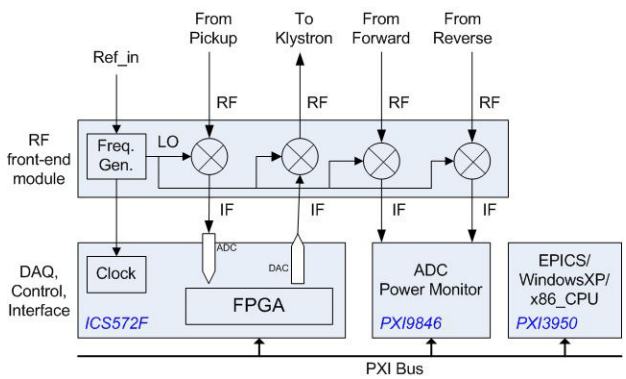


Figure 2: Structure of one LLRF control unit.

### *Data acquisition of PXI9846*

There are two ways getting the samples through PXI9846 board: using task-oriented DAQPilot library or

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using low-level WD-DASK library, both of which are provided by the vendor ADLINK. The method based on DAQPilot library is chosen as it's easier to configure the sampling parameters.

The flow of the process using the API functions [3] is illustrated in Fig. 3. The "PXITask" file is generated by the DAQPilot software tool of ADLINK which includes all the sampling parameters of the board. After getting the handler of the device, we can read the data that the ADCs digitized. This process is added in the PXI9846 device support part in the IOC. Then the waveform record and the calculated power could be read out through the EPICS system.

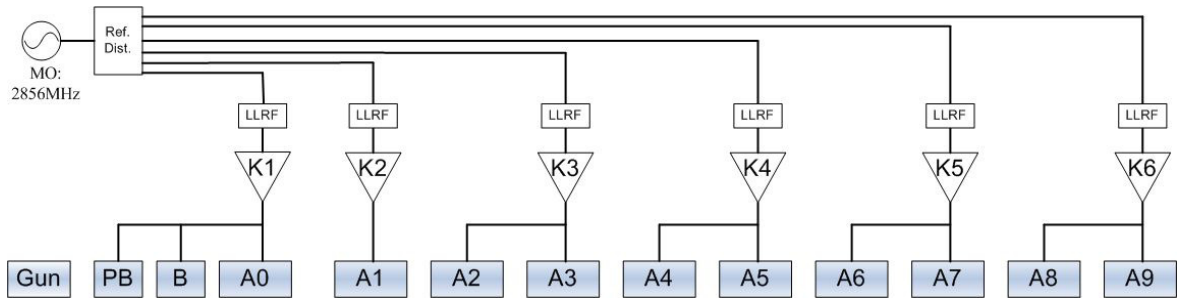


Figure 1: Layout of the LINAC.

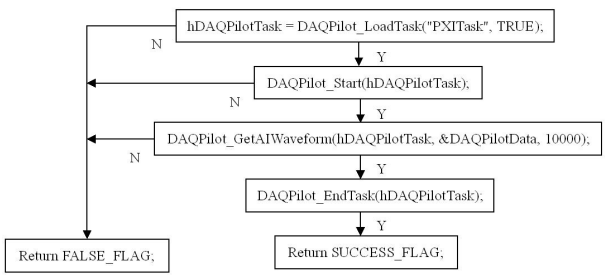


Figure 3: DAQ flow of PXI9846.

## *FPGA process and PCI communication of ICS572F*

The functional blocks in the FPGA are illustrated in Fig. 4. The data from ADCs are demodulated into in-phase (I) and quadrature (Q) components and then transformed into the amplitude and phase components. The errors of amplitude and phase drift are feed into two separated PI controller channels, adjusting the amplitude and phase output of the DAC based on a DDS core. The frequency of the IF signals before the ADC and after the DAC is 23.8 MHz, 1/4 of the clock 95.2 MHz. To produce a defined drive waveform and compensate the beam loading feed-forward (FF) control table shall be added in the data flow.

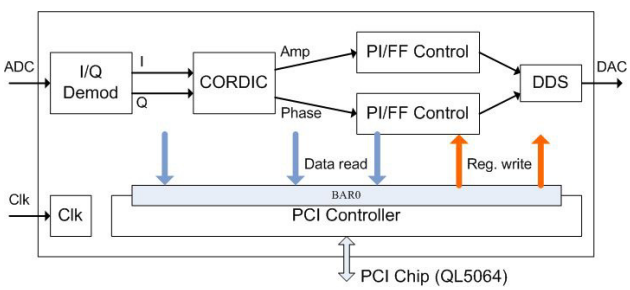


Figure 4: Data process and PCI communication in FPGA.

All the register reading/writing and waveform transfer are through the PCI local bus. The PCI bus interface chip is QL5064 from QuickLogic which can operate in 64-bit 66 MHz mode at rate up to 528 MBytes/s when enabling DMA transfer [4]. A PCI controller module is designed for the QL5064 in the FPGA while the read and write registers in the FPGA are mapped into the BAR0 of the QL5064.

It takes more effort to write the device driver of PCI bus in Windows than in Linux platform. One solution is using Windows Driver Development Kit (DDK) provided by Microsoft. However it would take a long time writing the stable and effective drivers especially for the developers who are not familiar with driver structure of Windows XP operation system. Another more preferable solution is applying the WinDriver [5] software package from Jungo Connectivity. WinDriver enables the developer a very fast and stable development of PCI bus without knowing much about the kernel level of the OS. It is chosen as the solution of the PCI driver of ICS572F running on Windows XP.

An INF file and a DLL file that the device driver needs are generated from the WinDriver software. After installation of the driver, the PCI bus device can be accessed by some simple API functions provided by WinDriver. The function flow of the data transfer is illustrated in Fig. 5. The device initiation functions are placed in the initiation part of the device support in the IOC while the data transfer function is inserted in the read and write part of the device support respectively according to different control words.

The driver created with WinDriver can be built and run for cross-platform like WIN32/UNIX/VxWorks only except Cygwin. Therefore, when the WinDriver is compiled with EPICS base on Windows XP OS and EPICS_HOST_ARCH is set to be cygwin-x86, the IOC compiler (GCC/G++) default macro definition of OP_SYS_CPPFLAGS += -DUNIX should be deleted to make sure the compiler compile the WinDriver driver for WIN32 rather than UNIX.

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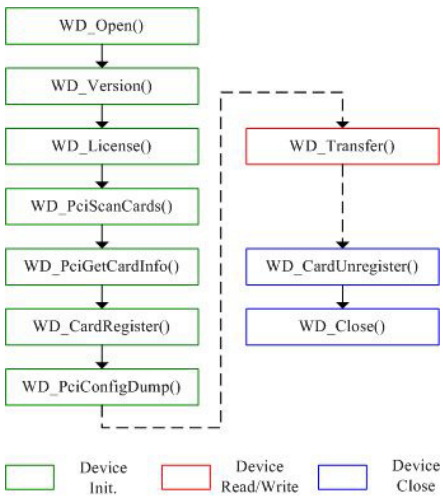


Figure 5: Software flow of data transfer in WinDriver.

## RESULT

The resolution of phase and amplitude detection can be achieved using the setup in Fig. 2 when connecting a RF signal that phase synchronized with the reference signal. An IOC including device supports of both PXI9846 and ICS572F is built. The waveform of the forward and reverse signals can be captured in the PXI9846 record of the IOC. The phase and amplitude of the pickup signal can be read out by registers through PCI bus which are shown in Fig. 6 and Fig. 7. The resolution results are ±0.1° (0.03° rms) in phase and ±0.3% (0.1% rms)in amplitude.

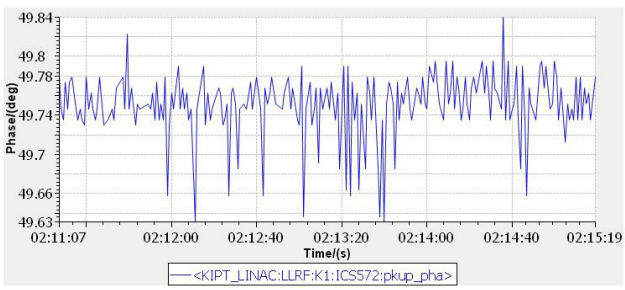


Figure 6: Phase detection by ICS572F board.

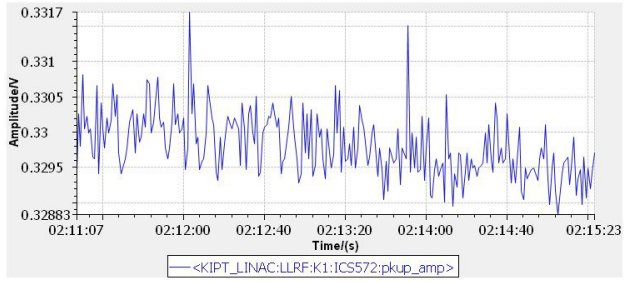


Figure 7: Amplitude detection by ICS572F board.

## CONCLUSION

A digital LLRF system is designed for the KIPT LINAC. The reference distribution system has been installed for six LLRF control stations. The hardware of the LLRF system has been set up. In the FPGA of the ICS572F board, the phase and amplitude of the pickup signal are calculated. The PCI bus controller is developed in the FPGA and the device driver of the PCI bus is written based on WinDriver. An EPICS IOC including PXI9846 and ICS572 boards control codes is completed and run on the Window XP. All the needed records that communicate with the boards can be accessed in the IOC. This prototype of LLRF system can be used for the LINAC control.

Further work includes DAC drive signal output of ICS572F and system integration. Although the WinDriver is adopted for the PCI driver, it is commercial software and not open source, so other solutions shall be studied. The feed-forward algorism is about to be evaluated when the LINAC starts to operate.

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