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DEVELOPMENT OF A 9 MHz 15 kW SOLID-STATE CW AMPLIFIER FOR RHIC

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Abstract

This paper describes the technical details of the development of a high-power solid-state amplifier for Brookhaven Laboratory. The amplifier must withstand short duration events of 100% full-power reflection, and also must guarantee delivery of continuous power into any load impedance at any angle.

INTRODUCTION

This paper describes some of the technical considerations in the design of a 9MHz 15kW CW amplifier for use in RHIC at Brookhaven National Laboratory (BNL). A total of six of these 15kW amplifiers will be commissioned, driving "gap cap" cavities [1].

The amplifier uses modular solid-state architecture and 6th Generation LDMOS power transistors. In the 15kW system, six 2.5kW amplifier units are combined via a 6:1 combiner unit to give a single 15kW output. The RF amplifier rack is located within the accelerator tunnel close to the cavity, and the associated switchmode DC power supply is located remotely to minimise the risk of damage due to ionizing radiation. A failsafe opto-isolated interlock link was designed to accommodate this requirement. The amplifier system has extensive control and monitoring functions and is equipped with three different control interfaces: it can be controlled locally via front panel push-buttons, or remotely via a wired parallel (PLC) interface or an Ethernet connection.

DESIGN CONSIDERATIONS

The major specifications of the amplifier are listed in Table 1. The requirement for the amplifier to supply significant amounts of forward power to mismatched loads presented a number of design challenges: Since circulators are not an option at 9MHz, the amplifier had to be capable of withstanding the mismatch in its own right, while remaining stable and well behaved under all load conditions.

To meet these specifications several key design factors had to be simultaneously optimised, namely: forward power, thermal management, stability, and parts count.

Forward Power

As a first approximation, the maximum power that a push-pull transistor pair can produce is limited to $2V_{dc}^2/R_L$, where V_{dc} is the DC supply voltage (fixed at 50 volts), and R_L is the load resistance presented across the transistor drains. Thus, if R_L is very large it becomes impossible to achieve the required output power. At the other extreme, if R_L is very small the available output power becomes very large, but as described later, there is a risk of destroying the device due to excessive die temperature. The various measures that were taken to address this issue are described in the following paragraphs.

Table 1: Basic Specifications

Frequency	9MHz ±10% minimum							
Power	15kW CW minimum							
Gain/phase Linearity	±1dB maximum and ±10° maximum from 15W to 15kW output							
Harmonics	<-30dBc at rated power							
Stability	Unconditionally stable over entire load space and dynamic range							
Forward power at worst-case phase	SWR	1	1.5	2	3	5	10	∞
	kW (min.)	15	15	12	9	6	4.5	3
Load transients	Withstands 100% reflection at full rated power for at least 100µs							

Thermal Management

Reflected power acts to disrupt the operating point of the transistor and affect its efficiency. For example, it can result in a very low impedance load being presented to the transistor, forcing the transistor to carry high current whilst simultaneously having a large voltage across it. This results in very high heat dissipation in the silicon die, which unless properly managed can lead to overheating and permanent destruction of the transistor. Safe operation hinges on minimising the thermal resistance between the power transistor and the cooling water. Therefore, a great deal of care was taken in the mechanical design to ensure a very low thermal resistance and a solid electrical connection from the flange to the earth.

Stability

Since the amplifier is required to operate into all phase angles of any possible VSWR, there is significant potential for amplifier instability. There is also a risk of that circuit elements might form high Q resonances with the load reactance. This can produce large gain variations and possible oscillations if any suitable feedback path exists. It can also result in damage to components such as harmonic filter capacitors or coupling capacitors.

Parts Count

In order to maximize the expected MTBF of the system, every effort was made to minimise the parts

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count, where this did not unacceptably increase component stress. Therefore, rather than building each PA module around an individual push-pull 1.25kW transistor, a pair of such transistors was used, with the two devices in each package connected in parallel. This halves the total number of peripheral components required, including balun transformers, matching and coupling capacitors, bias circuitry and DC supply filtering.

PA Design

A block diagram illustrating the main parts of the PA module is shown in Figure 1. Four of these PA modules are used in each 2.5kW amplifier unit, and six amplifier units are used in the 15kW system.

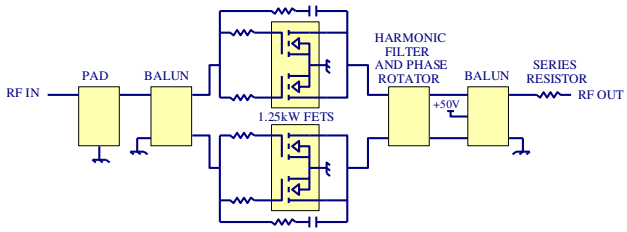


Figure 1: PA module block diagram.

Variations in the load impedance lead to corresponding variations in the linearity and gain of the amplifier. In order to make the amplifier as "well behaved" as possible, several measures were taken to minimise these effects. A small amount of shunt feedback was included from drain to gate on each device to improve stability, reduce the input impedance variation, and to help keep the gain constant as the drain load varies. To further reduce the input impedance variation and improve stability, a 5dB pad was included on the input of each module.

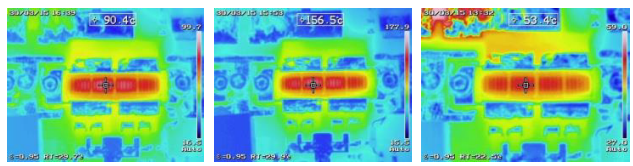
The loading of the harmonic components of the drain waveform plays an important role in determining the efficiency and output power of a solid-state amplifier [2]. Therefore, a balanced L-C filter network was included directly in the drain path of the PA output. This network provides a relatively constant reflection coefficient for the harmonic components of the voltage and current waveforms despite the variable load impedance, and also comfortably achieves the output harmonic specification of -30dBc. The network also provides the optimum phase rotation between the transistors and the series resistor at the output of the PA.

The output of this balanced filter passes through a coaxial isolating balun transformer, and then through a high-power series resistor. This resistor, along with the transformation and rotation that occurs in the filter network, modifies the range of possible load impedances that can appear on the drains of the transistors. Selection of the optimum values for the series resistor and the filter and tuning components involved extensive iteration between the computer models and actual measurements on the amplifier prototype. The eventual result was a design that can comfortably deliver the specified power to any load while neither saturating nor overheating.

The series resistor also serves to eliminate the risk of damage to the harmonic filter components by safely limiting the Q of any resonances that might occur between them and reactive load impedances.

Thermal Performance

The images below show thermal measurements on a PA with the ceramic lid removed from one of its transistors. The transistor was coated with a material with known emissivity so that the temperature of the silicon die can be directly measured. In each case, the PA is delivering 420W of forward power. The 3:1 conditions represent some of the worst-case extremes for achieving the required power level into the high impedance end of the load space, whilst maintaining a safe die temperature at the low impedance end.



50 ohm load. Die temp 90C. | 3:1 low Z load. Die temp 156C. | 3:1 high Z load. Die temp 53C.

Figure 2: Transistor thermal images.

VSWR Protection System

The VSWR protection in solid-state amplifiers often consists of a simple reflected power limiter. If the reflected power reaches the limit value the gain of the amplifier is reduced to prevent it rising any higher. However for this particular amplifier, the requirements are slightly more complicated, as the reflected power limit ranges from 600W into 1.5:1 VSWR up to 3000W into infinite mismatch. Thus, for any given forward power level there is a minimum permissible reflected power level. As shown in Figure 3, an analogue computation circuit was designed to produce a second-order polynomial approximation of this reflected power profile. The protection circuit measures the forward power and calculates the corresponding reflected power limit for that particular power level. The use of an analogue computation circuit avoided the possibility of steps, hysteresis or discontinuities in the amplifier's gain under mismatched conditions.

In addition to its continuous reflected power handling, the amplifier must also provide uninterrupted operation through events such as cavity discharges that may result in transient bursts of 100% reflection at full power. All components, from the transistors through to the RF output, were therefore designed to withstand such events. A time constant in the mismatch protection feedback loop allows up to 100µs of full-power reflection before the reflected power limiter begins to reduce the gain. This was tested by pulsing the amplifier at full power into infinite mismatch at all angles. A typical forward power response is shown in Figure 4, with approximately 200 µs delay before the protection activates.

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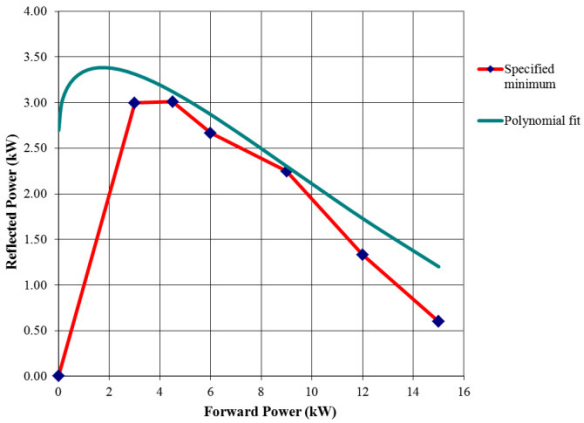

Figure 3: Reflected power limit and polynomial fit.

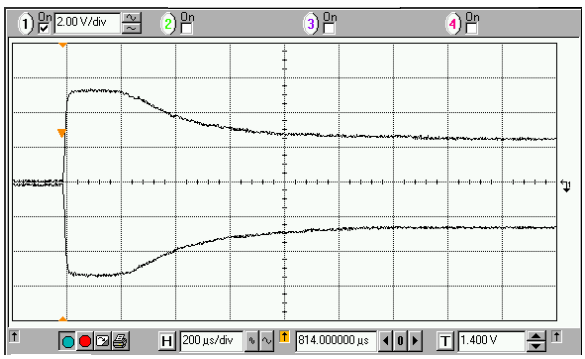

Figure 4: Transient reflection response.

Output Combiners

Since the load can be of any impedance, including purely reactive, all of the combiner and coupler stages after the PA modules are realised in high-power coaxial cable rather than lumped L-C elements. This avoids the possibility of component destruction due to high-Q resonances between circuit elements and reactive loads. The combiners (4:1 in each amplifier unit and 6:1 in the final combiner unit) use a Wilkinson topology, with ferrite loaded impedance transformers wound with ultra-low loss coax. They are designed to withstand any combination of worst-case partial failure modes and worst-case load mismatches indefinitely. Dual directional couplers, using the voltage and current sampling method, are incorporated into the main combiner structure.

Amplifier Tests

In order to test the amplifier over the entire load space, a high-power 4-bit binary phase shifter was constructed, allowing the angle of the reflection coefficient to be stepped in 22.5° increments through one full rotation. This was followed by a variable mismatch, consisting of a coaxial stub in parallel with the 50Ω dummy load, which allowed the VSWR to be set to 1:1. 1.5:1, 2:1, 3:1, 5:1 or 10:1. For the infinite VSWR case the 50Ω load was replaced with a short-circuit.

The measured variation in amplifier gain at one-tenth power, under the full range of load conditions is shown in Figure 5. Gain and phase linearity into a 50Ω load, over a 30dB range up to 15kW, is shown in Figure 6.

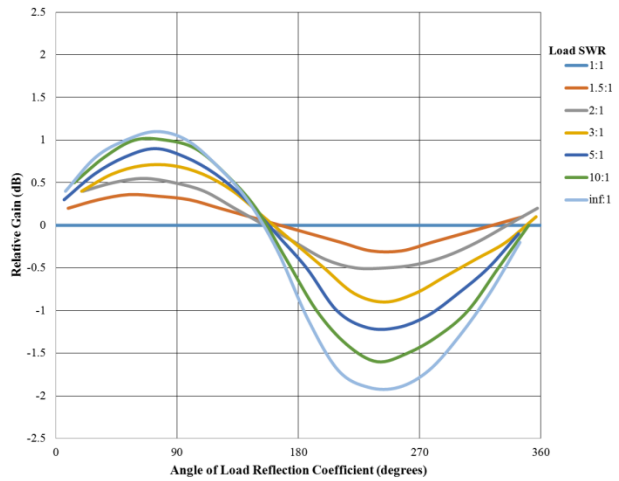

Figure 5: Effect of load VSWR and angle on gain.

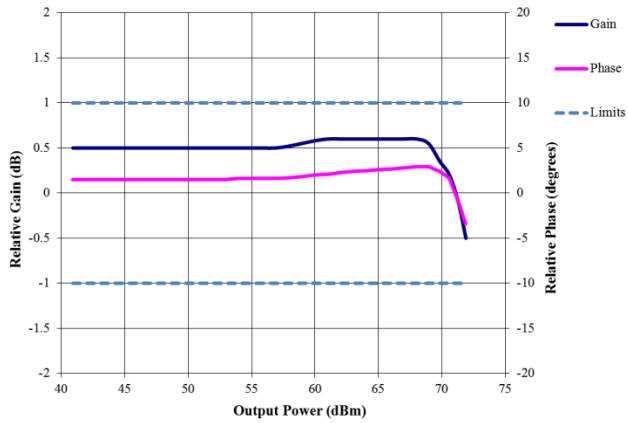

Figure 6: Gain and phase linearity up to 15kW.

CONCLUSION

A solid-state 9MHz 15kW CW amplifier which meets or exceeds requirements over its full specified range of load conditions has been successfully designed and tested.

ACKNOWLEDGMENT

Thanks to Salvatore Polizzo at BNL for his valuable insights during the preparation of this paper.

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[2] Francisco Javier Ortega Gonzalez et al, “Effects of Matching on RF Power Amplifier Efficiency and Output Power”, Microwave Journal, April 1998.