DESIGN OF THE RF SYSTEM FOR THE ACCELERATOR COMPLEX OF RARE ISOTOPE SCIENCE PROJECT*

J. Han, C.K. Hwang, O.R. Choi and J.W. Kim[#], IBS, Daejeon, Korea

Abstract

The rare isotope beam facility planned in Korea will utilize a superconducting linear accelerator to accelerate heavy-ion primary beams, in which an RFO accelerator in the injection line and superconducting cavities are to be powered by rf power amplifiers. The rf amplifier system is based on solid state device for superconducting cavities, and a tetrode tube for the final stage of rf amplifier chain of the RFQ. A 2 kW system was built as a unit and tested with dummy load. A combiner to combine four units is being tested. An LLRF system to control the amplitude and phase of RF fields, which was built for normal-conducting quarter-wave resonator, has been modified to control a superconducting cavity. We plan to test the LLRF system in established superconducting RF facility abroad before being used for a prototype superconducting cavity under fabrication.

INTRODUCTION

A rare isotope beam facility has been designed under the rare isotope science project (RISP) in Korea from the end of 2011. A superconducting linear accelerator is the main driver to produce rare isotope beams using the inflight fragmentation method [1]. ISOL method will be also used with a 70-MeV proton cyclotron. A post accelerator to accelerate isotope beam, which is produced and selected using the ISOL method, is a superconducting linac similar to the front part of the driver linac.

Highly-charged heavy ion beams are produced by an ECR ion source, and then accelerated by an RFQ before the beam being injected into the superconducting linear accelerator. Figure 1 shows a schematic diagram of the RF system for the superconducting cavities and normal conducting cavity of the RFQ. Each RF amplifier is controlled by a low level RF control (LLRF) system. We have developed solid state power amplifiers for the superconducting cavities in collaboration with domestic companies. A prototype LLRF system was studied using a normal conducting quarter wave resonator, and we plan to test an upgraded system at a superconducting rf laboratory abroad to study its performance.



Figure 1: Scheme of the RF system along the accelerator chain. The lower part shows the post linear accelerator for acceleration of isotope beams in low current.

The rf frequency of the low-energy section with the RFQ and the QWR is 81.25 MHz, and it is doubled to 162.5 MHz for the HWR, and increased to 325 MHz for the SSR1&2. The maximum rf power requested for each type of cavity is shown also in Fig. 1. The RFQ, which uses normal conducting cavity, needs maximum rf power of 150 kW.

The stability of rf fields has to be within $\pm 1\%$ in amplitude and $\pm 1^{\circ}$ in phase. Considering that superconducting rf cavity is sensitive to various perturbations like mechanical vibrations and Lorentz force detuning, test of a prototype cavity in connection with the LLRF system is a major upcoming task for the RISP.

SOLID STATE AMPLIFIER

The rf amplifier chosen for the QWR, which has a resonance frequency of 81.25 MHz, is solid state power amplifier (SSPA). Figure 2 is a schematic diagram of the RF amplifier. To produce the power of 2 kW, two modules of 1 kW SSPA are combined, and another 2-way combiner is used to generate 4 kW. Isolator is needed for the SSPA for protection from reflected rf power from the cavity.



^{*}Work supported by Rare Isotope Science Program (RISP) through the National Research Foundation of Korea (NRF) funded by Ministry of Science, ICT and Future Planning (MSIP) (2011-0032011). #jwkim@ibs.re.kr

ISBN 978-3-95450-122-9

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Design of 1 kW SSPA Module

The 1-kW module is based on a MOSFET transistor. Figure 3 is a circuit diagram of the 1 kW SSPA. For optimized design, simulation was performed using the ADS code [2]. Figure 4 shows variation of RF power gain as a function of the power output. The maximum gain of 29.8 dB is obtained at of an rf power of 55 dBm.



Figure 3: Circuit diagram of the 1 kW SSPA.



Figure 4: RF power gain versus RF power output calculated by using ADS.

Figure 5 shows test setup of 1 kW SSPA module. The driver supplies 1 W of RF power. Transistor of 1 kW SSPA is designed to use a 50 V power supply. Figure 6 shows measurement results of the RF output power versus gain factor. The gain factor is about 25 dB at 40 dBm, and maximum gain is 30 dB between 52 dBm and 60 dBm of the RF output. In comparison with simulation, measurement does not show the peak of power gain near 55 dBm, but the value is not far different.



Figure 5: Test setup for 1 kW SSPA module.

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Figure 6: RF power gain versus output RF power measured.

The 2-kW SSPA is built with a combiner, which is designed by Wilkinson method. As shown in Fig. 7, 2 kW (63 dBm) at 81.25 MHz was measured on spectrum analyzer. We plan to test a 4 kW SSPA soon by combining two units of 2 kW SSPA.



Figure 7: RF power of 2 kW at 81.25 MHz measured on spectrum analyzer.

RF SYSTEM FOR RFQ

RFQ cavity in the injection line of the superconducting cavity will need maximum RF power of 150 kW in cw at 81.25 MHz. The amplifier will use a high power tetrode in its final amplifier stage as shown in Fig. 8. At the intermediate stage, we plan to use an SSPA or triode in the power output range of 8-20 kW. Currently we plan to test both the SSPA and a vacuum tube for a prototype RFQ system, which will need a maximum power of 15 kW. The final amplifier system will be decided based on test results of the prototype.



Figure 8: A schematic layout of the RF system for the RFQ.

LLRF SYSTEM

A digital LLRF system using a field programmable gate array (FFAG) was fabricated and tested using a normal conducting quarter-wave resonator having resonance frequency of around 88 MHz [3]. The phase stability of approximately $\pm 1^{\circ}$ and amplitude stability less than $\pm 1\%$ was aimed. The ADC used has resolution of 12 bits for this prototype system. The phase control was better than the aimed value, but amplitude control was limited by the ADC resolution.



Figure 9: Block diagram of the LLRF system.

Figure 9 shows a block diagram of newly designed LLRF system. The RF input has four identical channels, and consists of a preamp, a band-pass filter and a16-bit ADC. This ADC has sampling rate higher than 120 MHz. The band-pass filter in front of the ADC is to reduce noise.

Calculations of magnitude and phase errors using the output signals of the ADC are performed in the FPGA.

The RF output signal is generated through the FPGA, DAC, IQ modulator and a low-power RF amplifier. IQ values calculated in the FPGA are fed to respective DAC channels. The resulting control signal is given to IQ modulator, and finally to a low-power RF amplifier.

There are five channels of low-frequency output in the LLRF system to drive the cavity tuners and other devices. Each channel has one DAC with sampling rate of 100 kHz and one audio frequency amplifier of about 5 W.

A special chip may be used to minimize jittering of the clock signal from the ADC. The ADC clock signal will be given by external reference signal, which is also one of the RF input signals. In the FPGA, the magnitude is calculated in dB referenced conveniently to a certain level and the phase is computed in degree. The resolution and working range is 0.004 dB and 20 dB in amplitude, respectively, and 0.5° and 360° in phase.

SUMMARY

A solid state power amplifier with the RF output of 1 kW at 81.25 MHz was designed and fabricated as a module. Then 2-kW system using a 2 way combiner was assembled as a unit component in 19-inch rack. We plan to test 4-16 kW SSPA's using a chain of RF combiner for powering up a prototype RFQ cavity, which will need a maximum power of 15 kW. A new LLRF board based on FPGA was designed and fabricated to be tested using a superconducting cavity. The phase and amplitude control of the LLRF system will be studied in established superconducting RF test facility. Then further upgrade both in hardware and software will be implemented.

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