# ULTRA-FAST DATA ACQUISITION SYSTEM FOR COHERENT SYNCHROTRON RADIATION BASED ON SUPERCONDUCTING TERAHERTZ DETECTORS

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*Abstract*

This paper describes a new real-time and high accuracy data acquisition system suitable for recording of the individual ultra-short pulses generated by a fast terahertz (THz) detector (e.g. YBCO, NbN, Zero Biased Schottky Diode). The system proposed consists of a fast pulse sampling board and a high data throughput readout board. The first board is designed for sampling of the fast pulse signals with a full width half maximum (FWHM) between few tens to hundred picoseconds. For each THz pulse four samples are acquired with a minimum sampling time of 3 ps. The high data throughput board consists of a PCIe - Bus Master DMA architecture used for fast data transfer up to 3 GByte/s. A prototype setup with fast THz detectors and the acquisition system has been successfully tested at the synchrotron ANKA. An overview of the experimental setup and preliminary results with multi-bunch filling pattern will be shown.

## INTRODUCTION

At the synchrotron light source, ANKA, up to 184 RF buckets can be filled with electrons with the distance between two adjacent buckets of 2 ns corresponding to the 500 MHz frequency of the RF system. Since a few years coherent synchrotron radiation (CSR) created from short electron bunches is provided by ANKA [1]. Depending on the bunch current the radiation behavior for CSR is different. At low bunch currents the radiated power is described by a quadratic dependence on bunch current. For bunch currents above a certain threshold, the quadratic dependence breaks down and THz radiation is emitted in bursts of high intensity. Arbitrary filling patterns can be used to study the influence of the interaction of adjacent bunches on the CSR. Variations of the bunch current, the momentum compaction factor, the RF voltage and frequency can be used to scan the parameter space for CSR generation. To detect and study the emission characteristics of CSR in the THz range over multiple revolutions a detector system based on thin Yttrium Barium Copper Oxide (YBCO) superconductor film has been developed [2]. The intrinsic response time of only a few picoseconds resolve signals of individual bunches within a multi-bunch environment.

An ideal data acquisition system for CSR analysis requires two signal processing chains: one is analog-to-digital converter (ADC) for intensity measurement and the other is time-to-digital converter (TDC) with discriminator (e.g., constant fraction discriminator), for accurate time jitter measurement between two consecutive bunches. This possibility can be used for measurement of synchrotron oscillation amplitude and phase of the individual bunches. Waveform sampling is an alternative to simplify the complexity of the DAQ system, and also to improve time resolution. In this paper we present a new pulse sampling architecture operating in a continuous mode for the measuring of individual pulse peak amplitude and the relative pulse time jitter between two consecutive bunches.

## PRINCIPLE OF OPERATION

Available commercial DAQ system or real-time oscilloscopes for high bandwidth (e.g. above 40 GHz) are very expensive and, due to limited internal memory and missing fast readout interfaces, are not suitable for long term bunch-to-bunch CSR measurements. To circumvent these limitations a DAQ architecture for fast and continuous sampling of the individual ultra-short THz pulses has been developed.

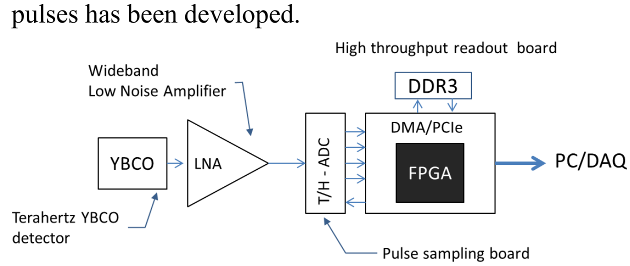


Figure 1: Coherent Synchrotron Emission - experimental station.

The setup used for the CSR analysis is shown in Fig. 1. The ultra-fast THz YBCO thin film detectors operating at cryogenic temperature were developed to resolve picosecond THz pulses. The detector chip is embedded in a high-speed detector block which is equipped with ultra-broadband RF connectors up to 65 GHz [2]. The detector signal is then fed via a 65 GHz semi-rigid cable and vacuum feed-through to a wideband low-noise amplifier (LNA) [2]. A typical YBCO detector response to a single electron bunch after the LNA is shown Fig. 2. The sampling board receives the analog pulse from the LNA and samples it by 4 individual samples as shown in Fig. 2. The sampling architecture consists of four parallel wideband channels each operating at 500 MS/s. Each channel contains a wideband track-and-hold amplifier [3] connected to a 12 bits resolution fast ADC as shown in Fig. 3.

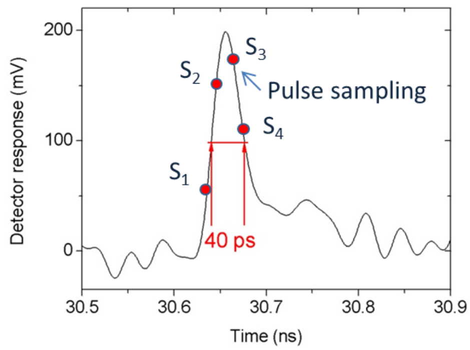

Figure 2: YBCO detector response, the pulse width of 40 ps (FWHM) limited by the LNA.

In the architecture proposed, a clean jitter phase locked loop (PLL) is used to generate a clock signal with high temporal accuracy. The clock is distributed to the picoseconds delay chips [3] by a low skew and jitter clock fanout. In this way, the track-and-hold chips receive a time controlled sampling signals synchronized with the ANKA RF-clock (resp. bunches time distribution). Each delay chip is individually programmable by field programmable gate array (FPGA) from 3 to 100 ps.

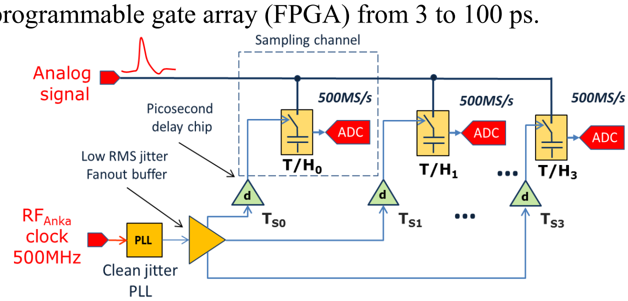

Figure 3: Pulse sampling architecture.

The readout board receives the 4 digital samples all within 2 ns with 12 bits ADC resolution and sends the data acquired directly to the PC/DAQ system. In order to keep a continuous data acquisition the necessary bandwidth is evaluated to be 24 Gb/s (12 bits @ 2 ns * 4 digital samples). Therefore, a high data throughput readout board has been developed at KIT based on a bus master DMA architecture connected to PCI Express end-point logic to ensure high data throughput of up to 2 GByte/s [4]. A new DMA design is on-going and the preliminary test exhibits a throughput up to 4 GByte/s. A large DDR3 memory device, shown in Fig. 1, is employed for a temporary data store before the data transferring to the DAQ system.

## DIGITAL PULSE SAMPLING PROTOTYPE BOARD

A fast pulse sampling prototype board has been developed in order to test some potential critical parts like fast transmission lines, PCB materials and electronics components selected. The board contains a single sampling channel operating at 500 MS/s. The track-and-hold amplifier receives the analog pulse from the output of the LNA and acquires one sample in the peaking time region of each THz pulse (resp. CSR bunch emission). The ANKA input clock signal (500MHz) is delayed by the picosecond delay chip, located on the board, and propagated to the track-and-hold. Every sample is digitized by a fast ADC with 12 bits resolution. The board is connected to the high data throughput board by a fast and high density Samtec connector [5]. The whole setup is shown in Fig. 4.

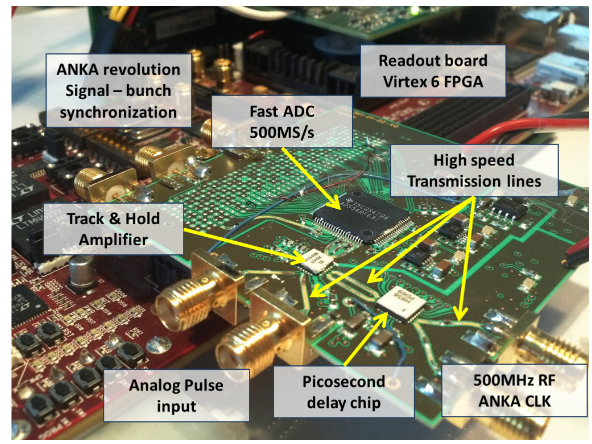

Figure 4: Pulse sampling prototype board connected to high data throughput DAQ.

Both analog and digital signals require a wideband signal propagation and a low noise of both voltage and time levels. Therefore the PCB is made by ROGER 4003 material and the signals are routed by dedicated transmission lines. Well separated analog and digital grounds in conjunction with ad-hoc RF filters located closer at the critical components have been adopted to reduce the influence of the digital circuit on the analog devices. Moreover, the via fences and guard ring techniques have been employed in the PCB layout in order to reduce the cross-talk between adjacent transmission lines, the electromagnetic interference (EMI) and improve the performance at high frequency [6]. A low time jitter is required, which is dependent on deterministic and Gaussian contributions. The deterministic jitter (DJ) depends on the duty cycle distortion, cross-talk, EMI, etc. This component has been drastically reduced by the techniques mentioned before regarding hardware layout techniques, moreover, the residual noise can be measured and corrected in the FPGA. The second contribution is defined as Random jitter (RJ) which corresponds to a randomness of edge deviation occurring in all electronic signals and can be modeled by a Gaussian function. The main contribution of this component is caused by the electronic devices. For this reasons, a low RMS jitter in the range of hundreds of femtoseconds was the main requirement for the components selection. If we assume there is no correlation between devices the total RJ for each sampling channel has been calculated to be less that 500 fs. The board exhibit a dynamical range of ± 800 mV at a sampling speed of 500 MS/s with a noise level measured to be about 2 mV (RMS).




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The time characterization of the board has been achieved by a sequential equivalent time sampling method where one sample per pulse is taken after a very short but well defined delay. An analog pulse shape with a width less than 200 ps, supplied by a signal generator, has been applied at the input of the sampling board with an incoming pulse repetition of 500 MHz. When the pulse occurs, a minimum settable sampling time is added by the delay chip and propagated to the track-and-hold in order to move the sampling time with a minimum time step. This process has been repeated for all possible 32 programmable delay values of the delay chip.

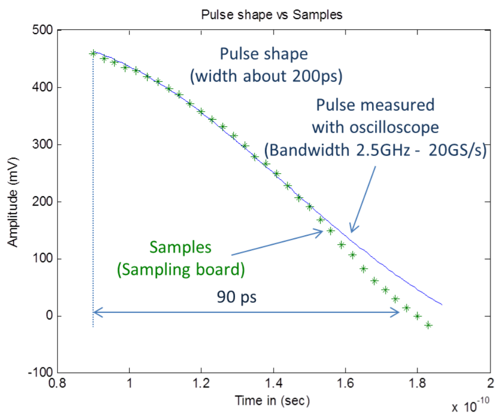


Figure 5. Comparison between the oscilloscope measurement and the 32 samples acquired by the sampling board.

Figure 5 shows the pulse fall time acquired by oscilloscope (input bandwidth of 2.5 GHz) and the sampling point acquired by the board with the method described. The pulse profile was obtained by 32 samples, one for each delay chip step, in 96 ps of sampling time range. The sample points are very close to the pulse measured. The difference seen between the curves is due to the limited input bandwidth of the oscilloscope. This measurement confirms the low DJ noise level present on the board and the good time control accuracy achieved.

## EXPERIMENTAL MEASUREMENTS AT ANKA

Figure 6 shows the peak amplitude of each THz pulse (bunch) sampled and acquired. This shows the typical filling pattern of the ANKA storage ring, consisting of three trains in the orbit positions 0-24, 50-80 and 129-165 separated by a several ns gap. The prototype system is able to resolve single bunch fluctuation in a multi-bunch filling pattern. Multiturn measurements of CSR are an important diagnostic tool for storage rings with short bunch operation [7]. The diagnostics possibility of the ultra-fast DAQ system has really broad range. For example, it will be possible to determine bursting behavior of single bunches in a multi-bunch environment. Moreover, the acquired data will provide a possibility to determine correlation coefficients between buckets in order to study the bunch-bunch-interactions [8].

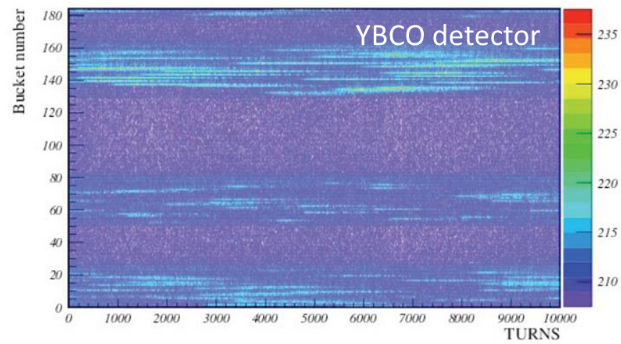


Figure 6. ANKA CSR measured with YBCO detector and DAQ system.

## CONCLUSIONS AND FUTURE WORK

In this paper, we presented a continuous data acquisition system suitable for sampling of CSR pulses with a fast THz detector. An prototype board has been produced and characterized in both analog-to-digital conversion and time accuracy. A dynamical range of ±800 mV was found with a noise about 2 mV (RMS). A time control accuracy less than 3 ps was achieved. The prototype board has been tested at ANKA and was able to sample the peak energy of ultra-short THz pulse with an incoming rate of 500 MHz. The final four sampling channels board is under developing. The voltage and time characterizations and the preliminary test beam results will be presented in further manuscripts.

## ACKNOWLEDGMENT

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