

IMPROVED VECTOR MODULATOR CARD for MTCA-BASED LLRF CONTROL SYSTEM for LINEAR ACCELERATORS

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Abstract

Modern linear accelerators require a high-precision RF field regulation of accelerating cavities. A critical component to achieve high-precision in the feedback loop of a Low Level Radio Frequency (LLRF) controller is the vector modulator driving the high power RF chain. At FLASH, the Free Electron Laser in Hamburg and European XFEL, the LLRF controls are based on MTCA.4 platform. This paper describes the concept, design, and performance of an improved vector modulator module (DRTM-VM02).

It is constructed as a Rear Transition Module (RTM). The module consists of digital, analog, diagnostic, and management subsystems. A FPGA from Xilinx Spartan 6 family receives data from a control module (AMC) using Multi-Gigabit Transceivers (MGTs).

The FPGA controls the analog part, which includes fast, high-precision DACs, I/Q modulator chips, programmable attenuators, power amplifier, and fast RF gates for an external interlock system. Pin assignment on the Zone3 connector is compliant with digital class D1.2 recommendations proposed by DESY. The design has been optimized for mass production and can be easily extended to a wider frequency range. Electronic switches offer software configuration of power and clock sources.

the resonant frequency of the cavities, down to an Intermediate Frequency (IF) using multichannel downconverter modules (DWC). Analog IF signals are digitized by a commercial off-the-shelf AMC module¹. Data is sent to the main LLRF controller module (DAMC-TCK7) using Low-Latency Links (LLL) on the AMC backplane. The controller executes real-time and offline algorithms to compute an required phase and amplitude corrections. The new values are transmitted to the DRTM-VM02 board over the LLL connection. There, an on-board Field Programmable Gate Array (FPGA) deserializes the data and drives fast, high-precision DACs. The current signal from the DACs is conditioned and converted to voltage, before driving a microwave modulator chip.

The previous revision of the board has been described in detail in [2]. The project requirements described there are still valid.

DESIGN DESCRIPTION

This section describes only the main changes introduced in second revision, including:

- modification of Zone3 pin assignment for compliance with Class D1.2
- extension of clock source selection capabilities
- addition of reset circuit for frequency dividers
- optimization of noise and nonlinearity performance
- addition of electronic switch for analog power supply
- improvement of module management subsystem

INTRODUCTION

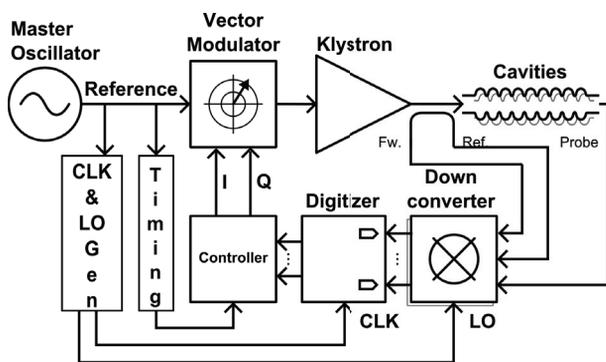


Figure 1: LLRF system architecture

The simplified block diagram of an LLRF system architecture [1] is shown in Fig. 1. The Master Oscillator provides the reference frequency for the system, including the Timing and clock synthesis modules (CLK & LO Gen on the figure). Input and output signals of accelerating cavities are converted from a narrow band around

Digital Subsystem

The MTCA standard defines only the management interface on the Zone 3 connector between AMC and RTM module, providing the designers with the freedom to choose application-specific pin assignment. DESY has proposed a classification recommendation of the pins assignment, to improve the cross-compatibility of the boards, and support the system modularity[3].

The DRTM-VM02 is compatible with the D1.2 class recommendation, offering

- 4 MGT bidirectional lines
- 2 MGT clocks

¹SIS8300 from Struck Innovative Systems GmbH

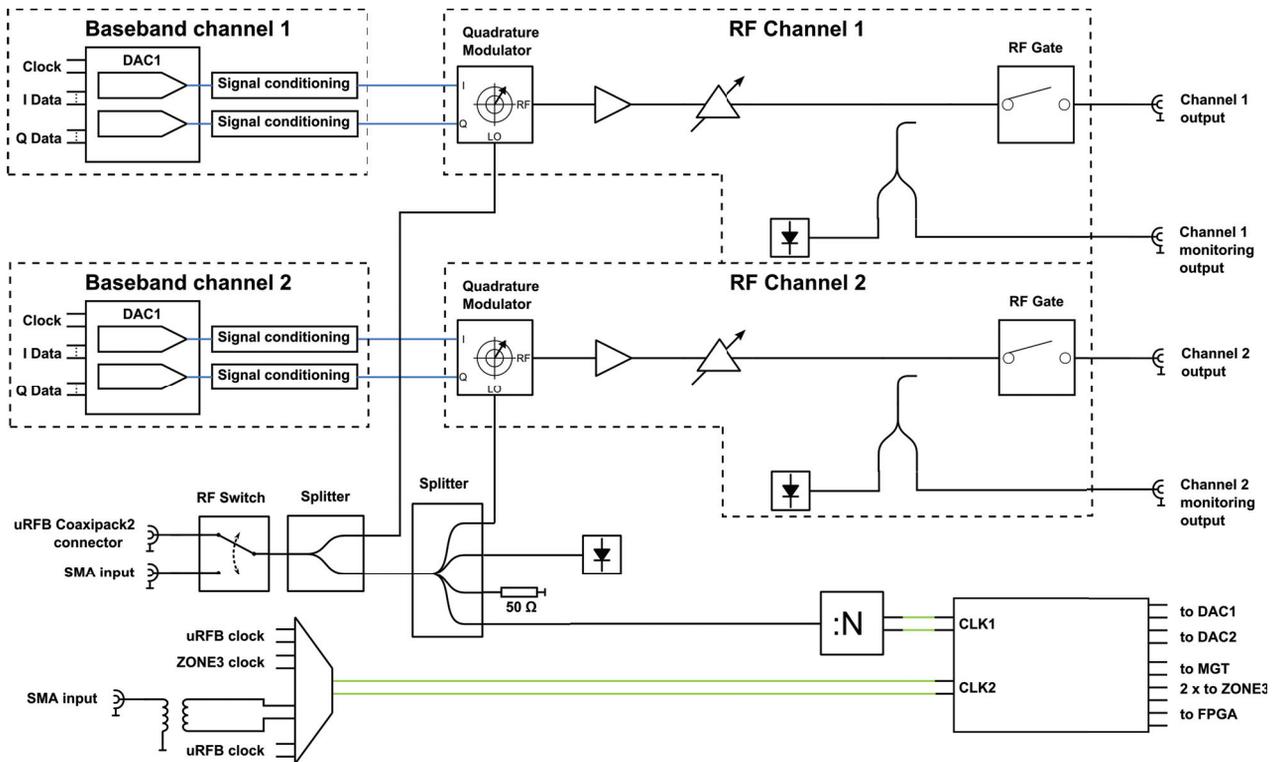


Figure 2: Analog and clocking systems block diagram

- a 38-bit wide parallel differential bus (12 clock capable)
- 3 general purpose clocks

Analog Subsystem

The block diagram of the analog part of the DRTM-VM02 board is shown in Fig. 2.

The first channel is used for driving the high power RF system and the second for calibrating the LLRF system, therefore, the noise level of the first channel is of greater importance. One of the factors influencing the noise level at the output of each channel is the power of the reference signal provided to the channel input. An unequal reference signal power distribution scheme has been chosen to achieve the best noise performance of the first channel, with limited input power.

A low additive phase jitter clock multiplexer has been added, allowing to select one of the following clock sources:

- an SMA connector (on the front panel)
- the Zone3 connector (provided by AMC board)
- one of two RF backplane clocks

The main clock divider and clock distribution IC has a maximum input frequency limit of 2.4 GHz. Board variants operating with a reference frequency higher than this limit are equipped with a prescaler. The prescaler divides the

frequency of the reference input signal (division ratio: 1 – 17) and drives one of the inputs of the main clocking chip. The second input is connected to the aforementioned multiplexer.

Random phase alignment between frequency dividers causes deviation in startup conditions of the LLRF algorithms. In order to eliminate this effect, a synchronous reset signal for the dividers is distributed over the AMC backplane and provided to the RTM modules (including the DRTM-VM02 board).

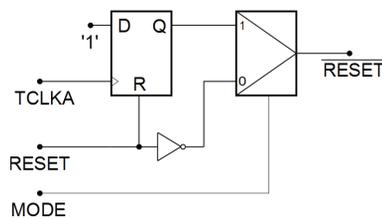


Figure 3: Simplified schematic of reset circuit

Module Management

The DRTM-VM02 board is equipped with advanced management and monitoring hardware designed according to IPMI (Intelligent Platform Management Interface) and MTCA.4 standards, as illustrated in Fig. 4. The management submodule allows for module hot-swapping, monitors all crucial parameters of the RTM board, and realizes E-keying on Zone3 signals.

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The power supply system (DC/DC converters and LDO voltage regulators) is controlled by the RTM Management Controller (RMC). The microcontroller unit (MCU) can selectively enable or disable sections of the power distribution network, eliminating the need for a dedicated power sequencer. The microcontroller monitors 16 of the most important power supply voltages and power good signals of LDOs.

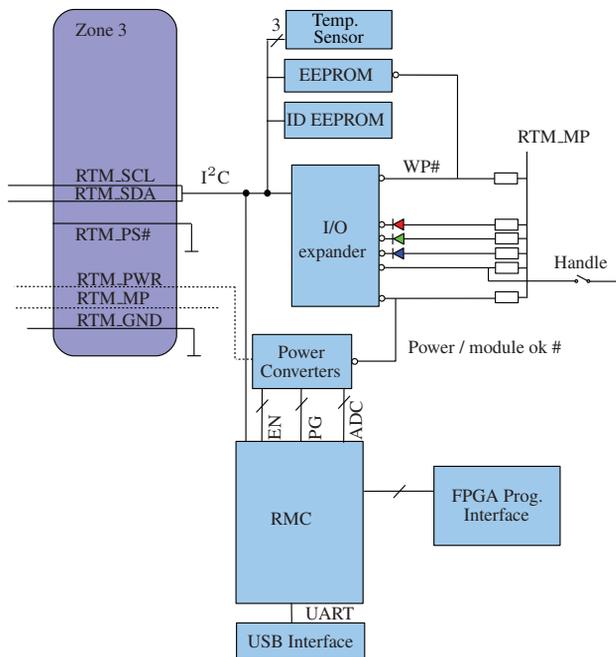


Figure 4: Module management

The presence of the analog backplane is determined using the communication link to a AMC management module. The MCU is also able to monitor the FPGA booting and can force the FPGA reconfiguration, which is crucial for the firmware upgrade functionality. The RMC contains three temperature sensors placed in the most critical parts of the PCB. Every board has a unique 64-bit signature provided by a dedicated circuit.

TESTS

The VM (1.3 GHz variant) has been tested at the laboratory in the debug mode. A very low-noise oscillator has been used as a reference signal source. A comparison of the input and output (for constant I and Q signals) signals' phase noise spectrum is presented in figure 5. The mains 50 Hz signal and its harmonics' distortions are visible in both spectra. The far from carrier (above 1 MHz offset) phase noise level is almost constant (-160 dBc/Hz).

A modulation performance displayed in figure 6 has been achieved after performing a calibration, which involved tuning gains and offsets of DACs. The measured carrier rejection is 72.4 dB and the unwatered sideband suppression is 51.9 dB.

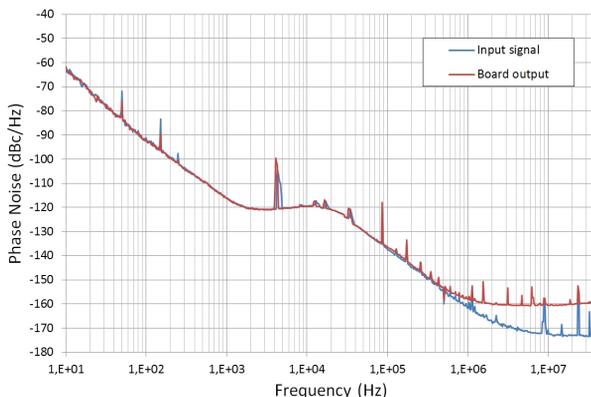


Figure 5: Input and output signals phase noise spectrum

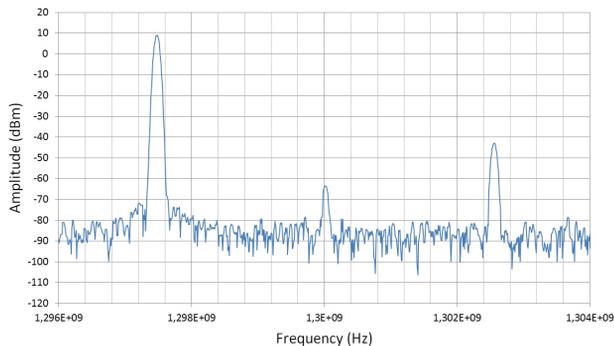


Figure 6: Single sideband modulation spectrum

OUTLOOK

The design meets give electrical and functional requirements.

An automated test stand for mass production of DRMTM-VM02 is currently developed at DESY. It will verify proper operation of all subsystems, greatly reducing the costs of the manual testing.

ACKNOWLEDGMENT

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