

TIME-RESOLVED ELECTRON BEAM POSITION MONITOR MACROPULSE WAVEFORM MEASUREMENTS ON THE LINEAR ACCELERATOR AT THE UNIVERSITY OF HAWAI'I FREE ELECTRON LASER LABORATORY*

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Abstract

Real time macropulse waveform measurements of electron beam will provide valuable data, such as phase, amplitude and energy spread, without disturbing the beam which will allow online bunch diagnostics on electron beam in linear accelerators. Therefore a low cost and space effective prototype system with an oscilloscope on a chip for real time measurement of the macropulse waveform is being developed for the Linear Accelerator at University of Hawai'i. We utilize a custom application specific integrated circuit (ASIC) for the purpose of sampling, storing and digitizing signals. The ASIC is controlled by a field-programmable gate array (FPGA). Initial assembly and testing of the system are complete. Full assembly and installation of the system is in progress. The technology and preliminary results of this project are presented here.

INTRODUCTION

The Free Electron Laser (FEL) Linear Accelerator at the University of Hawai'i FEL laboratory utilizes a thermionic, LaB6 cathode, microwave gun injector and a single section of S-band linac capable of producing a 40 MeV electron beam with average current of 200 mA over the duration of a $4.5 \mu\text{s}$ macropulse consisting of 1-2 ps bunches at 2.856 GHz. The micro bunching produces strong signal at the RF frequencies of the accelerator that is coupled out of the beam-pipe by a family of stripline and wall current beam position monitors (BPM's) which were installed along the MkV accelerator beamline [1]. In order to avoid phase matching problems in comparing two RF voltages and cable loss when comparing BPM signals, each BPM signal is mixed with a local RF reference oscillator in the accelerator vault. The output of the mixer is an intermediate frequency (IF) between 10-20 MHz which is carried to the control room for beam position calculations as well as beam waveform measurements.

Currently stripline BPMs are installed at four locations along the beam line and each BPM has four quadrant pickups which provide us with realtime information about the beam. In 2012, a logarithmic amplifier readout system was added to the BPM system that successfully yields a well-centered beam. However, the output of the mixers, if digitized, can be stored and provide amplitude, phase and en-

ergy spread data from the beam without disturbing it [2]. Therefore, to acquire this data the third generation Ice Radio Sampler chip (IRS3B), which has many desirable characteristics for recording our signals, programmed by a FPGA is used to digitize and record data.

The IRS chip was originally developed for Askaryan Radio Array. IRS3B is the second revision of the third generation IRS chip and it was custom designed at the University of Hawai'i Instrumentation Development Lab (IDLab) to be used in Belle experiment at the High Energy Accelerator Research Organization in Japan known as KEK. Having access to this technology at low cost, compare to commercial ASICs with ten times the cost and half the sampling speed, motivated the real time macropulse waveform measurement project.

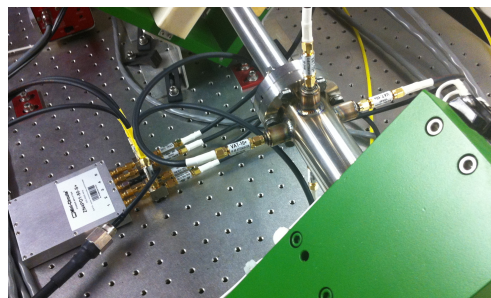


Figure 1: Stripline BPM and four port heterodyne converter installed on the beamline of the accelerator.

BPM WAVEFORM MEASUREMENT SYSTEM DESIGN

Readout Scheme

The raw 2.856 GHz BPM output signals are converted to an intermediate frequency signal by heterodyne mixing. A 2856MHz band pass filter is used to block the higher harmonics and other frequency leakage from entering the double balanced mixer (Mini Circuit ZX05-42MH-S+) and a low pass filter is used to block high frequency leakage from the mixer. A local oscillator (LO) distribution network utilizing four port power splitters is used to drive the mixers at the BPM stations (Figure 1). The 10 MHz output of each mixer is then carried to the control room where it is read out by the IRS3B chip. The specifications of the output

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signals are summarized in Table 1.

Sampling by IRS3B

IRS3B is designed to achieve very high sampling rate (4GSa/s) because it samples through a delay chain instead of a clock, where the delay window is approximately equal the inverse of the sampling rate. For instance if the chip is sampling with a delay of 1 ns then the sampling rate is approximately 1 GHz. It has a very large storage area of more than 32k sample per channel and it's a fast digitizer with conversion time of roughly 16 ns. Also this generation of the IRS chip includes the precision timing logic internally. Therefore it needs very little communication with the FPGA to run. The general specifications and a picture of IRS3B are presented in Table 2 and Figure 2 [3].

Table 1: Signal Specifications

Frequency	10MHz
Dynamic Range	~ 20dB
Pulse Length	4.5 μ s
Repetition Rate	4 Hz

Table 2: IRS3B Specifications

Number of Channels	8
Samples/Channel	32k
Operational Sampling Rate	2.5 GSa/s (currently)
Maximum Sampling Rate	4.0 GSa/s
Samples/ Conversion Window	64
Time of Conversion	~16 ns
Nominal Dynamic Range	9-10 bit

As shown in Table 2, IRS3B has 8 channels and each channel has a large depth. For our purpose, electron beam waveform measurement, this means that it's possible to simultaneously record all four mixer output of two BPM set (two locations on the beamline) provided correct delays are added to the signals. However, since IRS3B is designed to detect photons at Belle, it continuously samples the waveform until triggered, it then continuously fills the memory but skips over the cells with data. This means that the waveform recorded is from before the time of the trigger. On the other hand, in order to minimize number of timing calibration, there are 2 sampling windows (2 groups of 64 samples). One group is sampling while the other group is transferring the data to the storage. Therefore in order to record desired data, correct trigger and delays must be programmed to the chip.

Digitizing by IRS3B

Inside the storage area, a comparator is used to digitalize the data. The IRS3B converts the voltage difference to a time difference, using the comparator. Then the time difference is converted to a digital signal using a counter so

that the number of clock pulses corresponds to the time it took for the sampled voltage to reach the baseline of the comparator. Then the data is transferred to an FPGA and sent to a personal computer for analysis. The block Diagram of the setup is shown in Figure 3.

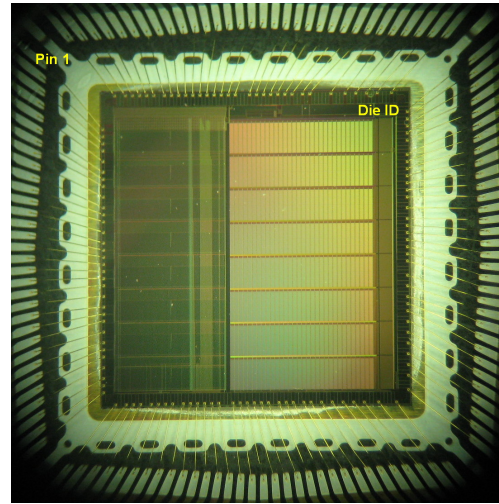


Figure 2: IRS3B: custom ASIC designed at University of Hawai'i IDLab.

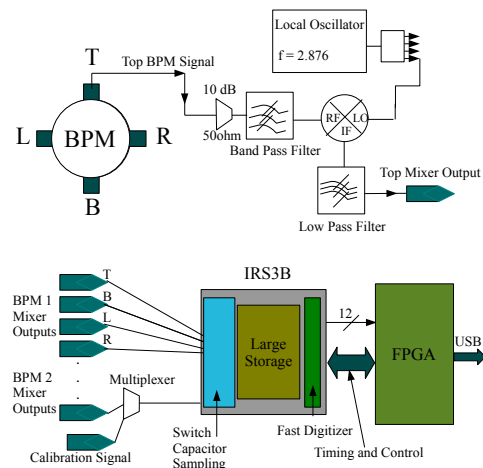


Figure 3: Block diagram of the macropulse waveform measurement setup.

HARDWARE AND SOFTWARE

The model designed and assembled for this project, is a printed circuit board (PCB) daughter card (DC) as a carrier for the IRS3B with 9 RF SMA inputs (8 from the BPM signals and 1 for calibration). The DC is secured on a Universal Evaluation Board (UEB) using parallel board stacking connectors. The Universal Eval Board used is a PCB designed at UH IDLab to allow general testing and evaluation of prototypes. The UEB hosts a Spartan 3 FPGA (Figure 4). Since Spartan 3 is a product of Xilinx, the Xilinx's In-

Integrated software Environment (ISE) and ChipScope Analyzer (an embedded software based logic analyzer from Xilinx) were used for testing and calibration of the board.

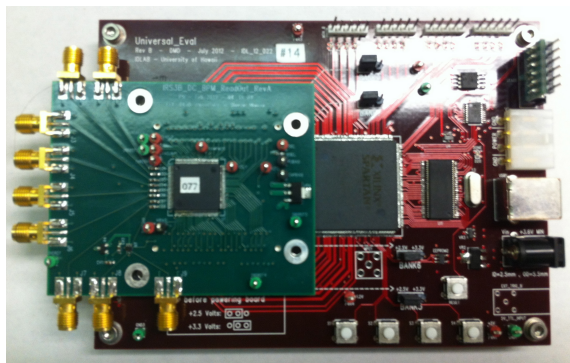


Figure 4: View of the prototype board for macropulse waveform measurement at University of Hawai'i FEL Lab shows the Daughter Card with the IRS3B ASIC mounted on the Universal Eval Board

RESULTS

Basic Calibration

Since the output of the IRS3B is recorded without conversion to voltage, our raw data is recorded in counts. In order to calibrate the system, an RF signal generator was used. The RMS voltage from the RF generator was converted to peak to peak voltage and plotted against the stored data by the system. Then the gain scale was determined by finding a best fit for calibration purposes (Figure 5).

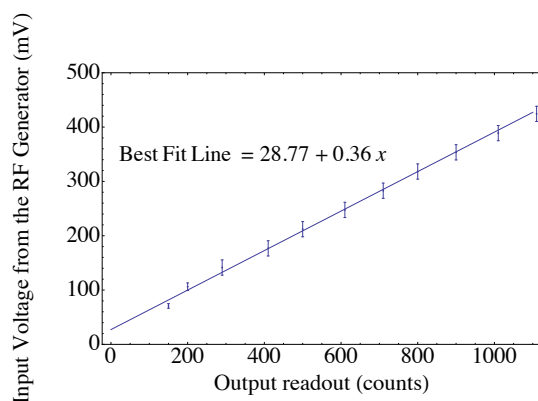


Figure 5: Gain scale plot for RMS voltage to count conversion in IRS3B

Testing the Readout and Storage Process

The advantages that the IRS3B offers in terms of high speed sampling, large storage arrays and fast digitizations are not without restrictions. For the ASIC to work at its

optimum state many bias values have to be adjusted. However once the ASIC is programmed optimally it can perform without any more adjustment. By programming the correct trigger and delay we are able to record data from one channel that is receiving a pulsed 10 MHz signal from a signal generator, an example of data recorded is shown in (Figure 6). Expansion to all 8 channels is in progress.

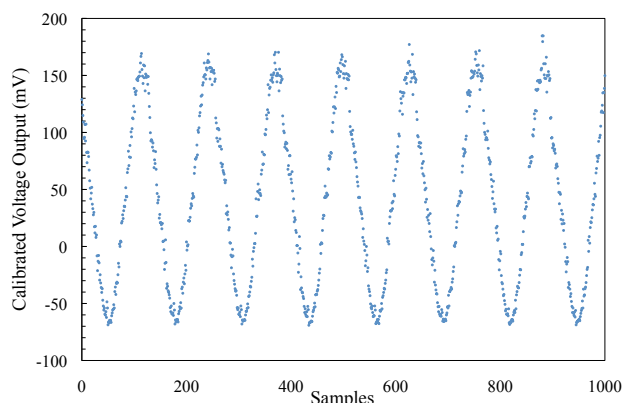


Figure 6: Calibrated data recorded from a single channel readout of the IRS3B, where each period takes 128 samples.

SUMMARY

Good progress was made despite the challenges in design, programing and debugging the system. The prototype design, assembly and initial testing of the system has been successful. Programing the boards to perform at full capacity is in progress. The finalized BPM waveform measurement system is expected to be fully operational in Fall 2013.

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