MODELLING OF PARASITIC INDUCTANCES OF A HIGH PRECISION INDUCTIVE ADDER FOR CLIC

J. Holma, M.J. Barnes, CERN, Geneva, Switzerland
S.J. Ovaska, Aalto University, School of Electrical Engineering, Espoo, Finland

Abstract

The CLIC study is exploring the scheme for an electron-positron collider with high luminosity and a nominal centre-of-mass energy of 3 TeV. The CLIC pre-damping rings and damping rings will produce, through synchrotron radiation, ultra-low emittance beam with high bunch charge. To avoid beam emittance increase, the damping ring kicker systems must provide extremely flat, high-voltage, pulses. The specifications for the extraction kickers of the DRs are particularly demanding: the flat-top of the pulses must be ±12.5 kV with a combined ripple and droop of not more than ±0.02 % (±2.5 V). An inductive adder is a very promising approach to meeting the specifications. However, the output impedance of the inductive adder needs to be well matched to the system impedance. The primary leakage inductance, which cannot be computed accurately analytically, has a significant effect upon the output impedance of the inductive adder. This paper presents predictions, obtained by modelling the 3D geometry of the adder structure and printed circuit boards using the FastHenry code, for primary leakage inductance.

INTRODUCTION

High-energy electron-positron colliders, such as CLIC [1], will be needed to investigate the TeV physics revealed by the LHC. They would provide very clean experimental environments and steady production of all particles within the accessible energy range. To achieve high luminosity at the interaction point, it is essential that the beams have very low transverse emittance: the Pre-Damping Ring (PDR) and Damping Ring (DR) damp the beam emittance to extremely low values in all three planes.

Kickers are required to inject beam into and extract beam from the PDRs and DRs. Jitter in the magnitude of the kick waveform causes beam jitter at the interaction point [2]. In particular, the DR extraction kicker must have a very small magnitude of jitter: the 2 GHz specifications call for a pulse of 160 ns duration flattop, 12.5 kV, 250 A, with a combined ripple and droop of not more than ±0.02 % [1]. In addition, the kicker system must have low longitudinal and transverse beam coupling impedances [3].

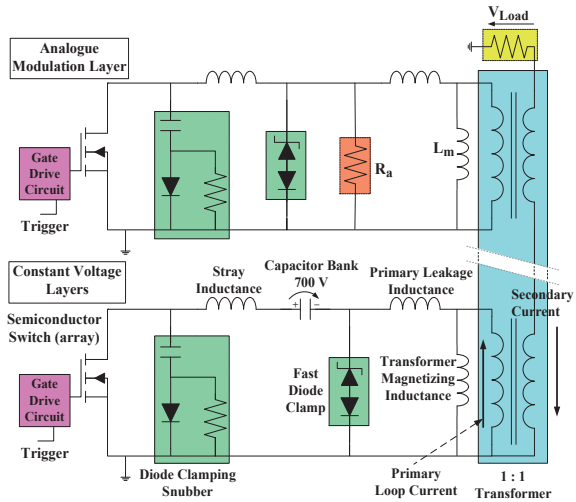

Figure 1: Schematic of an inductive adder with constant voltage layers and an analogue modulation layer.

THE INDUCTIVE ADDER

A review of literature of existing pulse generators has been carried out and an inductive adder (Fig. 1) has been selected as a very promising means of achieving the specifications for the PDR and DR kickers [4]. The inductive adder is a solid-state modulator, which can provide relatively short and precise pulses. With a careful design of the adder, it may be possible to directly meet the ripple and droop requirements of the PDR kicker [5]: studies have shown that analogue modulation may also provide a solution to meet the specifications for the DR kicker [5, 6]. The reasoning for choosing the main components of the inductive adder has been given in [6]. Currently, a 5-layer prototype inductive adder is being tested at CERN. This prototype is being used to verify the predictions for the inductive adder, some of which are presented below.

MODELLING OF PARASITIC INDUCTANCE AND CAPACITANCE

Circuit Model

Figure 2 shows a simplified schematic of a single layer of the inductive adder together with the main parasitic circuit elements. Good impedance matching between the inductive adder and the load is desirable in order to avoid reflections and hence to achieve short rise time for the output pulse.

ISBN 978-3-95450-122-9

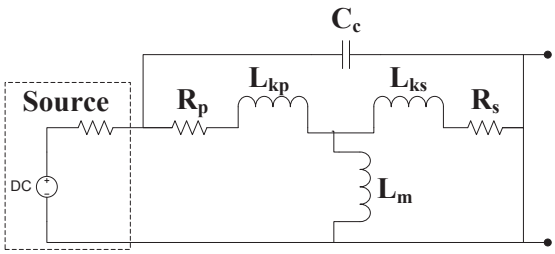

Figure 2: Equivalent circuit of a single layer of an inductive adder. Revised after [7].

In the literature, the following analytical equations are given for coupling capacitance C_c and secondary leakage inductance L_{ks} as functions of physical dimensions of a coaxial (i.e. ideal cylindrical geometry) adder stack [7]:

$$C_c = \frac{2\pi\varepsilon_i l_p}{\ln\frac{D_1}{d}}$$

$$L_{ks} = \frac{\mu_0 l_p}{2\pi}\ln\frac{D_2}{d}$$

Where ε_i is the permittivity of the insulation material between the primary conductor and the secondary stalk, and μ_0 is the permeability of free space. The definitions of the dimensions of a single layer of an inductive adder are shown in Fig. 3: l_p is the length of a single adder layer, l_c is the height of the transformer core, D_1 is the inner diameter of the primary conductor, D_2 is the inner diameter of the transformer core, D_3 is the outer diameter of the transformer core, and d is the outer diameter of the stalk. For the prototype adder, the dimensions are: l_p is 43 mm, l_c is 33 mm, D_3 is 161 mm, D_2 is 94 mm, D_1 is 66 mm and d is 45 mm.

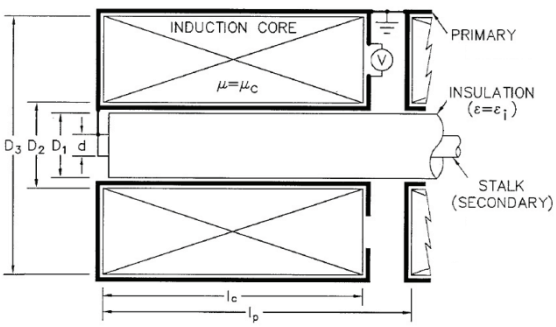

Figure 3: Illustration of an inductive adder cell. Revised after [7].

Primary Leakage Inductance

The primary leakage inductance L_{kp} is the total inductance of the primary circuit of a single layer of the inductive adder. Typically, the primary circuit consists of several parallel current paths each of which has a self (loop) inductance and mutual inductance to the other parallel loops. The mutual inductance depends on the distance between parallel current loops and the area of each loop. The primary leakage inductance has a significant effect on the output impedance [8]; however, it is impractical to accurately compute it analytically.

An approach to match the output impedance of the inductive adder to the load is to [9]:

i. make a conservative (i.e. low) estimate of the primary leakage impedance,
ii. manufacture a stalk which would then achieve the required total inductance (L_{kp}+L_{ks}) per layer,
iii. measure the total impedance of the inductive adder and, if required,
iv. machine the stalk to increase the secondary leakage inductance,
v. re-measure the total impedance of the inductive adder, etc..

This iterative process may require several trials and is quite laborious.

Another approach, which has been used in the study reported here, is to calculate the primary leakage inductance using the 3D code FastHenry [10]. Figure 4 shows the FastHenry model of a single current branch of the primary circuit of a single layer of an inductive adder. One layer consists of eight parallel current paths equally spaced around a circular printed circuit board (PCB). Each current loop includes a simple model of a pulse capacitor, a semiconductor switch, and the tracks and vias of the PCB. The predicted self-inductance of a single loop (L_{kpsl}) is 36.7 nH and the total inductance of the 8 parallel loops is 4.59 nH.

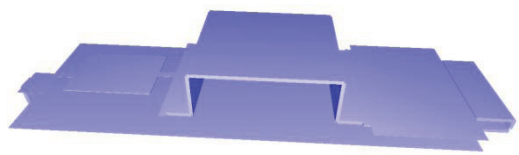

Figure 4: A FastHenry model of a single current branch of a layer of the inductive adder.

The coupling capacitance (Fig. 2) is also an important parameter as it determines the output impedance of the inductive adder. Hence, a similar procedure has been applied for predicting the coupling capacitance, using the code FastCap [10]. The results of this study will be presented in [11].

EXPERIMENTAL RESULTS

Figure 5 shows a photograph of a PCB, which is a half of a single layer of the prototype adder. The semiconductor switches are replaced with copper pieces to permit the measurement of the primary leakage inductance.

One pulse capacitor of the half-layer is initially charged to 10 V, and then discharged by mechanically closing the loop. The pulse capacitor, the primary leakage inductance and resistance of

ISBN 978-3-95450-122-9

Figure 5: A half-layer of the prototype inductive adder.

the discharge loop create a resonant circuit, the voltage of which was measured using a Tektronix DPO5034 oscilloscope. Figure 6 shows a simplified lumped element model of the resonant circuit. The primary leakage inductance of the circuit was computed from the measured waveform using formulae, which have been given in [12]. Table 2 summarizes the results of analytical estimates, computational estimates and measured values of various parasitic elements.

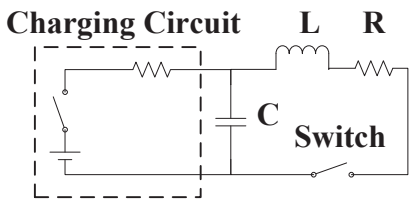

Figure 6: A simplified lumped element model of the resonant circuit, formed by a primary loop.

In addition, the coupling capacitance and secondary leakage inductance have been calculated using the analytical equations, presented above. The coupling capacitance has been measured using a Fluke PM6306 LCR meter. The secondary leakage inductance is derived from impedance measurements carried out using a Rohde & Schwarz vector network analyser ZVB 4. These values are also shown in Table 2 together with the analytical values.

Table 2: Analytical estimates and predicted and measured values for primary leakage inductance (for a single loop), secondary leakage inductance and coupling capacitance.

	L_{kpsl} (nH)	L_{ks} (nH)	C_c (pF)
Analytical	n/a	6.3	6.2
Computational	36.7	n/a	n/a
Measured	43	6.6	7.0

CONCLUSIONS

A method to predict the value of the parasitic inductance of the primary circuit of the inductive adder has been described. The measured value of the primary leakage inductance, of a single loop, is 6.3 nH higher than the prediction, which requires further study. One reason to the difference could be that in the primary loop measurements the effective current path is partly narrower than that represented in the simulations. The measured values of the coupling capacitance and the secondary leakage inductance are close to the analytical values. The presented method, once fully verified, will be used to predict the parasitic inductance for the next version of a PCB for the CLIC DR inductive adder: this will permit high precision matching of the output impedance of the inductive adder and the impedance of the load.

ACKNOWLEDGEMENT

The authors thank doctoral student Michael Betz for helping with the impedance measurements.

REFERENCES

[1] M. Aicheler (ed.) et al., "A Multi-TeV Linear Collider Based on CLIC Technology: CLIC Conceptual Design Report", CERN-2012-007.
[2] Y. Papaphilippou et al., "Conceptual Design of the CLIC Damping Rings", Proc. IPAC'12, New Orleans, USA, May 2012, TUPPC086; http://www.JACoW.org
[3] Y. Papaphilippou, "Parameter Specification, EDMS #989080, Kickers for the CLIC Damping and Predamping Rings", PBS reference: 1.2._.10.
[4] J. Holma et al., "Preliminary Design of the Pulse Generator for the CLIC DR Extraction System", Proc. PPC'11, Chicago, USA, June 19-23, 2011.
[5] J. Holma and M.J. Barnes, "Pulse Power Modulator Development for the CLIC Damping Ring Kickers", CLIC-Note-938, CERN, Geneva, Switzerland, April 27, 2012.
[6] J. Holma and M.J. Barnes, "Preliminary Design of an Inductive Adder for CLIC Damping Rings", Proc. IPAC'11, Spain, Sept. 2011, THPO032; http://www.JACoW.org
[7] C. Burkhart et al., "MIA Modulator for the LLNL "small recirculator" experiment", Elsevier Science, 2001.
[8] W. Zhang et al., "A Simplified Model for Parameter Estimation and Circuit Analysis of Inductive-Adder Modulator", IEEE Transactions on Dielectrics and Electrical Insulation, Vol. 14, No. 4, pp. 913-920, Aug. 2007.
[9] E.G. Cook, priv. comm., May 29, 2012.
[10] www.fastfieldsolvers.com
[11] J. Holma and M.J. Barnes, "Initial Measurements on a Prototype Inductive Adder with Ultra-Flat Output Pulse for the CLIC Kicker Systems", to be published.
[12] J. Holma and M.J. Barnes, "Evaluation of Components for the High Precision Inductive Adder for the CLIC Damping Rings", Proc. IPAC'12, New Orleans, USA, May 2012, THPPD076; http://www.JACoW.org