RESEARCH AND DESIGN OF DIGITAL POWER SUPPLY FOR HIRFL-RIBLL CORRECTOR MAGNET*

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Abstract

One digital power supply was designed for RIBLL (Radioactive Ion Beam Line in Lanzhou) corrector magnet at HIRFL (Heavy Ion Research Facility in Lanzhou). Adopting two parallel connected IGBT full-bridges as the power circuit topology, the power supply can generate bipolar DC current when it runs in the fourquadrant working states, which well meets the requirements of corrector magnet. SOPC platform of Altera based on Nios II is chosen to design the digital power supply regulator. Employing FPGA as the control core and utilizing SOPC principles, the digital regulator is designed against special requirements of accelerator power supply. The test results indicate that performance of the power supply can meet the design requirements.

INTRODUCTION

RIBLL is the Projectile Fragmentation secondary beam line constructed at HIRFL and in operation since January 1998, which has undertaken a lot of experimental tasks. To improve the quality of secondary beam and efficiency of beam commissioning, a corrector magnet is required to be located before the entrance of RIBLL. But it's not convenient to correct the main beam's position and direction due to the unipolar current generated by the original corrector power supply, therefore the scheme of converting the power supply to bipolar output is proposed. Main characteristics and requirements of the new power supply are described as follows: be run in DC mode, the rated power is ±750A/±35V, and the current stability is 200 ppm (parts per million) over 8 hours.

Owing to programmability, high reliability and integration, etc., digital control has become the development trend of accelerator power supply nowadays, for this reason, the new power supply which will replace the old analogue one will be a digital one based on FPGA. The scheme of the digital power supply is introduced in the paper.

TOPOLOGY

The digital power supply adopts two H-Bridge converters in parallel as the circuit topology (as shown in Figure 1). The control signal of 90 degree phase-shift is utilized to drive the tubes of the two converters in order to achieve the effect of frequency multiplication. This H-bridge converter structure can run in four-quadrant working states and provide any-polarity voltage and current.

To realize the dual polarity current output, four PWM (Pulse Width Modulation) signals are required to be generated to drive four IGBTs (Insulated Gate Bipolar Translator) for each H-Bridge. As we all know, it will lead to short-circuit if two IGBTs in the same bridge arm work in breakover mode at the same time, hence dead-time control should be applied to PWM generation module in order to avoid the short-circuit. Figure 2 shows the four PWM waveforms, in which PWM11, PWM12, PWM13 and PWM14 are the driving signals of S1, S2, S3 and S4 shown in Figure 1. Using triangle wave as carrier, PWM11 and PWM12 are generated by comparing one triangle wave with two values (u1 and u2), where u1 is the output of the regulator loop, u2 is the sum of u1 and DT (dead time). PWM13 and PWM14 are generated in the same principle by 180 degree phase shift of the triangle wave.

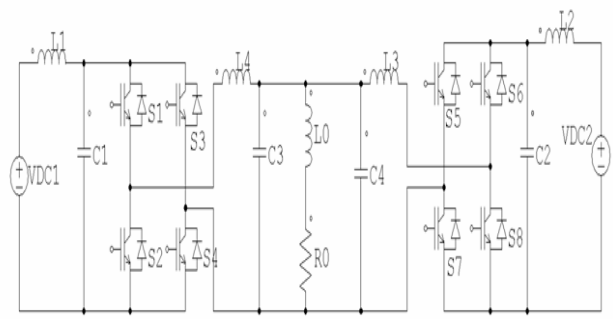

Figure 1: Topology of power supply.

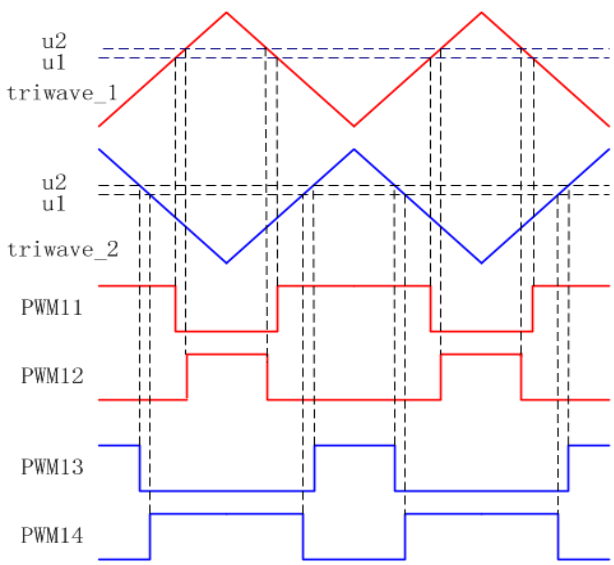

Figure 2: H-Bridge PWM waveforms.

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CONTROL STRATEGY

It has two purposes of the digital control, one is to make the power supply satisfy the stability specification and the other to make the two converters work in the same way by drawing the same amount of current from both of them.

The digital regulator makes use of the structure shown in Fig.3, it consists of current loop, voltage loop, and current-sharing loop, and each loop employs PI algorithm. Using the output of outer loop as reference inputs of current-sharing, it ensures that the two H-bridge generate the same current. I_ref indicates current reference in Figure 3, I_fd denotes load current feedback, V_fd means load voltage feedback, Avg1_fd current feedback of one H-Bridge, and Avg2_fd current feedback of another H-Bridge.

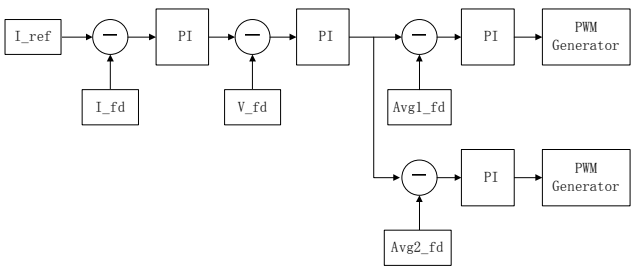

Figure 3: Structure of digital regulator.

HARDWARE DESIGN

To meet the requirements of operation and on-site commission of the power supply, Altera EP2C70 FPGA is chosen as the controller core of the digital controller and some peripherals are extended, including memory (Flash, SDRAM, SSRAM), two kinds of communication interfaces (one Ethernet and two UARTs), digital-analogue and analogue-digital conversion module (ADC and DAC), fiber optic receiver, EPCS controller, PWM output channels and fault signal input channels. The functions of these peripherals are described in the following text.

ADC module is used to high-speed sample the output current or voltage, and DAC module is used to convert digital signals to analogue signals, which is convenient to observe digital signals by oscilloscope.

The power supply is controlled through Ethernet by control interface in remote computer. Many operations on the power supply can be done through the Ethernet, such as power on, power off, power reset, updating current reference, sending waveforms, and configuring parameters of digital regulator. Meanwhile, real-time running status information of the power supply will be back-fed to the remote computer, such as current, voltage, fault type, and register's calculation result of digital controller.

The power supply can also be controlled by local control panel through one of the two UART interfaces, which has the same function as Ethernet. The other UART is used as communicate port between State Monitor and Operation Unit and digital controller. The function of the unit consists of collecting internal nodes state of the power supply, making a response to fault and interlock signals according to the nodes state, and performing necessary protection through controlling relay.

SOFTWARE DESIGN

The function module of digital controller comprises control strategy, ADC and DAC control, low-pass filter module, PWM generator, over-current and over-voltage protection modules, all of which are realized in FPGA with Verilog hardware description language. Register file and Avalon interface file are also designed. The function module and the files are encapsulated into the digital regulator component by Component Editor in SOPC (system on a programmable chip) Builder.

As shown in Figure 4, two embedded soft-core processors, memory, some interfaces, synchronous optical fiber component and digital regulator component are working together to construct the Nios II system. All of the peripherals are connected to the corresponding Nios II CPU by Avalon Bus. Two Nios II processors are programmed by Nios II Software Build Tools, and μC/OS II operating system is transplanted in CPU1, which is in charge of data communications with external interfaces, containing configuring parameters, doing waveform interpolation, and saving running state information of power supply. CPU2 is responsible for updating the reference of current or voltage.

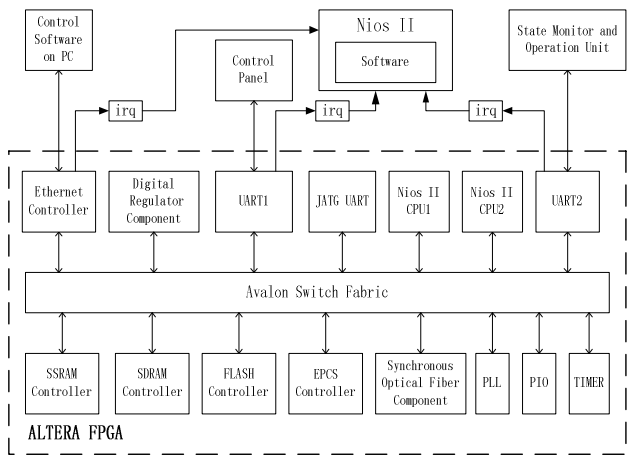

Figure 4: Nios II Processor System.

EXPERIMENTAL RESULTS

The corrector power supply has been designed and tested up to last month, and a set of experimental results is presented below.

Figure 5 shows the H-Bridge PWM signals for positive output, and Figure 6 shows signals for negative output. Channel 1 to 4 is PWM signal of the IGBT S1 to S4 respectively, and there is 5 us dead-time between two IGBTS in the same bridge arm.

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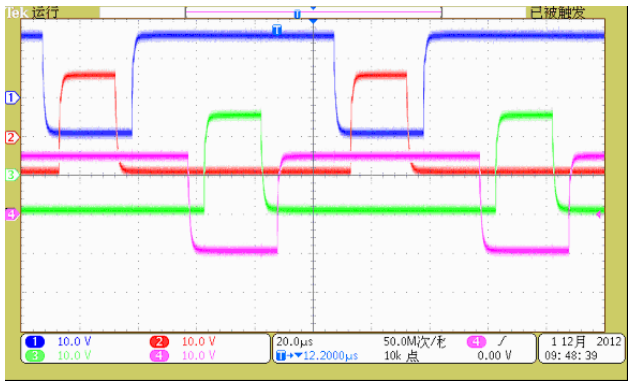

Figure 5: PWM signals for positive output.

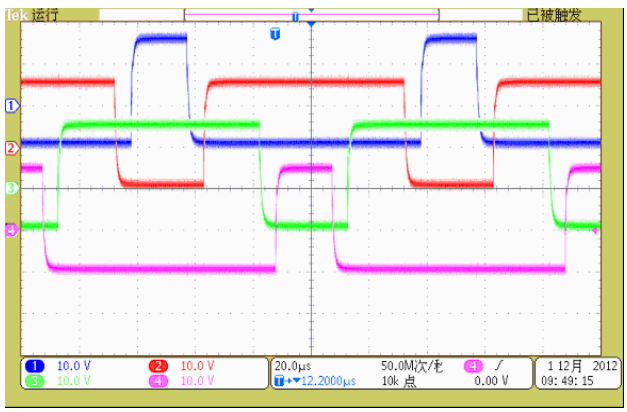

Figure 6: PWM signals for negative output.

Figure 7 demonstrates stability test result of 8 hours when the output current is 750A, and Figure 8 displays each H-Bridge's output current during 72 hours.

Formula 1 shows the way of stability calculation,

$$\gamma = \frac{I_{max} - I_{min}}{I_{average}} \quad (1)$$

Where, I_{max} indicates the maximum current in the measurement, I_{min} means the minimum current, and $I_{average}$ denotes the average current. The stability is 41.6 ppm according to the formula, which result satisfies the design specification.

As shown in Fig. 8, two H-Bridge almost output the same amount of current in the test over 72 hours, obtaining the satisfactory current-sharing results.

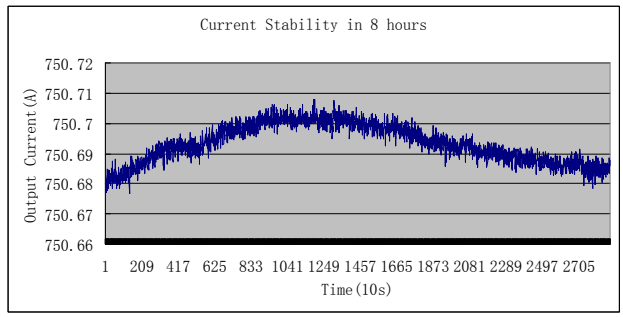

Figure 7: Current stability of 750A.

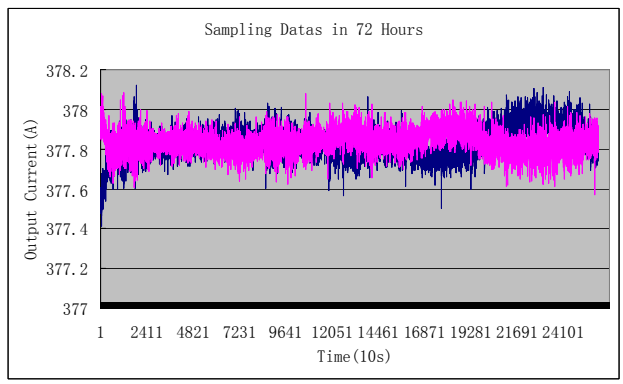

Figure 8: Output current of two converters.

CONCLUSION

According to the test results, the performance of the corrector power supply meets the design requirement. The power supply is waiting for the on-line operation in next experiment at RIBLL. Two H-Bridge converters by parallel connection can provide a good choice for power with a wide range of output, and the current-sharing strategy provides a good practice to control multi-level parallel converter.

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