DIGITAL PULSE PROCESSOR FOR HIGH DEMANDING SYNCHROTRON SPECTROSCOPY

S. Bucik, A. Bardorfer, B. Baricevic, R. Hrovatin, E. Janezic, B. Repic, D. Skvarc, Instrumentation Technologies d.d., Solkan, Slovenia
M. Vencelj, Jozef Stefan Institute, Ljubljana, Slovenia

Abstract

The availability of brighter synchrotorn X-ray sources enable more complex experiments, such as 2D or 3D X-mapping. All the electrical signals generated in semiconductive detectors are then processed and analysed by fast digital pulse processors (DPP).

The poster presents the state of the art DPP currently in development by Instrumentation Technologies (see Fig. 1). We will discuss the signal transformation and processing from the detector preamplifier output to the final result: energy histogram and time stamped list mode.

The signal processing chain starts with signal conditioning of the analog input signal. After the ADCs transformation, all the signal processing in the digital domain is done in FPGA. To each measured pulse a time-stamp is applied. Libera BASE FDK enables customer specific algorithms to be included in the FPGA.

THE ANALOGUE PART

The preamplifier of the silicon detector is directly connected to the analogue input of the digital pulse processor. The termination is selectable between 50 Ohm and 500 Ohm to suit different termination adjustments. The voltage signal (max +-10V) is properly amplified/attenuated and transformed for further processing (optimal matching to detector preamplifier: pulse reset/continuous discharge, polarity). The PGA (programmable gain amplifier) chip amplifies the signal to the optimal resolution/energy range, moves the signal into the right operating point and makes it accessible to the 16 bit ADC (analogue digital converter). The sampled signal (150Mhz) is now accessible in the digital domain.

FPGA DATA PROCESSING

In the digital domain the digitized signal is processed in two steps (see Fig. 2). All the demanding tasks and those that need fast execution are processed on the FPGA (Xilinx Virtex 6). The signal data that exceeds the user selected energy threshold is analyses with the Moving Window Deconvolution (MWD) algorithm for pulse height determination [2]. Each pulse is transformed to a flat-top trapezoidal shape. Each trapezoidal pulse is marked as accepted or rejected. Pulses are marked as rejected, if two or more pulses come to quickly one after another. The system can detect them, but can not properly calculate their amplitude, that's why they are rejected (Pile up rejection).

To each accepted pulse a time-stamp is added [1]. The time-stamp is calculated as the time difference between the last synchronization and the “pulse start” time. The synchronization occurs on system start-up, changing instrument operation modes or triggered manually.

The combined data: amplitude (16 bits) and time-stamp (64 bits) is sent as a list mode data-flow to the AMC CPU (Advanced Mezzanine Card, Central Processing Unit). Additional 48 bits are used for other data.

The FPGA also calculates statistical data as: sum of input events, sum of accepted output events, real time, live time, paralyzable and non- paralyzable dead times, , ICR, OCR ....

The Libera BASE FDK enables customer specific algorithms to be included in the FPGA.

Figure 1: A 4 channel digital pulse processor.

AMC CPU DATA PROCESSING

he main function of the AMC CPU (Intel i7, 2.53GHz, 4GB RAM) is to further process the data from the FPGA and to enable the clients to access the system. The software on AMC CPU is based on the Libera BASE framework. Therefore most of the software libraries and communication interfaces to the FPGA and clients are standardized, so they are the same as in all new Libera family products.

All the data processed and calculated in the FPGA is available to the client trough the AMC CPU. The data throughput limit of the system is determined by 4 main factors: FPGA to CPU transfer, CPU load, local area network throughput and data write speed (usually hard disk) on the client side.

ISBN 978-3-95450-115-1

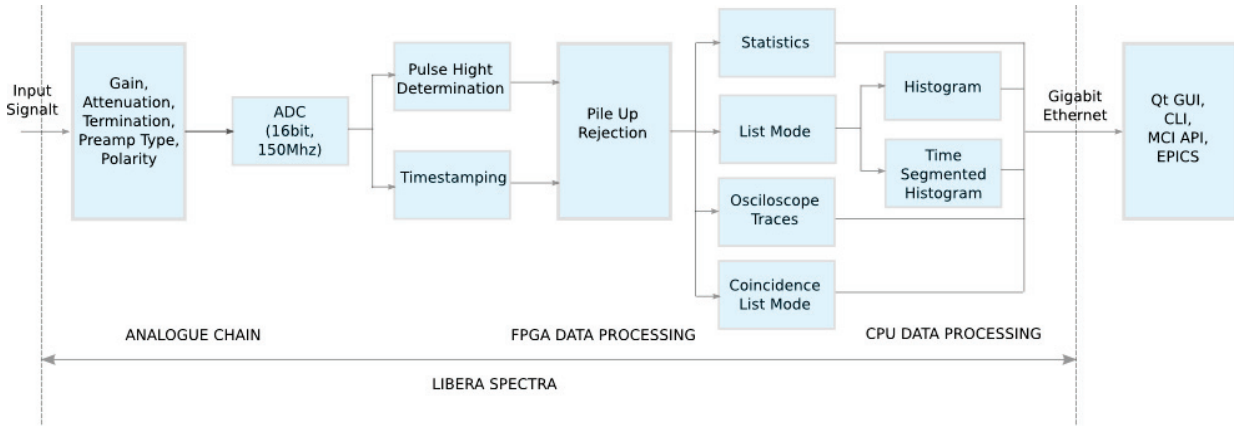

Figure 2: Data flow within channel of a digital pulse processor.

CLIENT ACCESS

Clients interactive accesses the system through Libera BASE defined interfaces. A Qt based GUI client software is available (see Fig. 3). It enables the user to:

- Control the system: the connection, reset, board management, health diagnostics …
- Set, copy, save and load parameter settings.
- View oscilloscope traces (time domain digital signals, that help the user to set appropriate settings)
- View and save histograms
- View and save statistics
- Save list mode data

Command Line interface (CLI) provides batch mode interface. A EPICS server implementation enables easy integration of the instrument into the control system

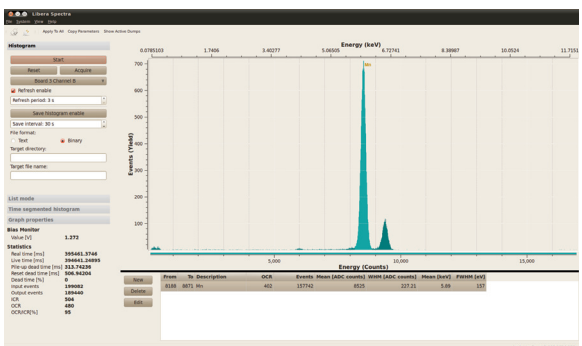

Figure 3: The Qt GUI: Basic histogram and statistics.

MTCA.4 ARCHITECTURE

The MTCA.4 architecture known as MicroTCA for physics enables high data transfer capabilities, modularity, synchronization options, extensive management of the boards. The main components of a instrument are (see Fig. 4):

- Crate with power supply.
- MCH (MicroTCA Carrier Hub) module – power management, health diagnostics, switching fabrics
- Powerful CPU.
- Up to 10 Libera Spectra modules.

Figure 4: The MTCA.4. Crate. From left: Power supply, MCH, CPU, 2 x Libera Spectra module, space other 8 modules and/or another power supply.

CONCLUSION

The selected platform enables the instrument to work autonomous. The client is only needed to set the configuration settings, for data visualization and data saving. In case of basic histogram calculation there is no need for a permanent network connection. The Libera BASE framework enables an uniform interface to different clients (CLI, EPICS, Qt GUI...)

REFERENCES

[1] J. Kolar, “Multichannel Digital Acquisition FPGA-based System for Photon Detectors Equipped with Resistive and Reset Preamplifiers,” SRI’09, Melbourne, Australia, September 2009

[2] J. Stein, f. Scheuer, W. Gast and A. Georgiev. “X-ray detectors with digitized preamplifiers”, Nucl. Instr. And Meth. in Phys. Res. B, 113, pp. 141-145, 1996