THE PRELIMINARY TEST OF A DIGITAL CONTROL SYSTEM BASED ON THE FPGA FOR A PEFP 120-KEV RF CAVITY*

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Abstract

PEFP developed a 120-keV RF cavity for their ion implantation applications. Due to ambient disturbances, the cavity's resonance frequency may vary in long-term test. We designed a digital control system to change the frequency of the RF sources for tracking the cavity's frequency variations. The digital control system has functions such as, phase shift, phase comparison, proportional-integral compensation, waveform generation and frequency/pulse modulation, and driving signal generator. Most of them are implemented digitally in a Virtex II 4000 Field Programmable Gate Array (FPGA). In this research we show the design and the preliminary test results of the digital control system.

CONTROL SYSTEM OVERVIEW

Proton Engineering Frontier Project (PEFP) has developed a 120-keV RF implanter which for utilized as heavy ion implantation for semiconductor manufacture, and so on. In case of its working environment, there are some unexpected disturbances. So the cavity's accelerating gradient cannot always work at the peak point. In order to maximize the RF field accelerating gradient $\boldsymbol{E_0T}$ for the cavity, we designed a digital control system for this RF implanter.

This algorithm's goal is to change the RF source driving frequency by using the relation of phase and frequency. If the frequency delta (cavity frequency v.s. driving source) has a phase difference located within its bandwidth. By measuring the phase difference, we can evaluate the frequency delta according to it. We then adjust RF source's frequency to generate this signal for the amplifier. The control system is a Field Programmable Gate Array (FPGA) based feedback loop which can keep the resonance of the cavity.

The control logic consists of a phase comparator, phase shifter, Proportional Integral (PI) compensator, and a waveform generator. There is a VME PowerPC (Single Board Computer) SBC which is used as the carrier board to hold the FPGA processor card. The real physical system consists of the PEFP cavity and amplifier. In this work, we mainly talked about the system architecture design, FPGA control logic design and preliminary waveform generation test in low power. [1-4]

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MOTIVATION AND CONCEPTS

Motivations and Resolved Schemes

PEFP RF Implanter was placed at a normal-temperature environment. The ambient disturbances were not controlled. Such as the (1) vacuum pump vibrations, (2) and ambient temperature drift. These unavoidable disturbances are rapidly and seriously changing cavity resonance frequency. Thus it can affect or decrease the accelerating gradient of RF implanter's cavity in long-term test. We designed a variable RF source is tracking the resonance of the cavity. Fig. 1 shows the signal flows of designs for the control system. The cavity's frequency change rate is far lower than the response rate of digital control loop. So we don't need to build a broad range (out-of-bandwidth hopping) intelligent search algorithm. We just care fast tracking algorithm within the cavity's bandwidth.

In this scheme, we choose the variable RF source and a FPGA based digital system, and a SRS DG535 pulse generator triggers FPGA data acquisition. Our goal is to keep cavity working at resonance by adjusting the source (reference frequency) dynamically.

The Function of Digital Control System

The FPGA card receives two signals come from cavity and RF source (FPGA card itself). The control logic calculates the change quantities of phase before and after the cavity, so as to the measure the required frequency deviations. And we use a PI compensator to compensate the loop, just reducing the fluctuations of the loop error signals. That means the reference signal, i.e. the RF source's frequency was controlled by FPGA logic. We made the FPGA logic to generate a 12.8 MHz drive RF signal for the amplifier.

THE ALGORITHM OF DIGITAL CONTROL SYSTEM

The cavity originally designed driving frequency is around 13-MHz. The sampling clock is 51.2-MHz. The card output centre frequency is 12.8-MHz. The reason for us to choose 12.8 MHz sinusoid signal, the first reason is that because we have to cover the cavities resonance frequency fluctuates around 13-MHz designed working frequency.

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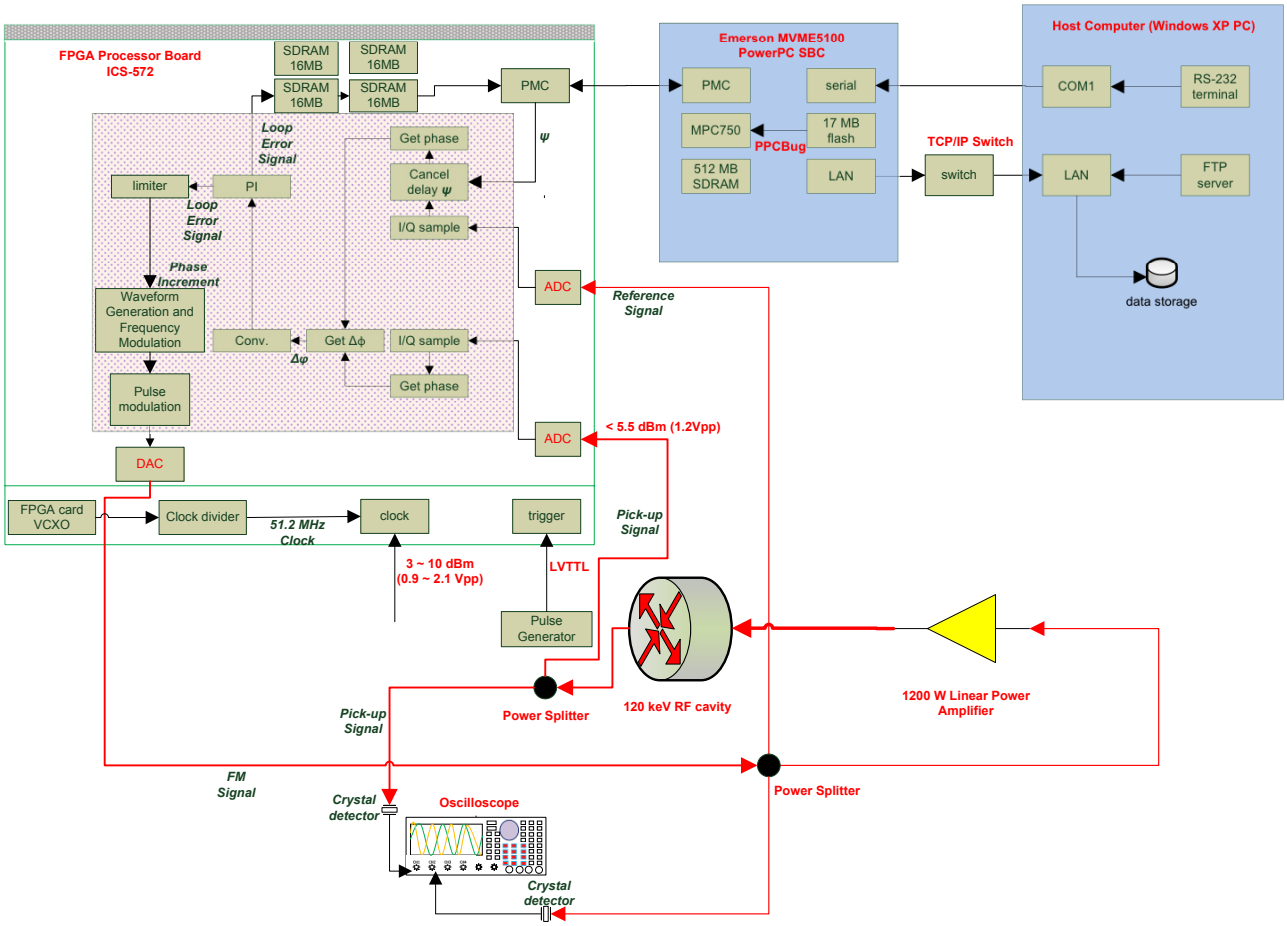

Figure 1: Block diagram of the digital control system's RF signals and logic signals.

The second reason is that we use the card internal clock. The clock divider CDC7005 can just exactly produce this frequency.

We use the phase difference method to determine the how much frequency increment we should change for the internal RF source. For a RF cavity working in normal temperature, we need to cover around -45 degree to 45 degree phase variation range (just cavity's 3dB bandwidth, usually called half-power point) in FPGA algorithm.

FPGA Control Logic

The key part of the control algorithm resided in the FPGA, the logic is shown in Fig. 3. The FPGA processor XC2V4000 contains the custom signal processing logic made by us. From the incident reference and cavity signals, FPGA logic directly sampled both RF signals in a constant time interval pattern-style with 51.2-MHz timing clock. So we can obtain the Q, I –Q, -I… sequence from two signals, respectively.

We need to obtain two I samples and two Q samples during one RF cycle, this is a reason why we choose 51.2 MHz sampling clock v.s. 12.8 MHz IF. And then we use a rotation matrix to cancel the natural phase difference ψ induced due to time delay of mismatched lengths of cables. Next we use a CORDIC algorithm to obtain their phases, and compared both of them to obtain the difference. And we convey the phase difference into next stage as loop error signal. The PI compensator will control the error signal. Finally we output compensated loop error signal to VME computer. Meanwhile we generate a 12.8 MHz sinusoid waveform in FPGA, and then we use the loop error signal to modulate this carrier. Next the modulated signal will be filtered by a pulse clock. The final signal will output through (Digital-Analogue Converter) DAC.

LOW-POWER RF TEST

See Fig. 2. This is the RF experimental set-up. Fig. 4 is diagram of experimental configurations for our control system. We use a pulse generator triggers both ADC and DAC operations.

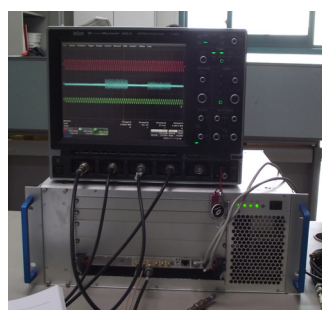

Figure 2: The system under low power test.

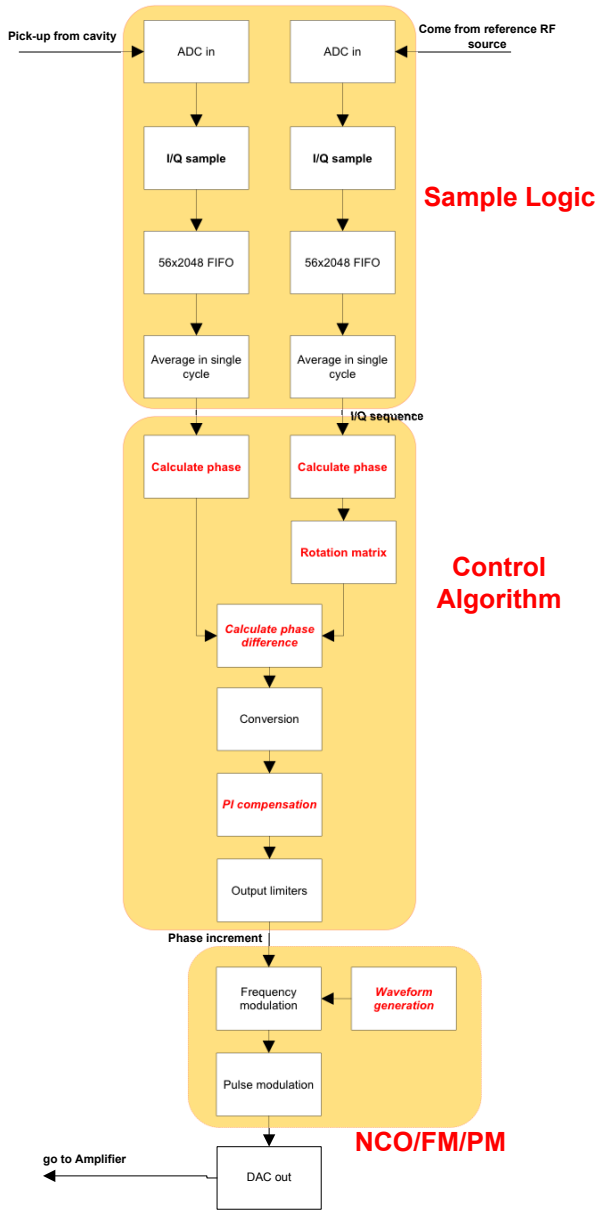

Figure 3: The flow graph of the FPGA algorithm.

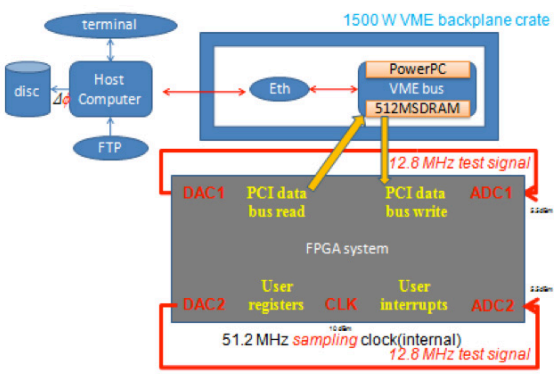

Figure 4: The test configuration of 12.8 MHz RF signal generation.

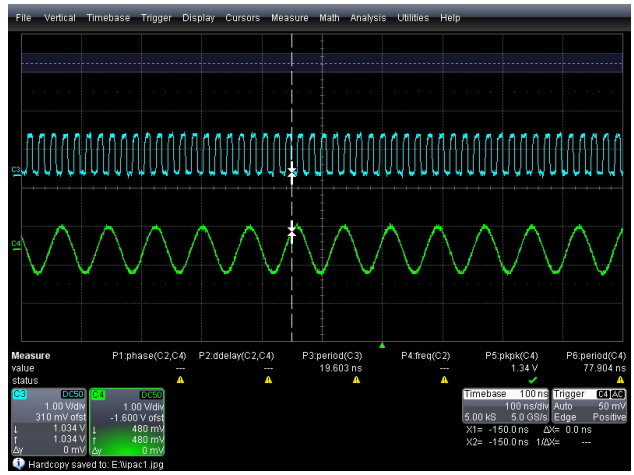

Figure 5: FPGA generated 12.8-MHz drive RF signal and 51.2-MHz sampling clock.

In the Fig. 5, the blue trace is the internal 51.2 MHz sampling clock coming from card's VCXO. The green trace is the generated 12.8 MHz driving signal coming from DAC.

CONCLUSION

In the presence of the environmental disturbances, such as, fast pump vibrations and slow temperature drift, the resonance frequency of cavity varies frequently in long-term test. We designed a control system which manipulates an internal RF source producing a single-tone signal to drive the amplifier. The algorithm in FPGA calculates and determines the frequency of driving signal. So the system can quickly reduce the frequency deviations between internal RF source and the cavity, i.e. the reference signal is always tracking the change trend of cavity resonance frequency. Thus the RF implanter's accelerating gradient can be maximized in given forwarded power and coupling coefficient. The design was finished. Through the preliminary test, we can produce the single-tone 12.8 MHz driving signal by using the FPGA card.

ACKNOWLEDGMENT

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