DROOP COMPENSATION FOR THE HIGH VOLTAGE CONVERTER MODULATORS AT THE SPALLATION NEUTRON SOURCE*

G. P. Patel, D. E. Anderson, D. J. Solley, M. W. Wezensky, Oak Ridge National Laboratory (ORNL), Oak Ridge, TN 37831, USA

Abstract

The Spallation Neutron Source (SNS) has been in operation since 2006 and routinely operates at 1 MW of beam power. At 1 MW, the High Voltage Converter Modulators (HVCMs) are delivering 8-11 MW pulsed power to the Klystrons for up to 1185 us at 60 Hz. The pulsed output of the modulator has a substantial voltage droop operating in open-loop mode. Achieving 1.4 MW operations require an increase in the output pulse width of the HVCM, resulting in loss of LLRF control margin due to modulator voltage reduction at the end of the pulse. Initially, the HVCM was designed with a pulse width modulation scheme for droop compensation but early operations at full duty revealed this technique unreliable. Increasing the output voltage of the modulator would likely compromise system reliability. This paper proposes the use of alternate modulation schemes to address the voltage droop. The effect of frequency modulation and phase modulation on voltage droop is studied. Experimental results will also be presented.

INTRODUCTION

SNS is a proton Linear Accelerator (Linac) used for Neutron Production [1]. There are 15 HVCMs in the Linac producing high voltage pulses up to 135 kV for 1185 us at 60 Hz. Several upgrades have been made to improve overall HVCM reliability [2]. A future operational goal for SNS involves delivering 1.4 MW of beam power on target. This requires increasing the output pulse length of the HVCM by about 15 %. This paper discusses the present HVCM voltage droop and its limitation for the future operational goal. It proposes pulse width modulation techniques like frequency shift and phase shift modulation techniques to address the voltage droop. Experimental results are from 60 Hz operation.

The system block diagram of the HVCM at SNS is shown in Fig. 1. A 3-phase 13.8 kV: 2.1 kV transformer feeds power to a 6 pulse SCR rectifier. The rectifier charges two 112 mF storage capacitor banks up to +/- 1150 V. Three full bridge IGBTs switching at 20 kHz feed energy from the capacitor banks to step up transformers in the HVCM oil tank. The transformer leakage inductance and the high voltage capacitor connected across the secondary of the transformer form a resonant circuit. This resonant convertor helps reduce switching loss and enable high frequency switching of the IGBTs. The secondary is connected to a voltage doubler rectifier circuit. The pulsed DC output is filtered through a pi filter and fed to the klystron's cathode. Due to the high switching frequency, the entire system is very compact compared with other MW-class modulators.

HVCM SYSTEM

The typical output pulse from the test HVCM is shown in Fig. 2. The measured output voltage droops by approximately 3 % which can be attributed to the storage capacitor discharging. With increased voltage droop, the phase margin of the low level RF (LLRF) system decreases and the LLRF system can no longer maintain control of the phase and amplitude to 1 degree and 1 %, respectively. One alternative to increase the voltage
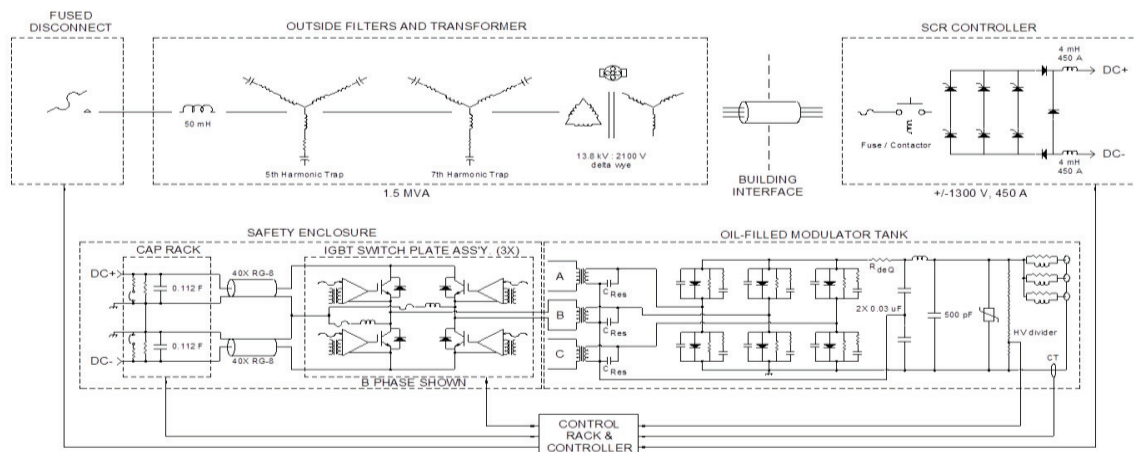

Figure 1: SNS HVCM Block Diagram.

delivered to the klystron at the end of the pulse is to increase the DC bus voltage. However, this results in higher voltage across the IGBTs, reducing their reliability and increasing the probability for a dynamic avalanche failure. Additionally the klystron cathode is overstressed and may cause cathode arcs. Therefore investigating alternate modulation techniques is an attractive solution.
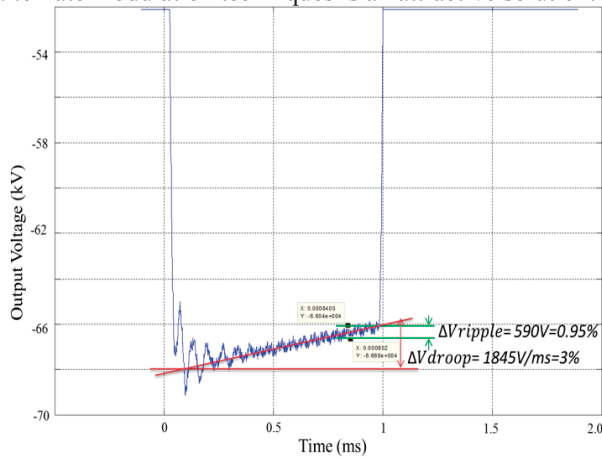

Figure 2: Typical HVCM output voltage. Start pulses not optimized.

FREQUENCY MODULATION

A new state of the art controller is under development to address the present controller shortcomings. In addition to implementing independent IGBT gate control to enable operation utilizing different modulation techniques, it will also provide data storage for HVCM signals during routine operation and fault events. This new controller has faster acquisition, detection and shutdown capability and permits future expansion of HVCM to interface with new intelligent gate drives, series switches and can support an additional redundant H-bridge in the system. The new controller is developed on a Labview PXI chassis with three reconfigurable FPGAs. One FPGA is dedicated to generate gate drive signals for IGBTs, while the other two FPGAs monitor and store the HVCM signals.
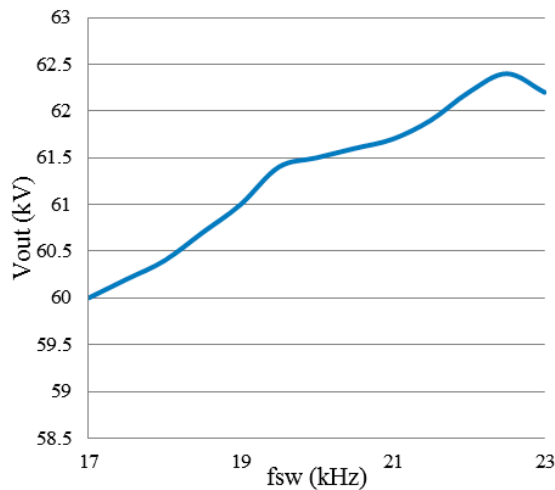

Figure 3: Output Voltage versus IGBT switching frequency, DC Bus = +/- 1000 V.

With an early version of this controller on the test modulator, the output voltage was monitored by changing the IGBT switching frequency from 17 kHz to 23 kHz with a constant DC bus of +/-1000 V. The results are shown in Fig. 3 and indicate maximum gain from the HVCM at 22 kHz. Hence just by increasing the switching frequency we are able to achieve higher voltage. This causes higher switching losses and stresses in the IGBT module but the increased stresses are acceptable [3]. However operating at a different but constant switching frequency during the macro-pulse does not affect the droop rate. Figure 3 also suggests that a frequency sweep for the duration of the macro-pulse can help flatten the pulse. This type of modulation is referred to as frequency shift modulation (FSM). Experimental results with frequency shift modulation induced a higher voltage ripple on the output voltage. This may be attributed to the parasitic inductance from various bus connections, higher commutation current levels in the IGBTs, and the pi trap filters at the output of HVCM which are not optimized for this mode of operation. A high voltage ripple on the output pulse is undesirable as it also affects the control margin of LLRF systems. Test results show that if the frequency change for the duration of macro-pulse was less than 2 kHz, the voltage ripple could be contained to less than 2 %.

PHASE MODULATION

In most cases, the IGBT pairs (pair A+A- and pair A+* A-*) for an H-bridge convertor are turned on and off simultaneously. In phase modulation there is a phase shift Φ between the switching pair as shown in Fig. 4. This reduces the effective duty cycle, permitting control of the energy transferred from the storage capacitor bus to the step-up transformer.
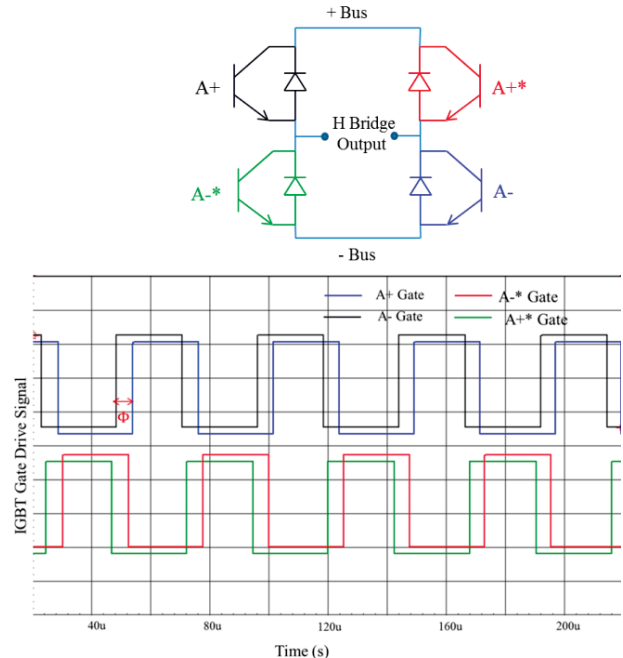

Figure 4: Gate pattern for phase modulation.

Experimental results for phase modulation with a constant DC bus of +/- 1000 V from the test modulator are shown in Fig. 5. The output voltage increases almost linearly with an increase in phase modulation. This result indicates if a phase modulation sweep is performed for the duration of the macro-pulse the output voltage droop can be compensated. This type of modulation is denoted as phase shift modulation (PSM). Phase modulation does introduce hard turn on for trailing IGBTs and increases the device power dissipation. If the phase modulation is not reduced below 90 %, the turn-on and turn-off currents in the IGBTs can be kept less than 1000 A; a level deemed acceptable based on operational statistics.
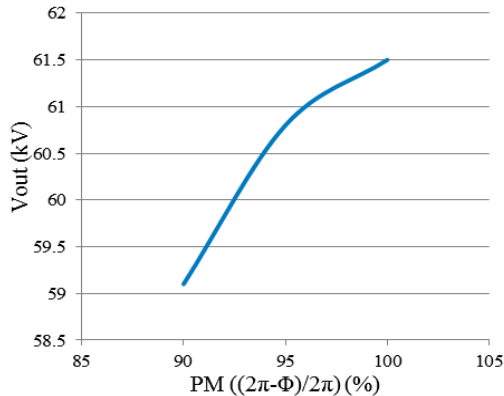

Figure 5: Output Voltage versus Phase Modulation (DC Bus = +/- 1000 V).

PROPOSED ALGORITHM

From the wide possibilities of modulation techniques available with the new controller and the test results from the test modulator, two possible algorithms were selected for further evaluations. Figure 6 shows the output pulse of the HVCM with IGBT switching at constant 22 kHz and a phase shift modulation from 93 % to 100 %. Figure 7 shows combination of frequency shift (20 kHz to 22 kHz) and phase shift modulation (95 % to 100 %). The non-linear droop shown for the frequency and phase shift modulated data indicates a non-linear algorithm will need to be employed to optimize pulse flattening. Different modulators would require different optimum algorithms for droop compensation due to component variations and minor design variations for different klystron loads.
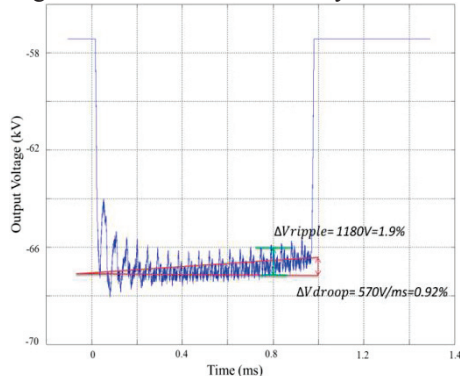

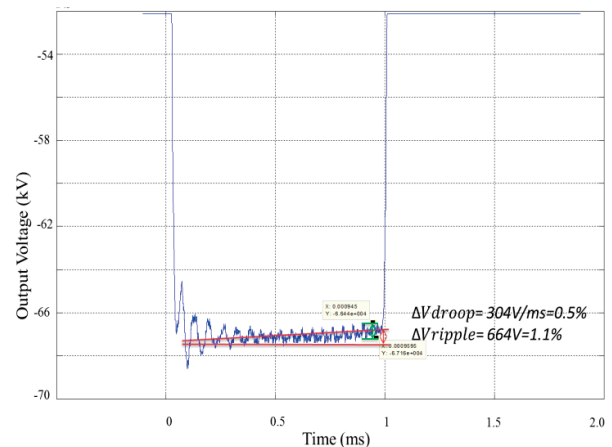Figure 6: HVCM output voltage with fsw = 22 kHz and Phase Shift Modulation from 93 % to 100 %.

Figure 7: HVCM output pulse with frequency sweep from 20 kHz to 22 kHz and phase shift modulation from 95 % to 100 %.

CONCLUSION

Unlike the DSP adaptive algorithm initially tested [4]; the algorithm presented is estimated empirically by monitoring the droop, ripple, gain and IGBT transients. The voltage droop could be reduced from 3 % to 1 % or lower by keeping the turn on and turn off currents less than 1000 A. The experiments were carried out at 60 Hz, full duty cycle for an hour. The next step involves running the test modulator at full power to gain additional operational hours and assess the impact on system reliability. Changing the switching frequency of the IGBTs introduces higher voltage ripple on the output pulse. Ripple reduction techniques like using a laminated bus structure, retuning the resonant circuit and modifying the output trap filters need to be investigated and implemented. These results support the implementation of phase shift and frequency shift modulation for pulse flattening to help achieve 1.4 MW beam power on target.

REFERENCES

[1] V. V. Peplov, et al., "SNS Linac Modulator Operational History and Performance," Proc. PAC 2011 Conf., New York, March – April 2011, p. 1340-1342.

[2] D. E. Anderson, "Developments in Solid-State Modulator technology towards High Availability," Proc. PAC 2009 Conf., Vancouver, May 2009, p. 111-121.

[3] G. P. Patel, D. E. Anderson, D. J. Solley, and M. W. Wezensky, "Operational Results of Pulse Shaping Techniques for the High Voltage Convertor Modulator," Proc. 2012 IEEE Int. Power Modulator High Voltage Conf., San Diego, June 2012, to be published.

[4] W. A. Reass, et al., "High-Frequency Multimegawatt Polyphase Resonant Power Conditioning," IEEE Trans. Plasma Science, vol. 33, no. 4, August 2005, p. 1210-1219.