FAST RAMPING ARBITRARY WAVEFORM POWER SUPPLIES FOR CORRECTION COILS IN A CIRCULAR ELECTRON ACCELERATOR

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Abstract

New fast ramping power supplies working in pulsed bridge technology upgrade the existing Corrector System at ELSA. Current changes of ± 0.8 A/ms are achieved. The newly developed CAN - Bus Interface allows linear interpolation of up to 250 support points with minimal time steps of 1 ms. The first stage uses 24 power supplies to improve the position of the beam orbit in the horizontal plane using dipole correction coils. It will be extended to include the vertical plane with new corrector coils in the near future. This contributed paper describes the operating principles of the power supply and the interface.

MOTIVATION

Polarized ultrarelativistic electrons are used to produce high energy photons, that probe the structure of matter at a very small scale. During their acceleration these electrons pass through a sequence of different magnetic steering fields, which define their orbit within the accelerator. On their way up to the extraction energy of several GeV the electrons encounter depolarizing resonances. These occur, whenever the electrons move through periodically horizontal magnetic fields, that turn the electron spins out of the vertical direction. The horizontal field components may show up in improperly aligned dipoles or if the quadrupoles are not passed in their central region. So the vertical displacements of the orbit have to be minimized using a set of vertical correction magnets.

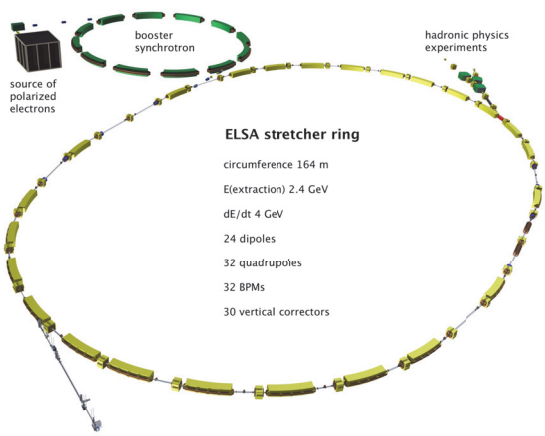

Figure 1: Overview of ELSA. The BPMs measure the orbit of the electrons at the point, where they are located.

The main dipoles are fed with the same current as they are connected in series to their power supply, which ramps up the current to keep the electrons on their orbit during acceleration. The differences of the magnetic field within each of the dipoles can be corrected for using small built-in correction coils. For an idea of how all the mentioned elements make up the accelerator see Figure 1.

The existing system of correctors used separately mounted vertical and horizontal correction coils, that were driven with currents up to ±1.5 A with field integrals of about 2 mTm. The upgraded correction system replaces in a first step the horizontal coils with the built-in ones and will in the near future use newly developed vertical coils, that can carry ±8 A and produce fields integrals of up to 10 mTm. To enable fast field changes newly constructed power supplies had to be installed, that where developed in house. They employ pulsed bridge technology and are programmed using CAN-Bus Interfaces that take advantage of the noise immunity of differential lines and of a sophisticated error detecting protocol.

THE POWER SUPPLY

The power supply consists of a 19 inch crate housing several 16*10 cm sized modules plus a coroidal core transformer (140 V, 600 VA) for the bridge and a TRACO supply (±15 V) for the controller and interface boards. In the following part of this section the different modules are described in some detail.

The Bridge

The advantage of using a pulsed transistor bridge lies in the attainable precision of the current (≈1‰) and in the fact, that the current change per pulse step depends only on the DC voltage supplied to the bridge divided by the inductivity of the coil. The bridge consists of 4 NMOS transistors STY140NS10 which are arranged like the 4 vertical legs of the letter H. The drains of the two upper transistors are connected to the DC voltage supply of 200 V, the sources of the two lower transistors connect to ground. The remaining pairs of drain and source pins are connected. Between these two connection points lies the coil and the shunt, that is used for the measurement of the current through the coil. The coil and the shunt take the place of the horizontal bar of the letter H as depicted in Figure 2.

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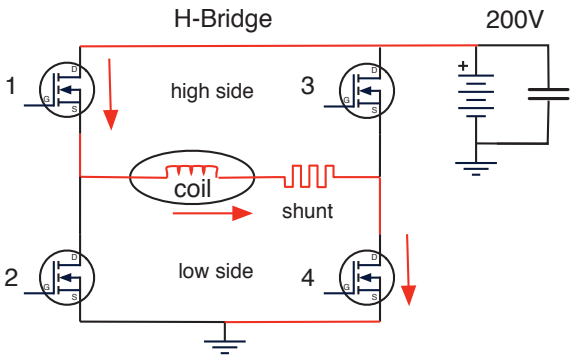

Figure 2a: Schematic of the bridge, current is injected.

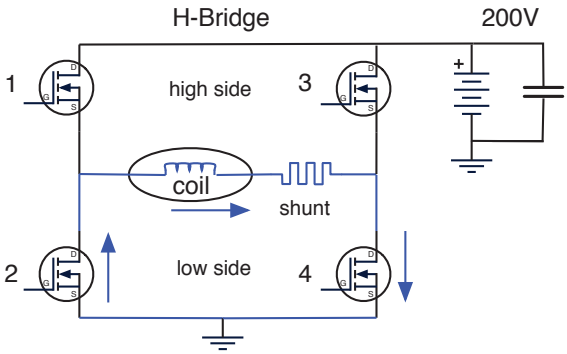

Figure 2b: Schematic of the bridge, current flows freely.

The left and right side inputs of the bridge, the two pairs of gate pins are driven by two special integrated circuits IR2112, *high and low side* drivers, that provide *high side floating supply offset voltages*, each connected to one pin of the coil. In this way each of the four legs of the bridge can be brought in the conducting or non conducting state. If two diagonally opposite transistors (1,4 or 2,3) are made to conduct, the full DC voltage is applied to the coil with the respective polarity. Special care has to be taken to ensure, that at no time both the upper and the lower transistor of either the left or the right side of the bridge are in the low ohmic state.

The timing diagram with the pulses supplied to the gates together with the clock is shown in Figure 3. The upper part of each signal shows the time when the corresponding transistor is in the conducting state.

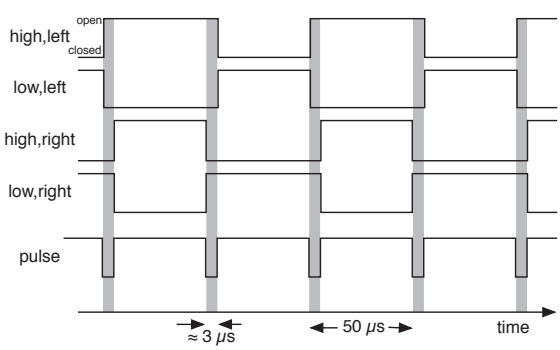

Figure 3: Timing diagram for the bridge.

During the grey painted time intervals in Figure 3, defined by the pulse clock, current is injected into the coil (see Figure 2a), during the rest of the time a circular current flows alternating through the upper part (both upper transistors and the coil) or the lower part of the bridge (see Figure 2b). In case the current within the coil is to be decreased, the timing is the same as shown in Figure 3, but with "left" and "right" labels swapped.

The bridge module gets its supply voltages via the back-plane using a connector equipped with some high current pins leading via screened cables to the coil. The other modules must be screened by a grounded plane, because of the intense noise generated at each change of state of the bridge. The transistors are cooled with a small fan and the module is provided with an over temperature switch to safeguard against thermal runaway.

The Controller

The main component of the controller board is an operational amplifier working as a *proportional-integral controller* that compares the desired input voltage with the actual current flowing in the coil, which is measured using a shunt of 25 mΩ. The sign of the output voltage of this amplifier determines the direction of the bridge: if positive, a chunk of current is to be injected into the coil, otherwise the current is to be decreased. The width of the clock pulses depends to some extent on the difference of actual and desired currents. It gets larger, if the difference is large, and shrinks with differences getting smaller.

The values of the resistors and capacitors, that define the behavior of the proportional-integral controller, have to match the inductivity of the coil. The dipole correction coil only has an inductivity of 2 mH because of the low number of windings, whereas the new vertical correction coils inductivity amounts to 263 mH.

The Interface

To connect the controller board to the control-system of the accelerator an interface board was designed, that uses the CAN-bus protocol for communication. It carries a special PIC18F8680 microcontroller with ECAN capability, that already knows about the low level of the protocol, and in addition also a CAN bus interface chip for the physical layer. In this way most of the complexity of the protocol is hidden from the developer and the user. The processor incorporates 64 KByte Flash RAM for firmware, on board memory of about 3 KByte Static RAM and a 10 bit ADC. The only other important chip on the interface board is a 16 bit DAC, that delivers the desired current value as steering voltage to the controller. A trigger signal is sent to each board, which initiates the output of the desired ramp consisting of an array of length < 256 of pairs of integers (time in ms, current in mA).

The firmware consists of a C program, that handles the communication over the CAN bus interface and that knows to interpret several commands sent from the control system. The ID part of the CAN message string contains one of 62 different addresses (integer numbers 1 - 62 that identify a certain interface board) and a bit combination that choses the intended command. Depending on the command there are sometimes chunks of data to be transferred including checksums over the whole message string. Because there are about 60

spatially distributed units to be dealt with, that are separated into four nearby groups, each command sent from the control system is to be acknowledged by the interface to avoid collisions of packets on the segment.

The most important commands understood by the firmware are the following:

- enable trigger
- disable trigger
- set the DAC to a certain value
- send the measured actual value back to host
- store the ramp in on-board RAM

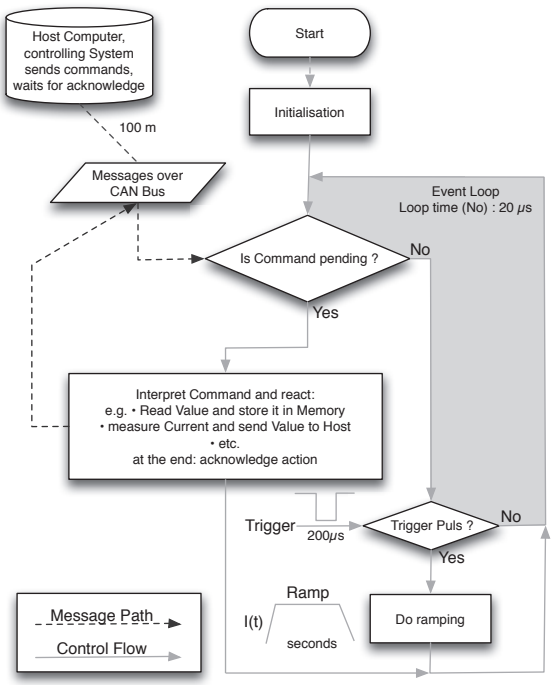

Figure 4: Flow diagram of the firmware operation.

Once a ramp is stored and the trigger is enabled, the firmware calculates on reception of the trigger signal the next piece of the ramp by linear interpolation in time steps of 1 ms (see Figure 4). The ramp consists therefore of a piecewise linear function, where the connected linear pieces themselves are made up from many small 1 ms steps.

To achieve reliable communication over large distances of about 100 m of CAT-7 cable the clock frequency of the CAN bus had to be reduced to 250 KBd, resulting in a transfer time for a ramp of 250 points from the control system into the memory of the processor of 300 ms.

RESULTS

The first experiences with the new power supplies, that are at the moment connected to the 24 dipole correction coils and the "old" vertical correction coils (limited to ±2 A), are very positive.

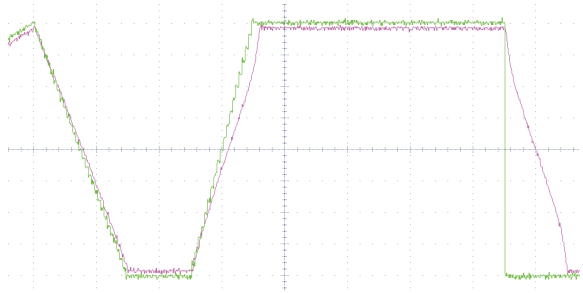

Figure 5: Scope shot of desired (green) and actual (pink) values of the current in a new coil, measured in a laboratory setup. The scales are 2 A/div vertically and 20 ms horizontally. The small deviations seen in the flat regions don't matter, because the magnet current is set by the control system in relation to the beam position.

Once the initial problems were ironed out, operation of the whole system has been reliable. But the full power of the new system will only be apparent when the new vertical correction coils are all installed. As seen in Figure 5 the actual current follows the desired current over the whole range of ±8 A, if the time step for this sweep is set to 30 ms. At a shorter time step of 20 ms a deviation shows up, more pronounced in the trailing part of the jump. A closer look to the green curve also reveals the 1 ms time step of the interpolation algorithm. The third jump of the desired current on the right side of Figure 5 is quasi instantaneous (1 ms). The actual current through the coils tries to follow and displays an s-shaped deviation from a straight line, but nevertheless reaches the lower value after slightly above 20 ms, which equals the design value of (16 A)/(200 V/0.263 mH).

Here lies the speed limit of the system. Ramps with local current change rates steeper than 0.76 A/ms cannot be followed and are smoothed out. But as the shortest time distance between the crossing of an imperfection resonance and and intrinsic resonance at a ramping speed of 4.5 GeV/s is 40 ms [1], this speed is high enough for our purposes.

CONCLUSION

The system necessary for fine tuning of the electron orbit of ELSA has been partly upgraded. The only missing part is the installation of the new vertical corrector coils. This involves mechanic construction work, which takes time, but is under way, and the coils will be replaced one after the other. All the power supplies for the correctors have been installed, are working reliably and are integrated in our control system. As all the development was done at the physical institute, the cost (not counting the work time) stayed reasonably low.

REFERENCES

[1] Andreas Balling et. al., "Precision Closed Orbit Correction in a Fast Ramping Stretcher Ring", PAC'09, Vancouver, BC, Canada, TH6PFP010, p. 3716.

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