DEVELOPMENT OF THE ENERGY-EFFICIENT SOLID STATE RF POWER SOURCE FOR THE JEFFERSON LABORATORY CEBAF LINAC*

X. Chang, N. Barov, D. Newsham, R. Wu, FAR-TECH Inc., San Diego, CA 92121, USA

Abstract

We present the current status of FAR-TECH's Solid State RF Power Source for the Jefferson Laboratory CEBAF Linac. This power source design features up to 8 kW CW RF output power, GaN amplifier stages with high efficiency (>60%), and a compact design to fit existing rack space and cooling requirements at the installation site. We have finished most of the designs and have successfully performed the most critical tests of this project, the 4 to 1 combiner test and the cooling test. FAR-TECH's solid state amplifier design has high efficiency, a wide range of design frequency (DC-3GHz), and long lifetime, which provides a good RF power source.

INTRODUCTION

Thomas Jefferson National Accelerator Facility (TJNAF, JLab) is currently upgrading their RF system [1]. One of the options is to employ multiple solid state amplifiers (transistors) and combine their power with combiners. The main advantages of the solid state option include high efficiency (>60%), long lifetime (in million hour scale per transistor), less graceful degradation., operating at low voltage (48V), and low maintenance cost. These remarkable advantages make the solid state RF amplifier a powerful candidate in the area of the RF power source.

Table 1: Comparison of klystron and solid state options

Parameter	Current Klystron	Solid-state Option: Requirements	Solid-state Option: Amplifier (RF3934)
Frequency	1.497 GHz	1.497 GHz	0 ~ 3 GHz
Peak Power	8 kW	8 kW	8 kW
Bandwidth	>6 MHz	>6 MHz	> 15 MHz
Incremental gain @0.5dB	>4 kW	>5 kW	> 6 kW
Efficiency	~33%	>50%	>60%
Lifetime	>40k Hours	>40k Hours	>50k Hours
High Voltage	11.6/14kV		48V

Table 1 lists the main parameters of the current klystron, the requirements of the solid state option, and the parameters of a module with 64 transistors. From Table 1, it clearly shows that the RF3934 [2] transistor satisfies the requirements completely.

There are some special requirements for this JLab solid state RF project. One of them is that the size of each module should be compact enough to fit in the original klystron spaces. The weight should also be as light as possible for easy installation. The cooling scheme for the modules also needs to be compatible to the existing water cooling system.

*Work supported by DOE Office of Nuclear Physics, DOE-SBIR #DE-SC0002529

EXPERIMENTS

System Configuration

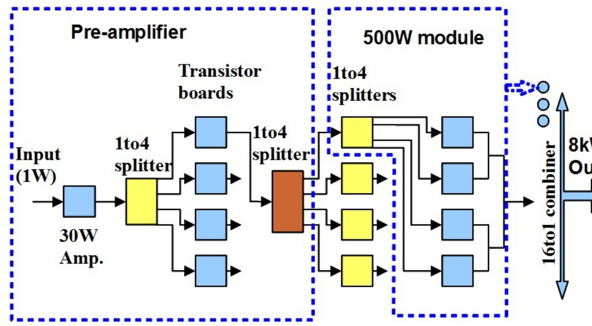

Figure 1: 8kW Amplifier diagram. Pre-amplifier has totally 4 X 4 = 16 outputs and there are 16 of 500W module each 8kW amplifier.

As shown in Fig. 1, the low power (~1W) input signal is first amplified to about 20W by a commercial 30W amplifier. The power is then split to 4 ports, where the peak power of each port can be more than 5W, to drive 4 transistors in the pre-amplifier. Each transistor operates at about 100W with a peak power of more than 120W. The output of each transistor in pre-amplifier is then split to 4 ports to create a total of 16 ports to drive the 16 of the 500W module.

Each input of the 500W module is then split to 4 ports again, where the peak power of each port can be more than 5W, to drive the 4 transistors in each 500W module. The 4 output powers from the transistors in each 500W module, with each output power between 100W to 125W, are combined together by a 4 to 1 combiner to obtain 400W to 500W output power for each 500W module.

There are 16 of 500W module in each 8kW amplifier. The output powers from 500W modules are combined together by the 16 to 1 combiner. The 16 to 1 combiner has been optimized extensively with HFSS [3] to achieve well matched and balanced (unbalance<±0.03dB), wide bandwidth (>20MHz @ -3dB).

Transistor Board Development

The most critical component in this project is the RF3934 transistor board (Fig. 2). Its properties determine the choice of most of the other components. By adjusting the board carefully we've achieved peak power of more than 120W at the circulator output and 105W at output with the gain of 14.5, incremental gain of 0.6, and an efficiency of more than 65%.

ISBN 978-3-95450-115-1

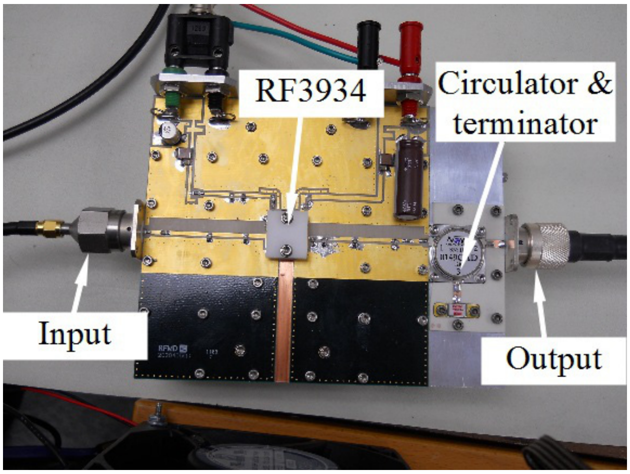

Figure 2: Transistor board with output circulator.

The transistors are not identical; the transistor boards could not be adjusted to be identical either. It is preferable that each transistor module has the same gain, same incremental gain, and the same output power near the operating point. The unbalanced power between each transistor modules will eventually be reflected back and absorbed by circulator terminators.

The drain voltage and gate voltage of each transistor can both be knobs for adjusting the operating point of each individual transistor module. However, for this project, the drain voltage is preferable to be fixed at 48V for all transistors. The procedure to tune each individual transistor module is as follow: First, choose an operating point for all transistor modules, for example, set power of each module to be 105W, set gain to be 14.5 and incremental gain to be ~0.6. The setting depends on the quality of the transistors and the boards. The above setting will produce about 6.5kW power assuming ~0.15dB loss in the 16 to 1 combiner. The next step is to adjust the gate voltage of each module to approach the same setting operating point.

4 to 1 combiner experiment

We first combined the powers of 2 modules together with a commercial 2 to 1 combiner. We successfully obtained total combined power of 230W at the combiner output. The gain was 14.3, incremental gain was about 0.5, and efficiency was 65% at that power level.

In the 4 to 1 combiner test, we followed the same procedures in the 2 to 1 combiner test and combined powers from 4 individual transistor modules through 3 of 2 to 1 high power combiner. Fig. 3 is the picture of our 4 to 1 combiner test.

As shown in Fig. 4, we obtained a combined power of 445W at the exit of the last 2 to 1 combiner. The gain was 14.5, incremental gain was 0.57, and efficiency was 60% at that power level. Taking into account the power losses in the cables and insertion losses in combiners (but not imbalance losses), the sum of the powers at exit of each transistor board was ~475W, and the efficiency went up to 64%, consistent with individual module measurement results. This experiment had been run for more than 27 hours totally, without showing any signs of instability.

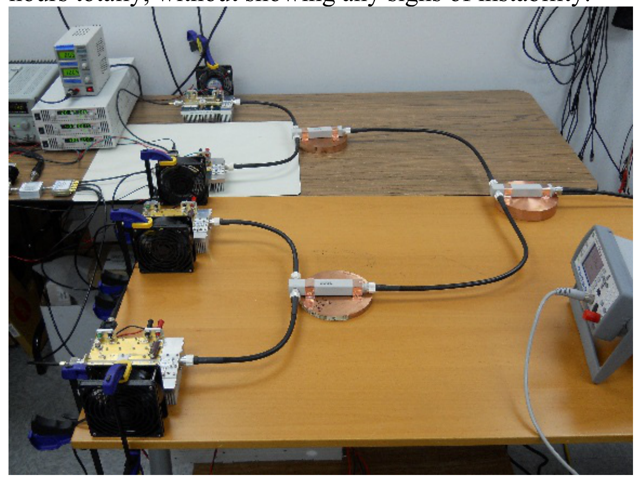

Figure 3: 4 to 1 combiner test setup.

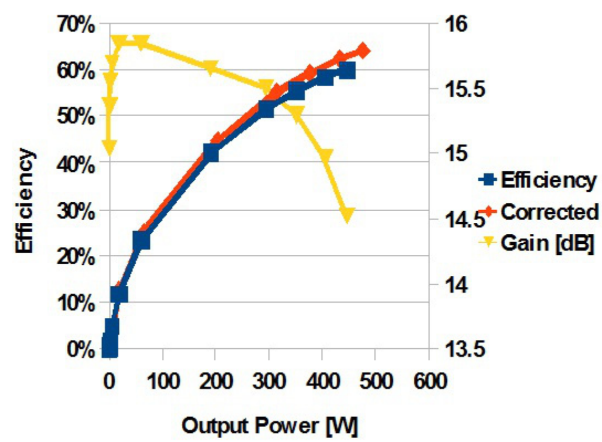

Figure 4: 4 to 1 combiner test results. The incremental gain (not shown) at peak power is 0.57

Cooling system

Cooling is another critical consideration in this project. The transistor lifetime, in terms of Mean Time Between Failure (MTBF), is an exponential function of its junction temperature (Tj), a few degree drop of Tj during operating could extend MTBF by tens of thousands of hours.

For easier installation purpose, it is preferable to separate the cooling system from the 500W modules. To carry it out, the cooling plates with cooling water pipes are fixed on the 8kW combiner. Each plate is clamped on both side by two 500W modules. A film with good thermal property is put in between the cooling plate and the 500W module to improve the thermal transfer.

The maximum rating of the RF3934 case temperature is 85ºC. The cooling water temperature at the installation location is 35ºC. The temperature of the cooling plate is less than 45ºC under the given conditions. This requires the temperature rise (ΔT) between the cooling plate and the RF3934 case to be less than 40ºC.

Figure 5: Cooling experiment. Tested materials include: Indium foil, Aluminium foil, Sil-Pad 900S film, Sil-Pad 2003 film, Thermal compounds.

We have experimentally studied the cooling effects of various cooling schemes (Fig. 5). Various means of making good thermal contact between the plate and module has been studied. Our final adopted cooling solution is not only the most practical solution but also the most effective cooling solution. The maximum ΔT with our final solution was less than 20ºC at transistor heating power of 80W, even at very weak compression pressure between the contact.

Control System

Each transistor board has its own optimized gate voltage (VG). During operation, when the control signal is off, all the VGs need to be off (<-6V). When the control signal is on, VG of each transistor board needs to go to their own pre-setting voltage (-2.5V>VG>-4.0V). There are some other control logics that need be satisfied. These are accomplished by our control PCB boards and the Programmable Logic Controller (PLC). PLC is a flexible and reliable component applied in industrial environment. Our control PCB is also designed to be as reliable as possible. For example, we eliminate all the unnecessary electrical connector connections and replace them with direct wire soldering connections.

CONCLUSION

We have successfully performed the proof of principle test of the Solid State RF Power Source for JLab project, the 4 to 1 combiner test. We achieved combined power of 445W at the combiner output, efficiency of more than 60%, gain of 14.5 and incremental gain of 0.57. It has been run totally for more than 27 hours without showing any unstable sign. We've found the most practical and most effective scheme for the cooling system. Our experiment results show us the bright prospects of this project.

ACKNOWLEDGEMENT

We would like to express our gratitude to colleagues at TJNAF from whom we received technical support. Special thanks to Dr. Rick Nelson for his helpful discussions.

REFERENCES

[1] R. Nelson and A. Kimber, "RF Power Upgrade for CEBAF at Jefferson Laboratory," PAC'11, New York, March 2011, THOCS4, p. 2127 (2011); http://www.JACoW.org
[2] See the RFMD website: http://www.rfmd.com
[3] See the HFSS website: http://www.ansys.com

ISBN 978-3-95450-115-1