

INTEGRATION DESIGN OF BPM AND ORBIT FEEDBACK ELECTRONIC FOR THE TPS

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Abstract

TPS (Taiwan Photon Source) is a 3 GeV synchrotron light source which is being in construction at NSRRC. The orbit measurement and control must be more precise than before in the TPS. New BPM electronic design with the latest generation FPGA and new mechanical form factor to enhance functionalities will be employed for the TPS. The prototype BPM electronics has been testing in the TLS. These testing experiences will be applied in the TPS BPM electronic and software modification. In the other hands, to achieve the stringent orbit stability goal of the TPS, orbit feedback system is designed to eliminate beam motions due to various perturbation sources. The new orbit feedback system is merged to BPM electric system. This design will enhance hardware reliability and fast data exchange performance. The design and implementation plan of the BPM system and the orbit feedback system are summarized in this report.

INTRODUCTION

The new TPS BPM electrical system based on Libera serial technique has been determined to be adopted in the TPS. From Libera Electron, Brilliance to Brilliance+, these electron beam position processors product family which covers the needs of wide variety are applied by many circular light source machines [1,2]. The instruments deliver unprecedented possibilities for both of building powerful single station solutions and complex feedback systems application. Compared to its predecessors (Libera Electron and Libera Brilliance), the latest member of the family Libera Brilliance+ allows even more extensive machine physics studies to be conducted due to large data buffers and the new true turn-by-turn position calculation [3]. It offers a large playground for custom- written applications with Virtex 5 FPGA, Virtex 6 FPGA in the gigabit data exchange module (GDx) for grouping data processing, orbit feedback control, and COM Express Basic module with Intel Atom N270 (x86) inside. First field tests of the new product were performed on real beam at Taiwan Light Source (TLS). The new platform has much extended possibility; orbit feedback controller interface card is a kind of option in the same chassis.

THE BPM INTERFACE DIAGRAM

The system block diagram of BPM is shown in Fig. 1. The BPM includes timing module, BPM signal processing module and inter-connection board (ICB) access module. The GDx interface block diagram is

shown in Fig. 2. That is one option of BPM system for orbit feedback. The FPGA development kit (FDK) serves as a container for custom applications on the GDx module. The container is placed in a well-defined environment, allowing the user's application to easily interact with the system.

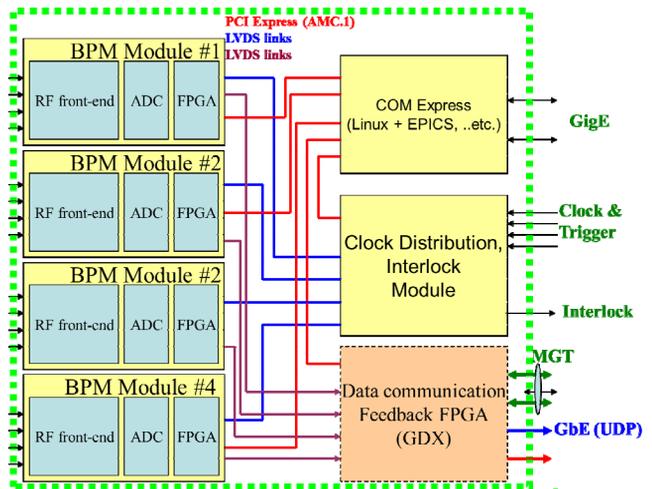


Figure 1: Libera Brilliance+ block scheme.

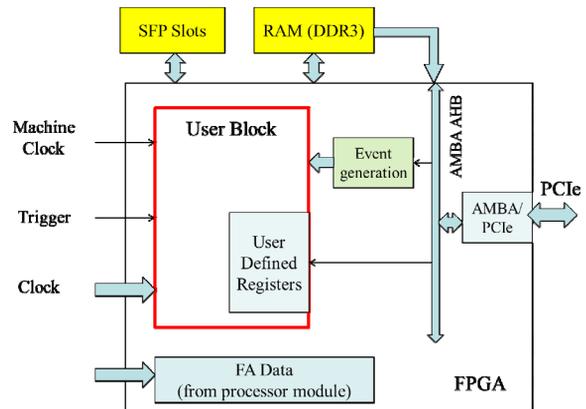


Figure 2: Interfaces of GDx.

The FDK has a write interface to the DDR RAM, enabling write access in a circular buffer fashion. It also has a built-in AMBA/AHB (Advanced Microcontroller Bus Architecture/Advance High performance Bus) slave which can be used for read/write access of arbitrary registers of the user's application. The LVDS bus serves as an input of the Fast Acquisition (FA) data from the processor modules (BPM data), ready for further processing in the application. The ADC clock is a beat of

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the LVDS data stream and for the processed data stream to DDR RAM. The interface to the SFP slots is provided. Two signals from external connectors on timing (TIM) module are also available. These are trigger and MC (Machine Clock – clock at accelerator revolution frequency). Events enable to trigger a certain event exactly at predefined time.



Figure 3: Libera Brilliance+ installation in the TLS with GDX module.

The platform installation, setup and preliminary testing in the TLS storage ring, is shown in Fig. 3. The GDX access BPM information is testing.

There are two approaches to process from ADC data to turn-by-turn data in the fast data of Libera Brilliance+. One is classic DDC approach; another is time domain processing (TDP). Using TDP, one can define which ADC samples are taken into accounts to measure the position. In our case, 1 turn was covered with ADC samples decimation. In case of small partial fill (single bunch or 20% for example), the instrument input does not be like as a continuous but fractions. The shape and length of the response depends on the fill and can be shorter than 47 ADC samples. The position calculation can be optimized for specific fill pattern. To adjust the calculation window, one can use the newly introduced “ADC mask” feature. This parameter defines which ADC sample is taken into account for position calculation (1=use the ADC sample, 0=don't use). The TDP provides the data to the circular buffer at exact revolution frequency and can be also used as source for fast 10 kHz and slow 10 Hz data streams. During the test, the filling pattern was almost CW so all ADC samples in one turn were taken into account. Difference seems not apparently in the regular and flatness filling pattern mode. Various filling pattern and introduced ADC mask will be applied to further study for the proper configuration at different operation mode in the future.

POWERSUPPLY CONTROL INTERFACE

The corrector power supply module is an sophisticated switching power supply with analogue regulator [3]. It will apply for slow correctors, fast correctors, skew quadrupoles. Two kinds of curent sensors are used in the power supply modules, DCCT for high precision power supply module to drive slow correctors, shunt is used for

power supply modules to magnets without stringent requirements. Each power supply sub-rack accomodate up to eight power supply modules. The center slot is allocated to install a special designed EPICS IOC with feedback support. Power supply module installed in sub-rack is shown in Fig. 4.



Figure 4: Photo of a power supply sub-rack.

The special corrector power-supply controller (CPSC) is designed. This module is embedded with Intel XScale IOP and Xilinx Spartan-6 FPGA. It was contracted to D-TACQ [4]. This module will be installed at center slot of the power supply sub-rack. The module embedded EPICS IOC and FPGA supports slow access for the EPICS clients and fast setting from orbit feedback system, and fast setting from the feedforward client. The fast setting from feedback engines with rocket I/O or feed-forward engines with Gigabit ethernet will be sumed together in CPSC to regulator module of corrector. The functional block diagram of CPSC module is shown in Fig. 5.

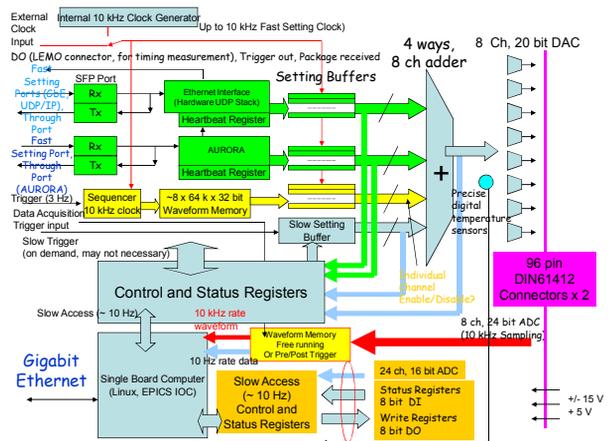


Figure 5: Functional block diagram of the corrector power supply controller module. The EPICS channel access is via an dedicated embedded IOC. The fast setting from feedback engines or feed-forward clients will sum with the EPICS CA slow setting together by FPGA.

The DAC module for power-supply of corrector would be designed for feedback controller, feed forward compensation and other slow settings, the output will be sum from different clients include slow EPICS control for

closed orbit correction, fast setting from fast orbit feedback. The feed-forward table setting can be issued from dedicated EPICS IOCs in advance that is more than one hundred Hz internal control rate feasibly. Beam excitation by noise can be performed by the similar scheme.

INTEGRATION BETWEEN FAST AND SLOW ORBIT FEEDBACK

Aluminum vacuum chamber of TPS would prevent fast magnet field penetration. So, two kinds of corrector were designed to stabilize orbit motion from DC to 250 Hz. Slow correctors are winding on sextupole magnets for DC orbit correction and slow orbit compensation. The slow corrector has slow response with high kick angle. The fast correctors installed at bellow sites have fast response with small kick angle. Integration of two kind loops will keep fast corrector from saturation.

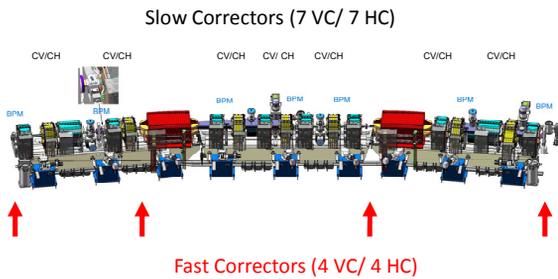


Figure 6: One cell of 24 double-bend cells for TPS lattice layout.



Figure 7: Relationship between major components of the orbit control in one lattice cell.

There are seven slow correctors designed in one cell. The BPM and slow corrector distribution are shown in Fig. 6. There are four fast correctors placed in one cell. Seven BPMs can be used in each cell for the global orbit feedback [5]. Fig. 7 shows major components of the fast orbit control in one lattice cell. Delivery of these components will be available in late 2012. Integration test

will be possible in 2013. Optimize control protocol are the current efforts.

There are two options to implement to deal with orbit feedback. The first option is to combine fast and slow orbit feedback system together and communicate both loops to prevent interference each other. The second option is that the fast orbit feedback covers frequency range from DC to 250 Hz. The DC value on the fast corrector will remove to nearby slow corrector by add fast corrector setting readback information in the loop to prevent saturation of the fast correctors.

Concept of the combine fast and slow feedback loops are shown in the Fig. 8. The BPM platforms can support fast data to fast feedback loop and slow data to slow feedback loop. Corrections for both loops are also updated simultaneously.

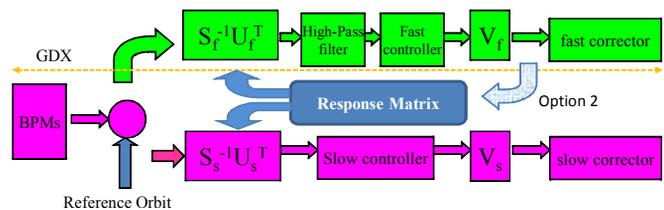


Figure 8: Feedback loop block diagram with slow and fast channel.

CONCLUSION

BPM electronics and integrated orbit feedback system combined with slow and fast correctors of the TPS are summarized. All major components were contracted. Testing is on-going for prototype. All components will be delivered in early 2013. Installation and system integration will be performed in 2013. Platform development is also on going to develop various software supports.

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