

DUAL HARMONIC OPERATION AT SIS18

K.-P. Ningel, P. Hülsmann, H. Klingbeil, U. Laier, C. Thielmann, B. Zipfel,
GSI Helmholtzzentrum für Schwerionenforschung, Darmstadt, Germany

Abstract

The heavy ion synchrotron SIS18 at the GSI facility will be upgraded by a dual harmonic RF acceleration system in the process of using SIS18 as booster for the future FAIR SIS100 accelerator. The dual harmonic mode will extend the SIS18 operating towards higher beam currents.

As a part of a large LLRF (Low Level Radio Frequency) upgrade of the synchrotron RF systems at GSI, new FPGA and DSP based electronics have been designed, built and commissioned. To prove the functionality of the LLRF equipment as well as the general dual harmonic topology, first machine development experiments using the existing SIS18 cavities have been performed at injection energy. In further experiments the proof of principle was shown during the whole acceleration cycle. Based on all these experiments, the main parameters of the control loops were determined. Additionally, the impact of RF gap voltage amplitude and phase variations on the ion beam have been investigated. The experiments showed a high sensitivity of the ion beam to small deviations in phase and amplitude between both harmonics and thereby confirmed the requirements on the high precision regarding the accuracy of the electronic setup especially for the closed loop control systems.

INTRODUCTION

The future FAIR accelerator is planned for operation at beam currents which are two orders of magnitude higher [1]. To minimize space charge effects and the risk of beam instabilities a double harmonic operation at SIS18 is planned: one broad band magnetic alloy (MA) loaded cavity, which is actually under development, will operate at $h=2$ (0.4-2.7MHz) [2]. The two existing ferrite loaded cavities will provide the higher harmonic RF voltage ($h=4$). As a preparation and test for the future control loop topology and to prove the functionality of the LLRF, setup experiments were performed using the already existing ferrite loaded cavities. Due to the bandwidth of 0.8 to 5.4MHz, experiments had to be performed at the harmonic numbers $h=4$ and $h=8$ at a limited extraction energy of 110MeV/u for $^{238}\text{U}^{73+}$.

LLRF SYSTEM

In Figure 5 the principle setup for the present SIS 18 can be seen. This topology is designed for the future FAIR synchrotron and storage rings with respect to the distributed supply rooms and to a flexible usage of all kind of frequency and phase references. It uses the following modules:

- An RF Reference Generator, here called Group DDS (DDS: Direct Digital Synthesis), is provided

with frequency ramps by the central control system (CCS) and generates RF signals at both harmonic numbers. For FAIR applications each supply room will be equipped with an RF reference generator whose phase will be compensated with respect to signal propagation delay and resynchronized by the GSI BuTiS timing reference system [3]. These generators will serve as frequency and phase reference for the DSP-based cavity synchronization.

- DSP-system [4] related to each cavity: Industrial PC with integrated DSP-based interface board (DSP: Digital Signal Processor) and narrow band signal detection and processing (see Figure 1).
 - Mixer Module converting RF signals (0.4 ... 5.5MHz) to an intermediate frequency (IF, 21.4 MHz).
 - Local Oscillator (Offset LO) [5].
 - Automatic Gain Controller (AGC).
 - Frequency Generator providing clock and IF signals.
- Each cavity is equipped with its individual DDS generator. The frequency information is provided by the CCS. The gap phase is digitally controlled by the DSP-systems and precisely synchronized to the Group DDS. The measured phase accuracy is better than $\pm 0.25^\circ$. These cavity DDS modules can remotely be configured thereby determining at which harmonic number the related cavity will operate.
- Amplitude Detector, Controller and Modulator consisting of analogue based electronics.

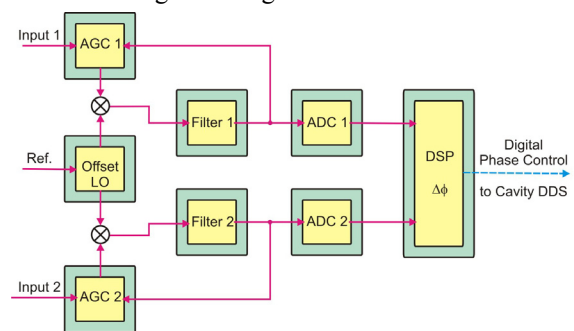


Figure 1 : Simplified set up of the narrow band signal processing of the DSP based PC system for cavity synchronization.

All LLRF devices are designed in a modular way that allows an easy exchange either in case of a defect or if new devices in enhanced technologies are available. Offset LO and AGC consist of FPGA-based devices including high speed and high precision AD and DA converters. These modules, basing on a common platform, were recently developed in the GSI RF

department. New applications on these platforms like digitally controlled amplitude detecting, controlling and modulating devices are in progress. Due to the modular concept a step by step replacement is always possible when new available components proved their capability and reliability.

The resonance frequency control systems of the ferrite loaded cavities are not displayed here. The present modules still consist of conventional analogue control loops. A standardized controller module which is applicable to all different control loops just by exchanging the relevant set of characteristic curves is currently in the design phase.

For optimized dual harmonic buckets phase and amplitude correction ramps are essential to provide a flat potential distribution at φ_s over the whole acceleration cycle. Before starting the experiments, measurements have to be performed for calibrating these theoretically determined ramps. The phase compensating ramps can be loaded into the DSP-system, which is dedicated for the phase control of the second harmonic cavity; the required amplitude calibration ramps can be electronically added to the amplitude ramps provided by the CCS.

MEASUREMENTS AND RESULTS

Major objectives of the planned machine development experiments were to prove the design and the technical requirements on the SIS18 and FAIR LLRF control loop topology and the determination of the impact of small deviations of phase and amplitude on the ion beam.

The experiments were organized in four major stages:

1. Generation of optimized dual harmonic buckets and determination of their influence on the longitudinal beam shape.
2. Determining ion beam losses while single harmonic capturing, creating dual harmonic buckets and single harmonic rebunching at injection level.
3. Phase variations of the dual harmonic RF voltages in small steps and determining the impact on the longitudinal beam shape over the whole acceleration cycle.
4. Determination of the influence of different ramping times at 0.1 T/s and 1.0 T/s.

Table 1 : Experimental Settings and Beam Parameters

Ion Species	$^{238}\text{U}^{73+}$
Injection Energy	11.147 MeV/u h= 4: 848kHz
Extraction Energy	110 MeV/u h=4: 2,475 MHz
Ions per Bunch	$\sim 3 \cdot 10^8$
dB/dt	0.1 T/s and 1.0 T/s, resp.

As a preparation for the experiments all cable lengths were aligned to compensate signal propagation delay differences. Phase and amplitude ramps were recorded to

calibrate the dual harmonic experimental setup. Additionally, parameters of the control loop system like phase and gain were analyzed to find the relevant operating range.

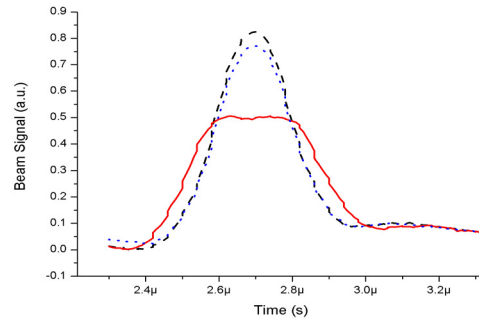


Figure 2 : Optimized amplitude of the second harmonic gap voltage. Total ion beam loss was only about 2%.

Running the machine development experiments the following results could be obtained:

- Proof of principle of the LLRF setup and confirmation of the requirements on the precision of phase and amplitude control loops.
- Successful experimental calibration and application of the theoretically determined correction ramps to phase and amplitude.
- Creation of flat bunches by confirming the theoretical value of 50% RF amplitude for the second harmonic cavity (see Figure 2, RF amplitudes: 7kV (h=4) and 3,5kV (h=8)). The ion peak current could be reduced by about 40% as desired for dual harmonic operation.
- Almost no particles are lost between single harmonic capturing (dashed line in Figure 2), and double harmonic bunching (solid) and single harmonic rebunching (dotted). A value of < 2% could be determined.

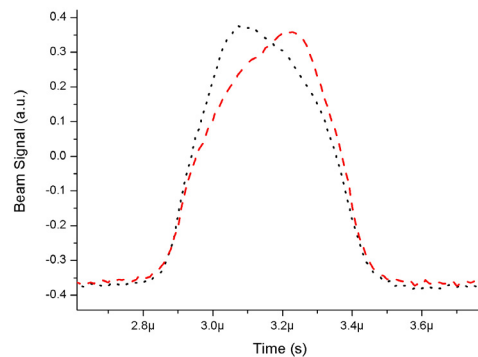


Figure 3 : Phase deviations of $\pm 5^\circ$ from the optimized phase result in significant asymmetric deformed beam shape.

- Variations of phase: As an example the impact of phase on the longitudinal ion beam shape for deviations of $\pm 5^\circ$ from the optimized phase is shown in Figure 3.

- A significant influence of the ramping speed on the longitudinal bunch shape could not be observed (0.1 T/s and 1.0 T/s).

While recording data over the whole acceleration cycle and comparing the gap signals with the related ion beam signal, it could be seen, that a flat saddle point of the equivalent voltage at φ_s and a flat bunch could not be realized on all parts of the ramp (as an example see the dotted curve at 2.475 MHz in Figure 4). Due to the high accuracy of the phase and amplitude control loops, an explanation for this might be a not optimized amplitude calibration ramp. For the moment, this was not the goal of this experiment and can later easily be improved.

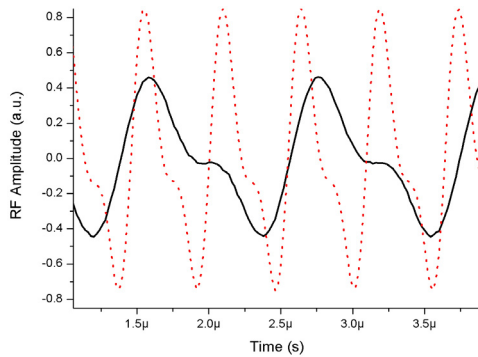


Figure 4 : Measured RF gap voltages at 2 different frequencies (solid: 848kHz; dotted: 2.475MHz).

CONCLUSION AND OUTLOOK

Machine development experiments took place at GSI in the responsibility of the GSI RF Department to run

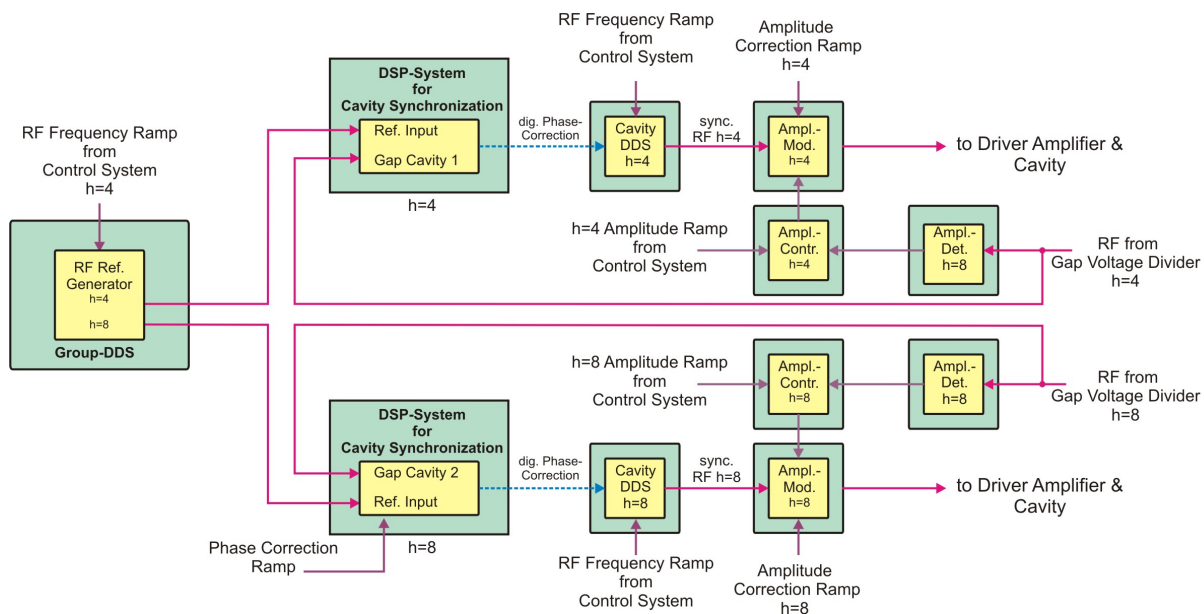


Figure 5: Block diagram of the control loop topology of the actual SIS18 synchrotron. In principle, this topology will be applied to the future FAIR synchrotron and storage rings as well.

performance tests of the newly designed control loop topology for the existing SIS 18 and for the future synchrotron and storage rings at FAIR. The measurements clearly confirmed the proof the principle as well as the technical capabilities of the technical setup and the approach of generating dual harmonic buckets. Additionally the requirements on the high precision of phase and amplitude control could be confirmed. The creation of flat bunches with a reduction of ion peak current by 40% and beam losses of less than 2% could be demonstrated. As a conclusion for SIS18 and for FAIR, it can be said that improvements in amplitude detection and calibration are necessary to finally succeed in a proper formation of the dual harmonic bucket with optimized phase and amplitude calibration ramps over the whole frequency ramp. Further machine development experiments will be performed to prove these assumptions.

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