# SYNCHRONIZED CLOCK SYSTEM FOR ACCELERATION PATTERN GENERATION AND ITS BEAM TESTS IN HIMAC SYNCHROTRON

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*Abstract*

In the routine operation of HIMAC synchrotron, a pulse system of field change with 0.2 Gauss in the monitor dipole magnet (B-clock) is used to generate pattern data in the acceleration system. To eliminate error pulse due to noise in analogue field signal, a clock system locked to a 1.2kHz clock for a power supplies was developed, which can be used to generate pattern data of an acceleration system with maximum frequency of 192kHz. Because the 1.2kHz clock is synchronized to a power line frequency of 50Hz that will be fluctuate about 0.1%, the clock of 192kHz must also follow this frequency fluctuation. To demonstrate the performance of new clock system, we have tested beam acceleration, and compared with the conventional B-clock system. Acceleration efficiencies were checked with changing these clock rates in the both systems. With these tests, we have found that the relatively low clock rate in the newly developed system is enough to get good acceleration performance. In this paper the clock system, and their beam tests will be presented.

## INTRODUCTION

In the routine operation of HIMAC synchrotron, a pulse system by field change with 0.2 Gauss in the monitor dipole magnet (B-clock) is used to generate pattern data in the acceleration system[1]. This system has been working with good stability and reproducibility since 1994, when the first patient was treated with a carbon beam. This good performance comes from the utilization of a digital control system with a direct digital synthesizer (DDS) that has enough reproducibility of the acceleration frequency. Though we have stable beam acceleration with this digital acceleration system, some problems have been recognized in the control of the beam acceleration system. In the control system of the acceleration frequency pattern, the frequency is controlled with a B-clock. This B-clock pulse is generated from an output voltage of a coil settled in a monitor dipole magnet with a voltage frequency converter (VFC).

Errors due to noise in the pick-up coil and electronics are inevitable. The smooth frequency sweep is required for the DDS in the beam acceleration, where B-clock pulse with small field change must be used. This makes the B-clock generator sensitive for the noise. Pattern memory that is used with the B-clock system has specialized functions that switches between T-clock and B-clock controls at start and stop point of the acceleration. Though the DDS itself is accurate, error in its output frequency occurs with B-clock noise pulse. To avoid this deterioration of the acceleration performance, clock pulse synchronized to 1.2kHz clock for power supply is desired to use. This makes also the pattern memory for acceleration system simple.

## RF CONTROL SYSTEM

With an unturned acceleration cavity[2,3], constructed control system is simple. There are only two pattern controls of an acceleration frequency and a voltage. The digital data of 24 bits can be generated with a maximum out-put rate of 1 MHz in these pattern memory. In the frequency pattern, acceleration frequency data are stored as a function of time, and pattern data are generated with synchronous 192kHz clock (see Figure 1). In the case of acceleration voltage, B-clock was used to generate the pattern data. These two pattern data control a direct digital synthesizer (DDS), which generates RF signal with controlled amplitude.

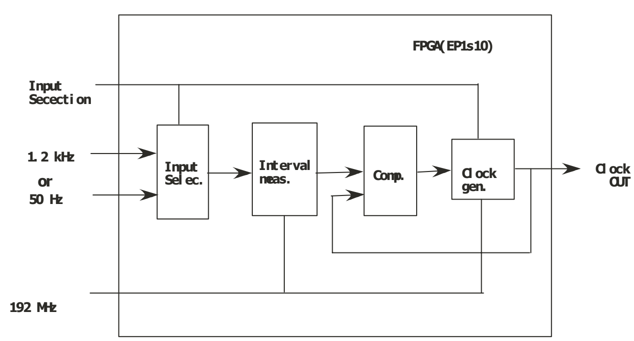


Figure: 1 A Clock generator of 192kHz for the acceleration system.

In the developed synchronous clock system, input clock of 1.2kHz was selected. With this choice, we can obtain accurate tracking between a lattice magnetic field and an acceleration frequency because this 1.2kHz clock is used to generate current pattern of lattice magnets. To obtain this synchronized clock, we have made a clock generator with digital system as shown in Figure 1. In the beginning of experiments, the accuracy of this clock generator was not enough. This reason is due to strong fluctuation of

1.2kHz clock as shown in Figure 2, though slow change of input clock rate was assumed in the system design. To improve this clock circuit, over correction was removed by limiting a correction value of clock rate in one correction step as in Figure 3. The improved performance was checked by counting the output pulse counts of 192kHz and 1.2kHz in same period. With this improvement, correct constant ratio of 160 between above two clocks was obtained.

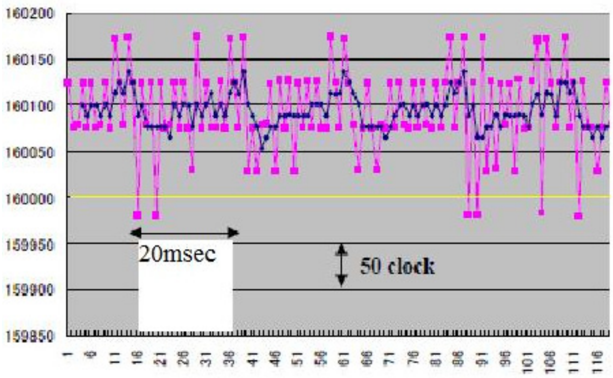


Figure: 2 Measured clock period of 1.2kHz input. Vertical number is counted pulses with 192MHz in the period of 1.2kHz clock. Averaged values with four periods are also shown.

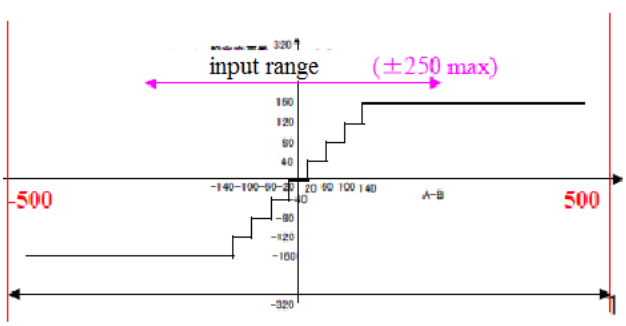


Figure: 3 Output correction count as a function of measured error count.

## BEAM TEST

To test the beam acceleration with a developed pattern generation system, the untuned cavity was used. The transistor amplifier was set at the separated room, and the RF power was supplied with 50 Ω coaxial cable that is about 50 m long. The acceleration is from 6 MeV/u to 400 MeV/u, and the corresponding acceleration frequencies are from 1.04 MHz to 6.6 MHz. To get proper acceleration frequency pattern, two trials were tested. One is with measured current pattern, and another one is with preset current pattern of the dipole magnets. Though the both ways of frequency pattern generations are possible to accelerate the beam, usage of preset current pattern is easy to obtain acceleration frequency pattern. This comes from its simplicity to generate the pattern with linear interpolation of 1.2kHz current pattern. With an obtained frequency pattern, the position errors are about 12mm during acceleration as in Figure 4, and the position errors are compatible with value in the daily operation with B-clock acceleration. To see an excitation of a synchrotron oscillation with a new clock system, we have measured a amplitude of synchrotron oscillation at a flat top. In Figure 5, measured frequency spectrums are shown in the cases of beam acceleration with new synchronous clock and also B-clock systems. In the case of synchronous clock acceleration, the side band spectrum

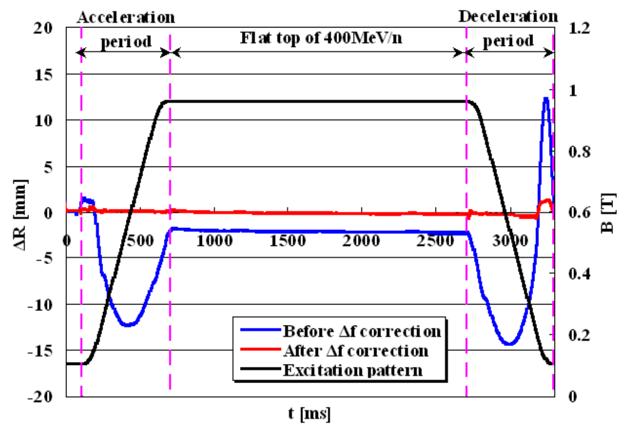


Figure: 4 Beam acceleration with T-clock frequency control. There are measured beam positions with and without error correction in the frequency pattern.

of synchrotron oscillation has lower amplitude by about 10 dB with a developed synchronous clock than the case with B-clock system. This result indicates a smooth acceleration with a synchronous 192kHz clock system. In the case of B-clock system, 0.2 Gauss step clock has been used, and larger clock step than 0.2 Gauss will make lower acceleration efficiency as shown in Figure 6. To see a dependency of acceleration efficiency on synchronous clock rate, we have tested with lower clock rate. In Figure 6, measured efficiency are shown together with the values in the case of B-clock system. Though the acceleration efficiency is degraded with larger clock step with B-clock system, the efficiency will be kept at high value from 192kHz down to 10kHz of the synchronized clock rate. If we see bunch width of the accelerated beam at the flat top, we can see similar tendency in the bunch width. In the case of B-clock system, the measured bunch width become broader with larger B-clock step width (see Figure 7). On the other hand, the bunch widths are almost constant between 192kHz and 10kHz of the synchronous clock rates. In HIMAC synchrotron, maximum field ramping of a dipole magnet is 2.0T/s, and maximum clock rate is 100kHz in the case of 0.2Gauss step. This means that we can utilize lower clock rate for pattern generation with the developed synchronous clock system.

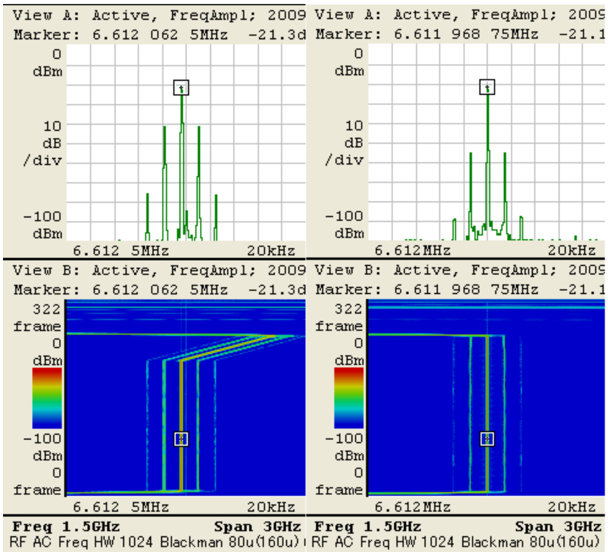


Figure: 5 These are spectrum of beam bunch signals at flat-top. Left data is in the case of B-clock acceleration, and right one is in the case of T-clock acceleration.

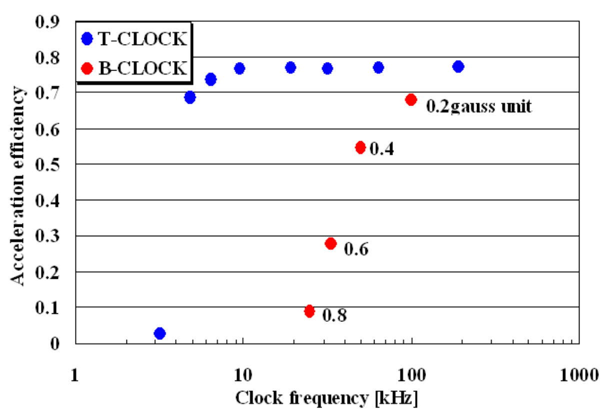


Figure: 6 Acceleration efficiency as a function of a clock rate. In the case of B-clock acceleration, maximum clock rate are indicated.

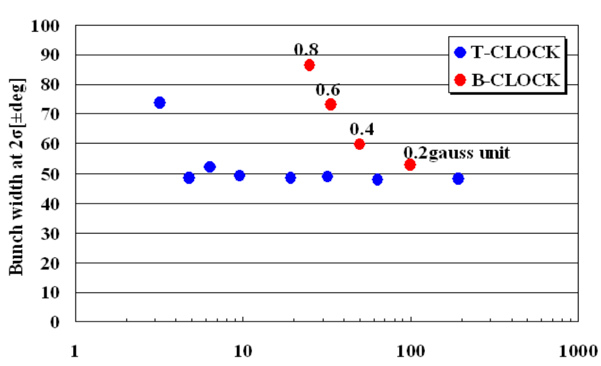


Figure: 7 Bunch width as a function of a clock rate. In the case of B-clock acceleration, maximum clock rate are indicated.

To demonstrate the easiness of pattern generation in acceleration frequency, we have tested beam acceleration with multi flattop pattern. Preset current pattern with eleven flattops is shown in Figure 8, and corresponding beam acceleration can be possible easily as shown in the figure. In this operation, beam was accelerated from 6 MeV/u to 430 MeV/u, and decelerated step by step to 140MeV/u. Though there is no fine frequency tuning to have small deviation of beam position, errors were less than about 12mm during acceleration and step-by-step deceleration. In the Figure 8, beam position with corrected acceleration frequency is shown.

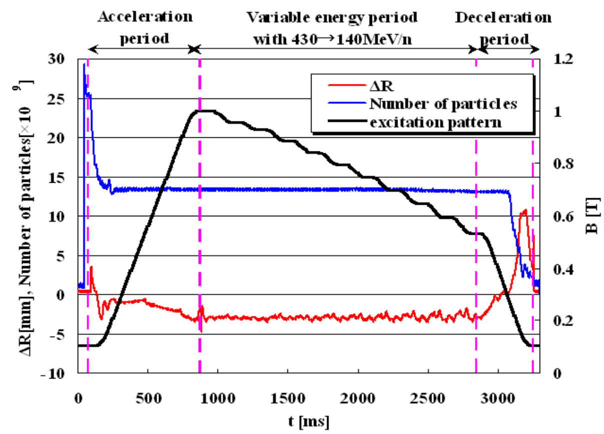


Figure: 8 Current pattern of the power supply for synchrotron dipole magnets. There are 11 flattops where the accelerated beam can be extracted.

## SUMMARY

In the beam test, the new clock generator was tested in the beam acceleration, and good performance was obtained. With this developed clock system, multi flat-top operation is possible. In the acceleration, we have also tested beam acceleration with lower clock rate, and found good acceleration with lowest clock rate of 10kHz.

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## REFERENCES

[1] M.Kanazawa, et al., NIM **A** 443 (2000)205.

[2] T.Misu, et al., NIM A **557**(2006)383.

[3] M.Kanazawa, et al., NIM **A 566** (2006)195.