DIAGNOSTIC SYSTEM COMMISSIONING OF THE EMMA NS-FFAG FACILITY AT DARESBURY LABORATORY

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Abstract

We present a single-shot/turn-by-turn BPM system for the world's first Non-Scaling FFAG Accelerator 'EMMA'. To satisfy the requirement of high rate measurement, the BPM system utilizes a front-end conversion of button pickup signals into compact flat-top-envelope 700MHz bursts. This allows also applying time-domain multiplexing into a single channel. In the BPM, both synchronous detector and ADC clocks are directly manufactured from the beam signal. The system architecture is described; BPM features are discussed; initial results of beam tests done on the ALICE injector have been given.

INTRODUCTION

The Accelerator EMMA [1], the Electron Model with Many Applications, will be used for study of the features of a non-scaling FFAG machine, mainly that of rapid acceleration with large tune variation and serpentine acceleration.

During accelerating, the bunch executes up to ten turns, whilst its horizontal orbit is spirally growing, sweeping about a half of the pickup aperture. For machine tuning, the bunch can be kept circulating in a stationary orbit. The revolution period is T=55.2ns and the intended bunch charge is 15 to 30 pC.

For cell-by-cell bunch trajectory monitoring in the EMMA ring (42 F-D cells) there are total 81 pickups: two pickups in each of 39 cells and one pickup in each of 3 remaining cells. A bunch betatron oscillation along the trajectory for a maximal tune value of 0.4 per sell can be sampled at about 5 points per wavelength. For a constant energy the turn-by-turn oscillation amplitudes measured in each pickup give relative values of the beta function at 2 points per beating period.

BPM SYSTEM

The EMMA BPM system comprises 81 parallel turn-by-turn BPMs installed in seven groups corresponding to the EMMA girder periodicity. Each BPM consists of a pickup, a pair of Front-End modules, and a VME-controlled module where the pickup signals are detected and measured with ADCs. Front-End modules are grouped in crates placed under the girder. Signals from Front-End modules are transmitted to VME modules placed in a rack room via low loss 40m cables.

Each BPM has a built-in buffer memory to record trajectory readings at up to 4k turns. Two pickup signals of each plane are measured individually and then used for position calculation in computer. The paired signals are multiplexed into a single channel. A time-domain multiplexing is used (implemented in the Front-End module) where on each turn, two pickup signals are sequentially transmitted, and then processed and measured, in the single channel. Multiplexing has the advantage in that it cuts significantly the BPM cost. Multiplexing produces also some processing advantages. In particular the problem of precise broadband subtraction of two pickup signals is replaced by a simpler problem of minimising of some multiplexing-by-product zero offset.

Another feature of the system is a novel method of conversion of a short pickup signal into a signal that first could be accurately detected and second would be still compact to avoid crosstalk between the multiplexed signals of each turn. The conversion which is a primary function of the Front-End is done using a cascaded strip line irregular coupler. Its output is a burst of three 700MHz waves whose envelope has a flattened top. Two such signals are multiplexed and then amplified by the Front-End amplifier and finally are detected in the VME module by a synchronous detector. The signal envelopes obtained with use of a low-pass filter are sampled one-by-one with the ADC.

For flattened burst envelope, using an overshot-less Gaussian filter, it is possible in a short burst time (~5ns) obtain a BPM output pulse with a flattened top. This enables reduction of the sampling noise generated by ADC clock jitter.

The EMMA BPM is a beam-synchronised BPM where a synchronous detector reference burst is manufactured from and an ADC clock generated internally is triggered by the BPM input signal. This beam-based approach allows using of single synchronous detector and single ADC and FIFO memory. This noticeably reduces the cost in comparison with a well-known externally-clocked I/Q scheme where a duo of each device is required. The reference burst circuit is based on a pair of precise high speed comparators which provides a minimal time jitter. The ADC clock circuit is made from fast ECL components to minimise the clock jitter. These measures are important as they reduce a voltage noise which is produced by the jitter of each kind.

PICKUP

Space availability and cost considerations have resulted in choosing button electrode pickups. Since a bunch turn-by-turn trajectory sweeps a large part of pickup aperture, it is necessary to use a pickup map to convert measured values to true trajectory coordinates.

To increase sensitivity and effectively load parasitic resonance, the button capacitance is minimized by use of semi-air supporting spacer. The pickup aperture is

D=48mm, the button size is $2\pi/8$, the effective radius $R_{\text{eff}} = 13\text{mm}$. A pickup signal that was recorded on the bench for a pulse 100ps is shown in Fig. 1, left. On the right, a signal of an ALICE injector pickup is shown for bunch charge 40pC. This pickup was used for the beam tests described below.

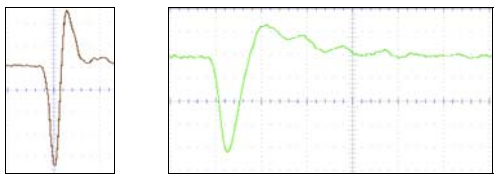

Figure 1: Left: EMMA pickup signal, test bench. Right: ALICE pickup bunch signal at the end of 50m of ECOFLEX-15 cable. Scope TDS6124C, 500ps/div.

FRONT-END

Using a design approach which resulted in a rectangle wave converter [2] for strip line pickup, we developed a triangle wave converter for button pickup. With such a delta-function response, this converter produces a trapezoidal wave for the button pickup signal. A flat top burst envelope of a three stage converter is achieved by compensation of the subsequent stage loss by increase of the coupling strength. [2]

The Front-End is made as a 3U 5HP Euromodule of non-standard length. It contains two converters each of which is made as a pair of irregularly coupled strip lines between two ground planes. A pair of the converter signals is made $T/4 = 13.8\text{ns}$ spaced using a built-in cable delay and then multiplexed in a passive combiner. Its output is fed into a low noise amplifier that is DC-fed through the cable which transmits the signals to the VME module.

For a combiner loss of 3.8dB and amplifier noise figure of 1.5dB the Front-End 'voltage' noise factor $\sqrt{F_{\text{F-E}}}$ comes to 1.9. The amplifier gain is 18dB, and transmission cable loss is about 6dB. At the cable's end, for a pickup signal as above the conversion coefficient is about 0.7mV/pC. The full range is 1.5nC.

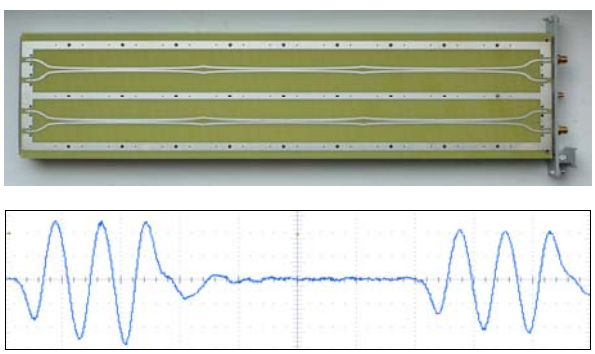

Figure 2: Top: a pair of strip line couplers; cable delay and amplifier are on the opposite side. Bottom: Front-End output for off-center bunch at the end of 50m of ECOFLEX-15 cable. Scope TDS6124C, 2ns/div.

For a batch of 75 modules the average spacing measured with network analyser (E5071C, time domain, triangle wave) is 13.85ns ($std = 0.032\text{ns}$) and the conversion coefficient difference is +1.3% ($std = 0.9\%$).

The converters and a Front-End output signal are shown in Fig. 2.

ANALOG PROCESSOR

The BPM 6U 4HP VME module supports two Analog Processor (AP) boards and one ADC Clock board all made as mezzanine boards. Two ADCs (14bit 2.2V 105MHz pipeline-type) that measure the AP board outputs are placed (together with individual memory) on the module motherboard. This arrangement makes the module a universal measurement station where different sets of mezzanine boards can be specified for different measurement tasks.

The AP board bears a VME-controlled Input Attenuator (–2dB to – 34dB), a Main Amplifier (noise figure 4.2dB, gain 36dB), a Synchronous Detector (triple balanced mixer), and a circuit which manufactures two detector reference bursts from the Amplifier output signal. This circuit also generates two beam trigger pulses for the ADC Clock board.

The Detector output through a Gaussian Filter (rise time 2ns and detector-input-to-filter-output conversion is –12dB) is fed into a Base-Band Amplifier (gain 14dB) and then converted into a differential signal feeding the ADC inputs. The AP single-ended output for the first burst of a beam signal above is shown in Fig. 3 (together with a pickup signal, pink).

With ALICE pickups, for a 20pC bunch and full gain, the AP output reaches half of the ADC range.

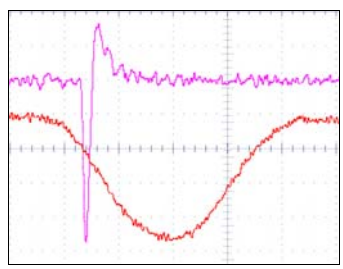

Figure 3: Analog Processor output (red), 2ns/div.

ADC CLOCK AND SAMPLING

Details of pipeline-type ADC work with burst clock are given in [3]. Prior to the beam pulse, the ADC receives an 'awakening' clock pulse from the EMMA trigger. After about 300ns, the beam trigger pulses of the bunch are generated in the AP. They are converted in the ADC Clock circuit into two 'beam' clock pulses spaced by $T/4 = 13.8\text{ns}$. The last pulse circulates in a loop circuit, and produces two more 'extra' clock pulses. If the bunch is single, the circulation continues until number of clock pulses riches the number that is necessary to overcome the ADC latency. With the next bunch in train or the next

turn available, the beam trigger pulses from the second bunch first suppress this circulation and then produce the next pair of 'beam' clock pulses followed again by a pair of 'extra' pulses. This process continues until the last turn happens. The circulation then carries the process to completion in the way as above. When the sampling is completed, the ADC Clock circuit sets the signal READY.

This scheme with 'beam' clock pulses provides an automatic and stable time correlation of the sampling moment and the beam signal.

The ADC Clock circuit counts bunches/turns and gives out this number for reading by the VME interface. The bunch/turn pulses are generated by the coincidence of two 'beam' clock pulses. The last bunch/turn is found using anticoincidence of each previous and consecutive bunch/turn pulse.

The ADC samples four times per turn. The samples are: $V1 = P + S1$; $V2 = P + S2 + s1$; $V3 = P + s2$; and $V4 = P$, where $S1$ is the button signal, $s1$ is its tail, $S2$ is the opposite button signal, $s2$ is its tail, P is some pedestal. Using $K = s1/S1 = s2/S2 << 1$, the bunch signals are:

$S1 = V1 - V4$,

$S2 = (V2 - V4) - K \cdot S1 = (V2 - V4) - K \cdot (V1 - V4)$

The coefficient K is calculated as

$$K = \frac{(V2 - V4) - \sqrt{(V2 - V4)^2 - 4 \cdot (V1 - V4) \cdot (V3 - V4)}}{2 \cdot (V1 - V4)}$$

The bunch offset in the button plane is:

$$y = R_{\text{eff}} \cdot \frac{S1 - S2}{S1 + S2}.$$

BPM RESOLUTION

Detailed BPM resolution consideration is done in [2]. Here we give some summary for the EMMA BPM.

The Front-End thermal noise at the AP Main Amplifier output calculated for the maximal gain in the base-band (170MHz) is $std_{\text{MAb-b}} \approx 3.2\text{mV}$. With attenuation setting, the output noise comes to a plateau about 1.3mV that is the thermal noise of the Main Amplifier. In the case of a jitter-free reference, the noise at the Synchronous Detector output is $std_{\text{SD}} = std_{\text{MAb-b}}/4 = 800\mu\text{V}$ and $330\mu\text{V}$ respectively. This is significantly larger than the Base-Band Amplifier noise and the ADC bit resolution noise $150\mu\text{V}$ and $30\mu\text{V}$ respectively (both being referred to the detector output).

A full bandwidth full gain Main Amplifier output noise $std_{\text{MAf-b}} \approx 8\text{mV}$ is converted by the comparators into a reference burst time jitter and a beam trigger time jitter. For an output burst slew rate 2V/0.5ns each jitter amounts to $std_{\text{RJ}} \approx std_{\text{TJ}} \approx 2\text{ps}$. Noise produced by the jitter of the first kind at the Detector output can be found applying an approach used in [2]. The output is proportional to $[1 - 4 \cdot std_{\text{RJ}}{}^2 / \tau(T_{\text{R}} - \tau)]$ where T_{R} and τ are the period and slop length of the input trapezoidal wave. For the output signal 0.25V the noise is about $10\mu\text{V}$.

ADC Clock jitter is a combination of the beam trigger jitter described earlier and some additional jitter originated in the ADC Clock circuit. Total jitter estimation is about 4ps. If the AP output pulse shown in Fig. 3 is sampled exactly at its apex, the noise generated by this clock jitter is negligible. A sampling point positioning error increases the noise, approximately linearly with excursion from the apex. For example, for the error 0.8ns the noise referred to the Detector output is $std_{\text{sample}} \approx 100\mu\text{V}$.

Concluding, one can say that the EMMA BPM resolution is decided by mainly the Front-End and Main Amplifier thermal noise. For bunch charge 20pC (the output pulse magnitude is about half the BPM range) the BPM resolution is expected to be about $30\mu\text{m}$. To keep the contribution of the sampling jitter minimal, the BPM is equipped with a VME-controlled clock delay that is pre-configured to allow scanning of the output pulse and setting the sampling point on the apex.

The BPM resolution plateaus at about $12\mu\text{m}$ for bunch charge greater than 100pC.

SUMMARY

The development of the EMMA BPM system is close to completion. The board/module prototypes have passed initial beam tests, the nearest task is commissioning of four BPMs on the EMMA Injection Line.

This single-bunch/turn-by-turn BPM can be used for diagnostics of circulating bunches in small machines and for bunch-by-bunch measurement of high rate trains. Being affordable, this BPM can replace a known Log-Ratio BPM and provide better accuracy and significantly higher resolution. Note for high charge bunches the attenuator-amplifier chain can be modified which provides the improvement of the plateau resolution at least twice.

ACKNOWLEDGEMENTS

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