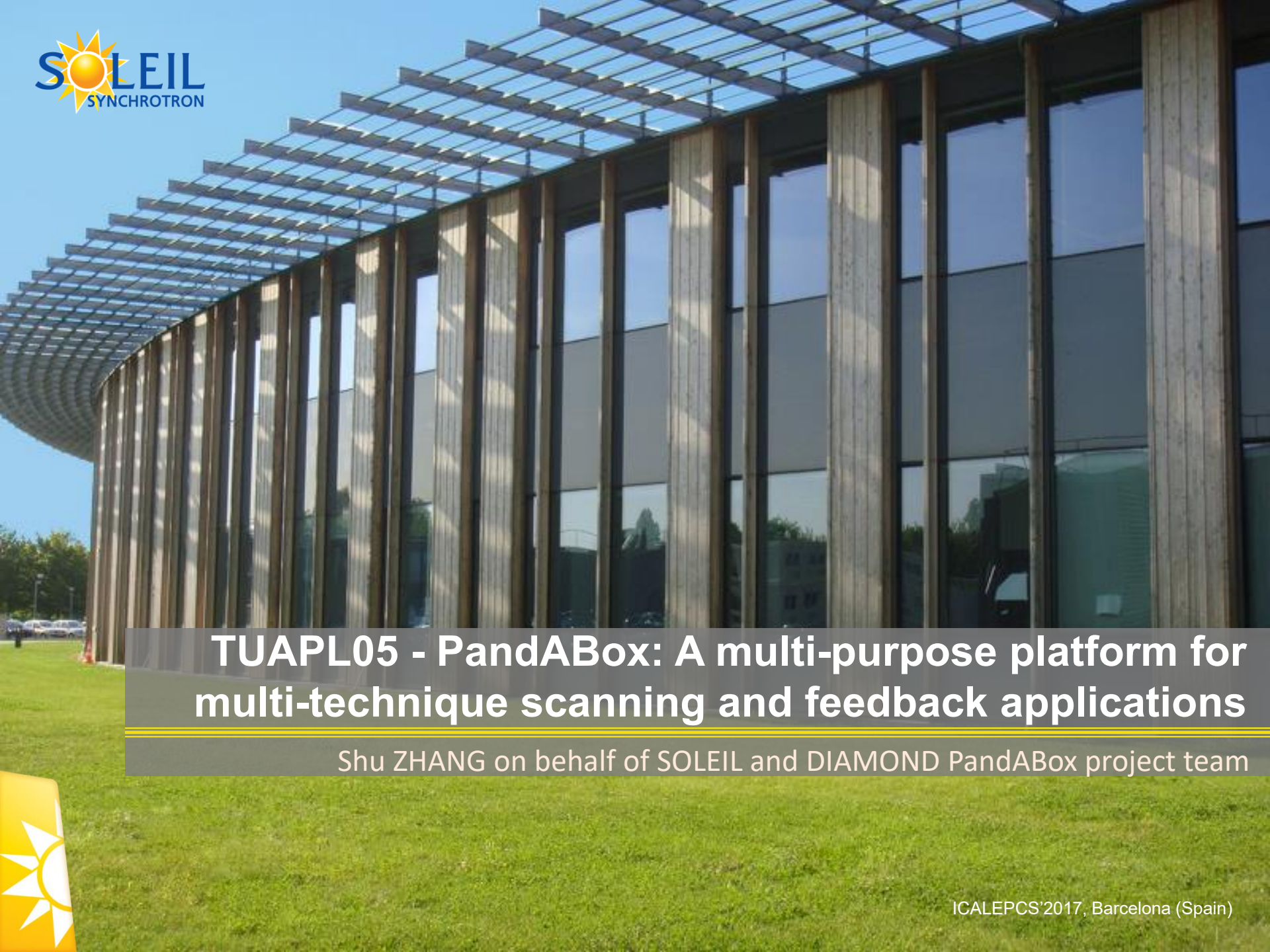


TUAPL05 - PandABox: A multi-purpose platform for multi-technique scanning and feedback applications

Shu ZHANG on behalf of SOLEIL and DIAMOND PandABox project team

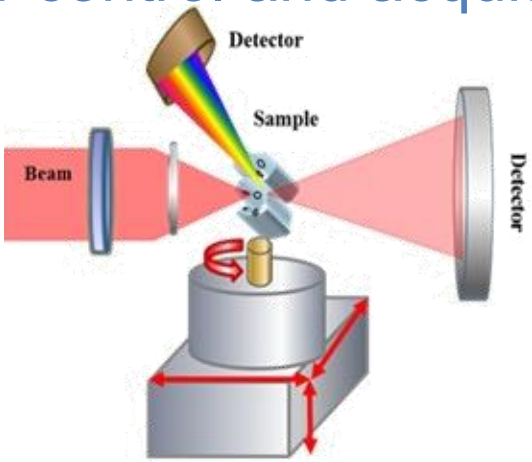
ICALEPCS'2017, Barcelona (Spain)

Outline

- Project introduction
- Hardware designs
- Firmware and software
- Applications at SOLEIL
- Summary and next steps

Introduction

- Main challenges for control and acquisition



Mechatronic instruments *to select photon energy (mirror, monochromator, etc.) and for the sample stages environment*

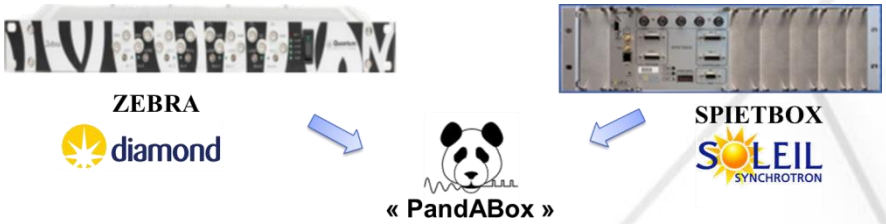
High-throughput ***detectors***

Synchronize *sensors and detectors with mechatronic instruments to acquire only* ***useful data*** *and to perform* ***fastest continuous acquisition***

- Initial objectives
  - Connecting **Motion Control** Systems and **Data Acquisition** Systems for simultaneous and multi-technique scanning applications
  - Providing Encoder Processing, Common Synchronous Triggering and Data Captures

Introduction

- Motivations
  - Managing obsolescence and limitations
  - Maintaining modularity
  - Improving performance
- Organisation
  - Development collaboration between SOLEIL and Diamond

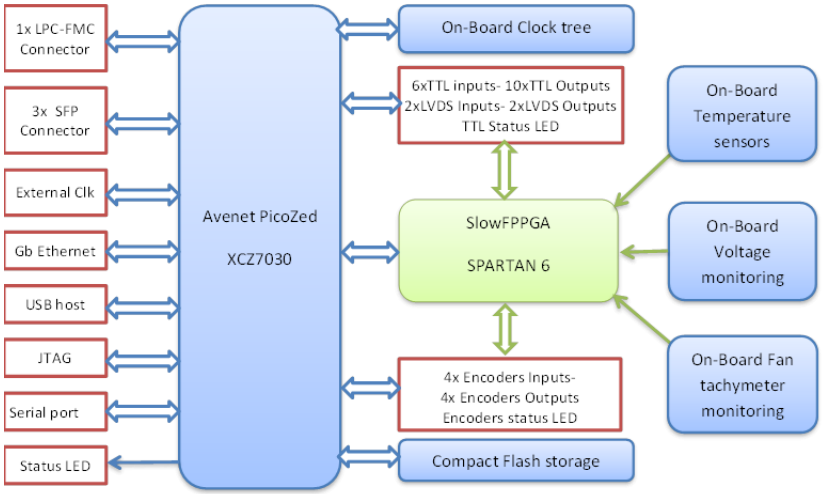


  - Task sharing
    - SOLEIL: Electronics and Mechanics
    - Diamond: Firmware, Software and Web GUI
- Status
  - Prototypes (HW, FW, SW) designed and validated, ready for production
  - Project shared on OHWR: https://www.ohwr.org/projects/pandabox/wiki

Hardware designs

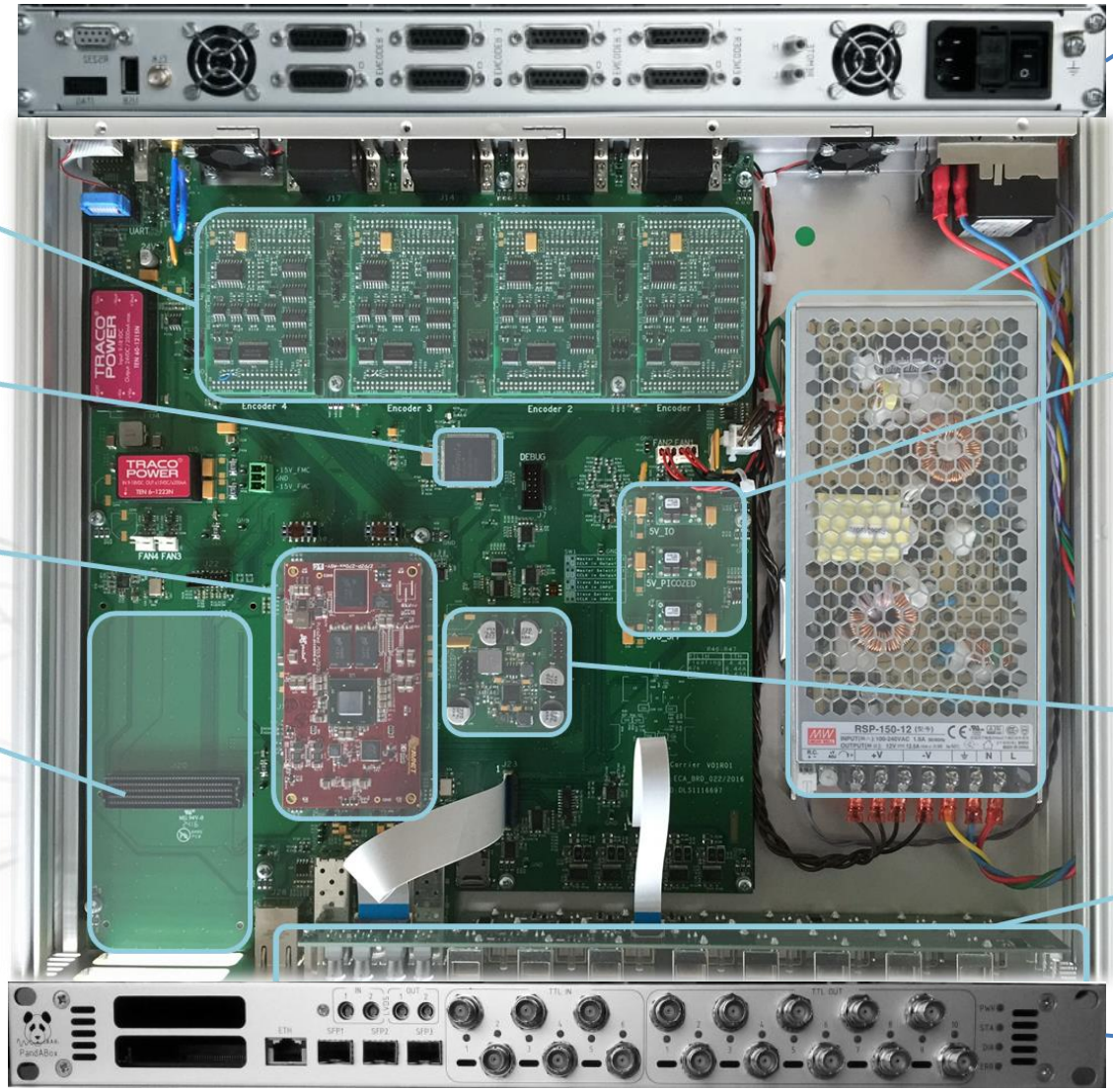
Hardware architecture and I/Os

- Platform developed around an off–the-shelf product:
  - Avnet PicoZed Z7030 module based on a powerful Xilinx Zynq 7030 SoC (System On Chip)
- HW architecture around PicoZed and I/O interfaces
  - 4-Channel Encoders I/Os (Quadrature, SSI, BiSS-C, EnDat)
  - TTL and LVDS I/Os
  - FMC LPC slot
  - On board clock tree & power supplies
  - 3 SFP ports
  - 1 Gigabit Ethernet for Control and DAQ
  - Slow control via a Xilinx SPARTAN-6 FPGA:
    - Temperature monitoring
    - On-board power supplies voltage monitoring
    - Fan-speed monitoring
    - Configurations of the I/O encoder signals
    - Front panel configurations
  - JTAG for SoC and FPGA debugging
  - RS-232 serial console terminal
  - USB host for firmware upgrades



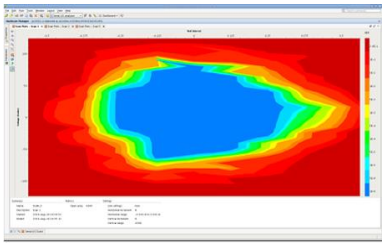
Main modules and I/Os

- Packaged in a 19” 1U rack (top view)

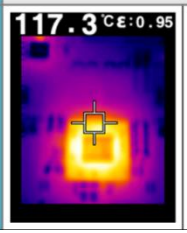
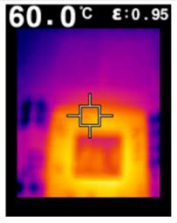
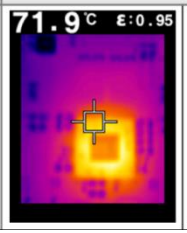
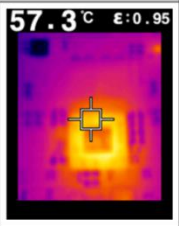


Prototype validation

- Prototype entirely tested (at Diamond and SOLEIL)
  - SoC **boot-up**, all **communications** and **I/O** interface tested with Diamond released **firmware**
  - **Fiber optic transceiver** test:
    - SFP transceiver + loopback FW + Xilinx IBERT IP
    - Validated at 6.25Gbps & 2.5Gbps, GTX-CLK0@125MHz, up to 550m cable



  - **Heating** issue:
    - Overheating on **commercial-grade** PicoZed
    - Internally developed firmware
    - Currently searching for better heatsink solution, currently employing **industrial-grade** PicoZed

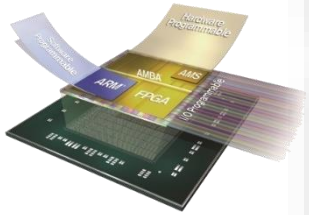
PicoZed grade	Commercial	Industrial	Commercial	Industrial
Firmware	FMC_250MHz (Generation and reading of 250MHz differential signals on FMC card in addition to sending Gigabit Ethernet UDP multicast frames over SFP port)		SFP_UDPonTrig (sending Gigabit Ethernet multicast UDP frames over SFP port)	
Temperature on the Zynq SoC of the PicoZed module				

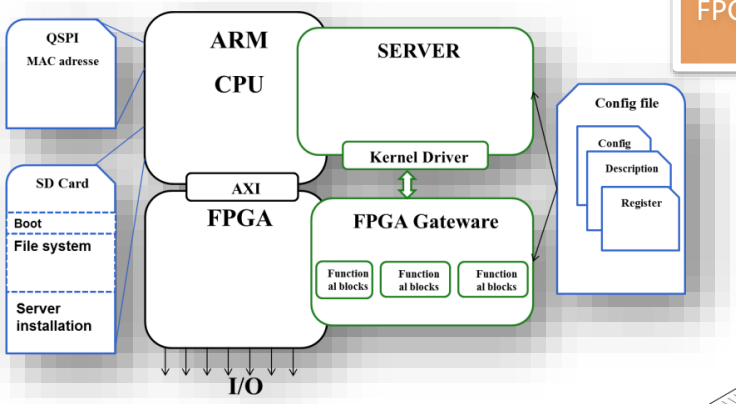
Firmware and software

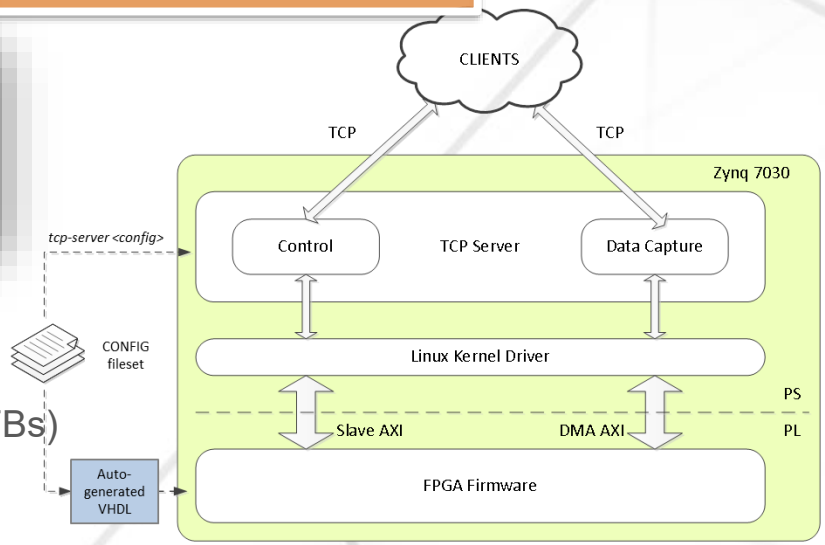
Firmware architecture

- Flexible and configurable architecture

THPHA068- PandABlocks Open FPGA ramework and Web Stack







  - **FPGA firmware layer**
    - Structured into numerous Functional Blocks (FBs)
  - **TCP-Server layer**
    - **Two** socket **endpoints** to connect to clients (EPICS, TANGO, etc.)
      - configuration **control** (control & status register)
      - streamed data **capture** (interface with DMA engines for synchronous R/W)

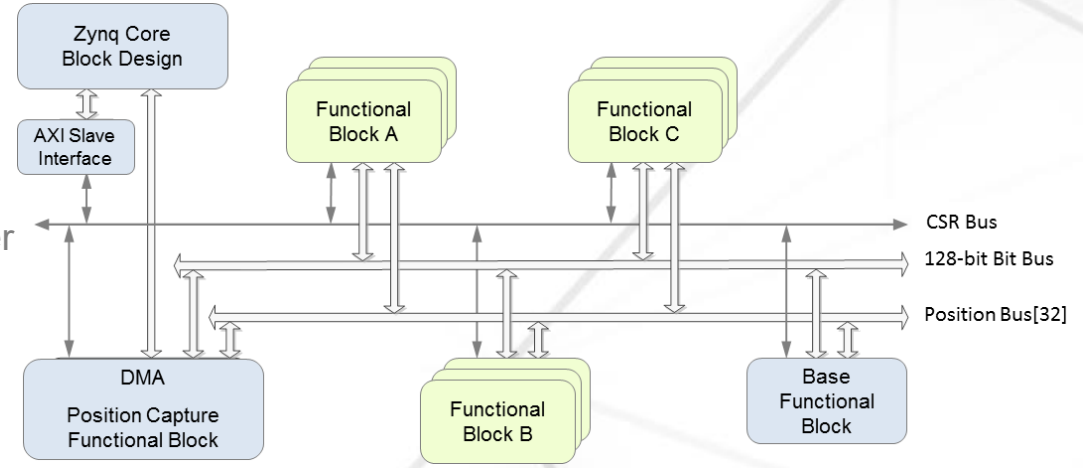
⇨ 2 layers **tightly coupled** through **a common set of configuration files** (FB's I/O ports, configuration registers, and descriptions)

⇨ Allowing to **design and compile** a custom set of **FBs** into the **firmware** with **access from the TCP Server**

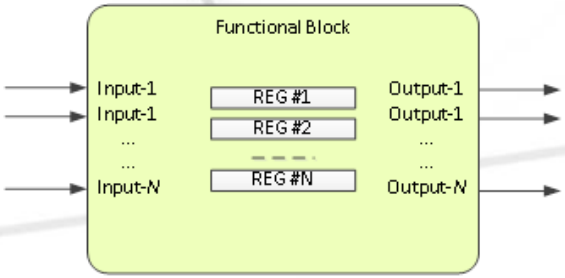
- Fully **re-wirable** (at run-time) architecture

Firmware Functional Blocks

- Physical and logic interface connected together by:
  - 128-bit Bit-bus and Position-bus
- Logic block functionalities
  - ADDER - Position Adder [x2]
  - COUNTER [x8]
  - DIV - Pulse divider [x4]: 32-bit divider
  - LUT - 5 Input lookup table [x8]
  - PCAP - Position Capture
  - PCOMP - Position Compare [x4]
  - SEQ - Time frame sequencer
  - etc.

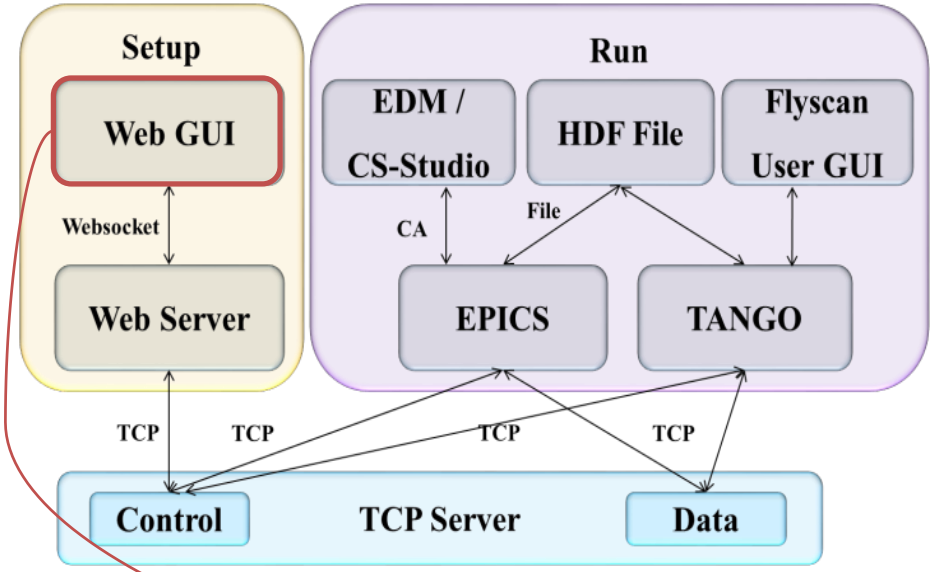


- Custom Functional Blocks can be added
  - Each FB contains:
    - Discrete bit-type input and output ports
    - 32-bits wide position-type input and output ports
    - Configuration and status registers



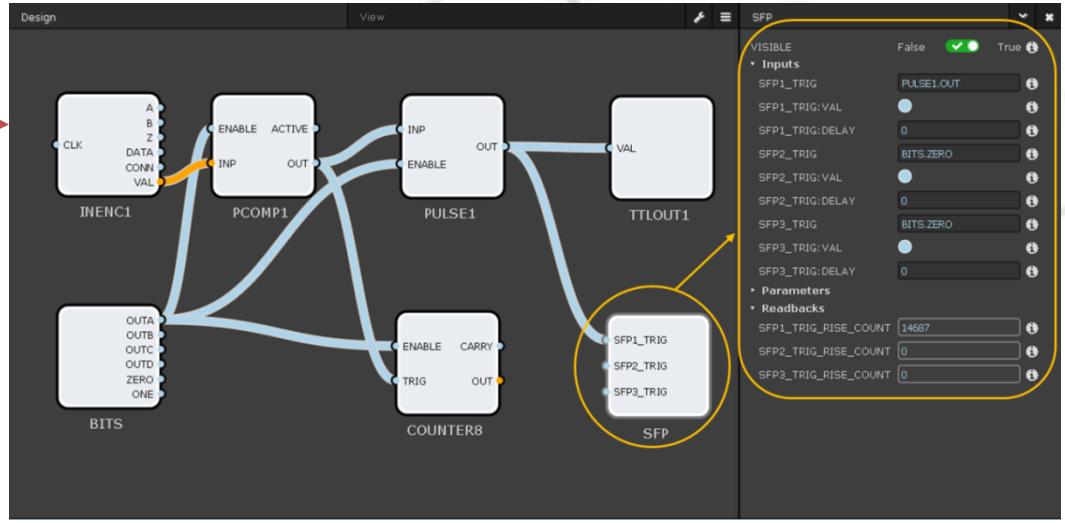
  - Dedicated FBs developed at SOLEIL to adapt application requirements
    - FPGA-Development-Kit available on OHWR
    - Web-GUI tool

Software architecture



- **TCP Server**
  - To interface with either **TANGO** Device Server, **EPICS** IOC, or web-server

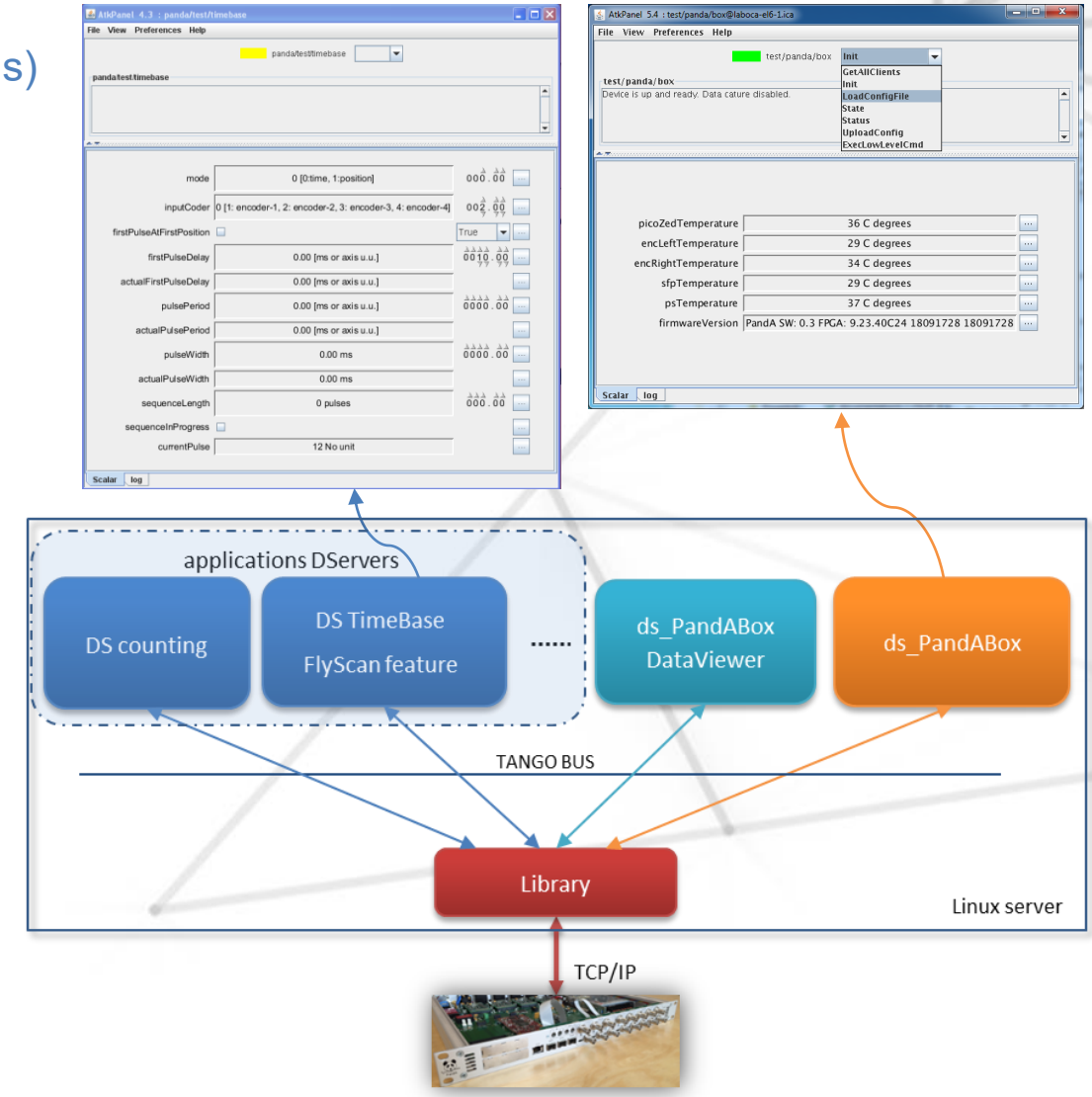
- **Web GUI**
  - **Visualizing** and **wiring** the functional blocks
  - **Setting** the functional blocks' **parameters**
  - Help to **build** customized **applications**



TANGO control software

- 3 types of Device Servers (ds)
  - ds_PandABox
    - Hardware configuration and monitoring
  - ds_PandABoxDataViewer
    - Generic DServer

    to create customized interface for expert diagnostics and specific configurations
  - Applications DServers
    - ds_PandABoxTimeBase
    - ds_PandABoxUDPTimeBase
    - Counting application
    - etc.

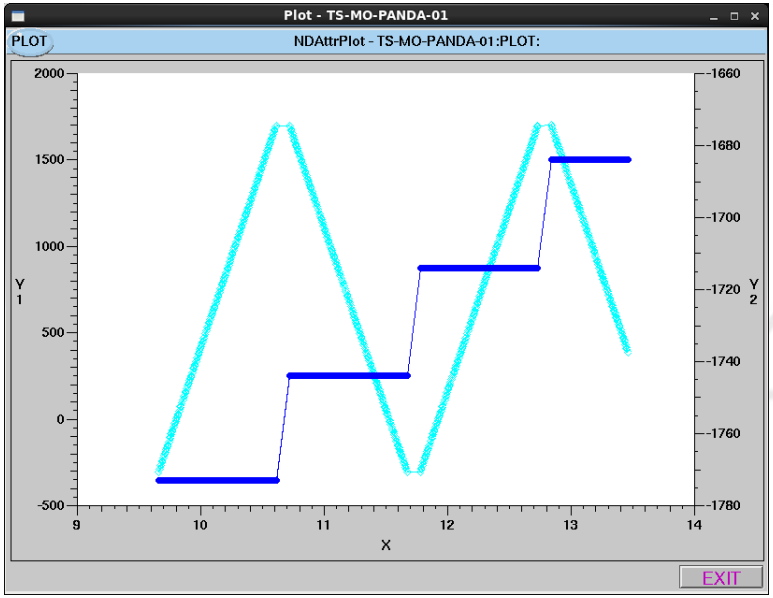


EPICS control software

- The ADPandABlocks EPICS

areaDetector driver captures a series of NDArray frames, each stamped with an NDAttribute for each captured position.

These can then be selected for plotting using the NDAttrPlot plugin, and written to file using the NDFileHDF5 plugin (both included as part of areaDetector)



Applications at SOLEIL

Applications at SOLEIL

- Hardware encoder processing
  - Adder, filtering, averaging, protocol conversion, etc.
- Continuous scanning (FlyScan) applications
  - Hardware synchronization triggers generation
  - Software synchronization notifications over UDP multicast frames
- Feedback applications

Continuous scanning application

FlyScan or Malcolm framework (TANGO DServer, EPICS IOC, etc.)

Ethernet Bus (TANGO, EPICS, etc.)

Software synchronization

Motion control

Sensor

2D detector

UDP Triggers

Time

Position

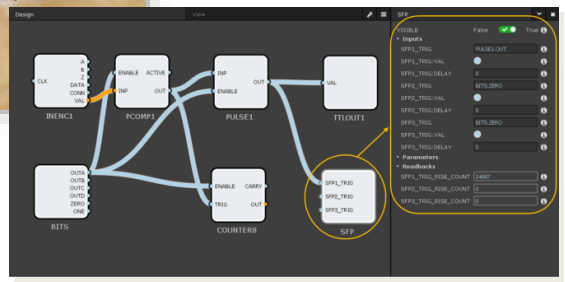
PandABox

Encoder signals

Hardware synchronization (Master clock bus)

Quadrature, BiSS, SSI or EnDat encoder signals

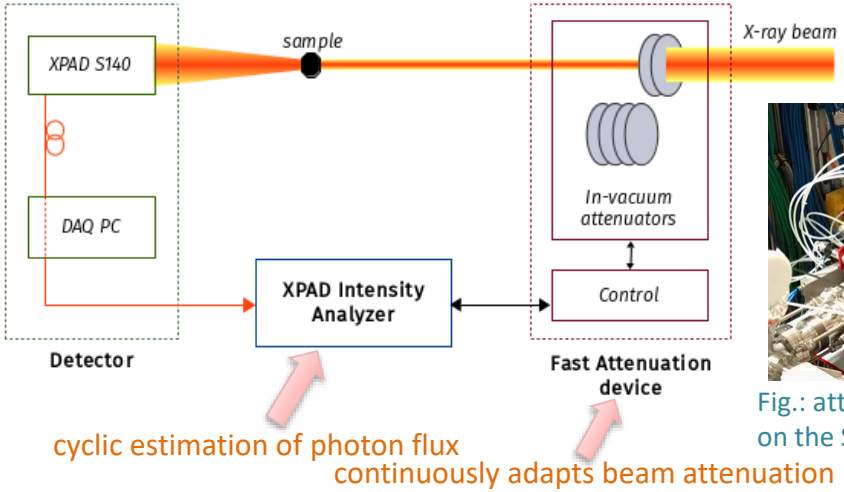
Firmware setup



Feedback application

- **Upgrade** and improvement of the real-time control system for the fast beam-attenuation with an XPAD detector

Global architecture of the XPAD controlled beam-attenuation system



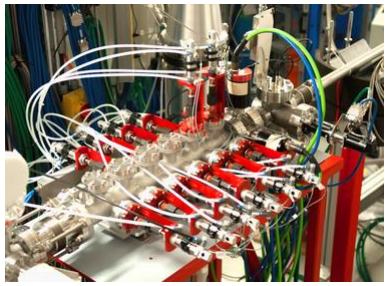
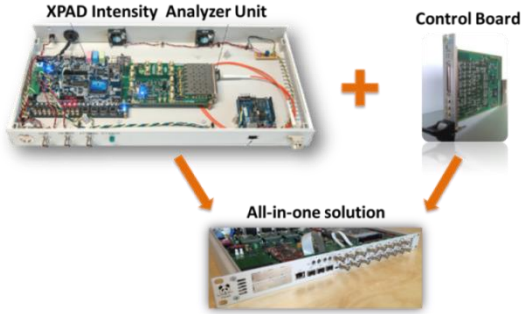


Fig.: attenuation system installed on the SixS beamline at SOLEIL

Upgrade **advantages**:

- Technical support in operation
- All-in-one solution
- Performance improvements



Upgrade **steps**:

- **Migration** of the detector intensity **analyzer** firmware
  ⇨ To be completed, tests with the detector on the beamline in progress
- **Improve** the analyzer by modifying its calculation **algorithm**
- **Migration** of the **control** board functions
- **Integration** of the full solution

ILA captured detector data frames with PandABox

Summary and next steps

- Initial objectives achieved, resulting system:
  - well adapted for multi-technique scanning and feedback applications
  - **flexible** design solution, **open** and **extensible** platform
    - Modular hardware with removable modules
    - Firmware and software easily configurable and adaptable
- TANGO DServers: development to be finalized
- Call for tender: to be prepared
- First applications implementation: ongoing
  - FlyScan applications commissioning
  - Upgrade and improvement of the real-time control system for the fast beam-attenuation with the XPAD detector
- D-TACQ FMC-ADC modules integration: ongoing
- Diamond status:
  - Deployed on 4 beamlines, being planned for the rest of the beamlines (10 interested so far)
- Both institutes
  - Improvements to have a more easily configurable system are being discussed

Acknowledgements

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Guillaume Renaud

Thanks for your attention

CERN OHWR project available

https://www.ohwr.org/projects/pandabox/wiki

Collaborate like "PandA"