MicroTCA generic data acquisition systems at ESS

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Outline

- MicroTCA overview
- ESS MicroTCA requirements
- Generic data acquisition platforms overview
- System showcase

MicroTCA Overview

EUROPEAN SPALLATION SOURCE

Why MicroTCA ?

"*MicroTCA is a modular standard.*

By configuring highly diverse collections of AdvancedMCs in a MicroTCA Shelf, many different application architectures can be easily realized.

The common elements defined by MicroTCA are capable of interconnecting these AdvancedMCs in many interesting ways—powering and managing them, all at high efficiency and low cost."

MicroTCA Overview

EUROPEAN SPALLATION SOURCE

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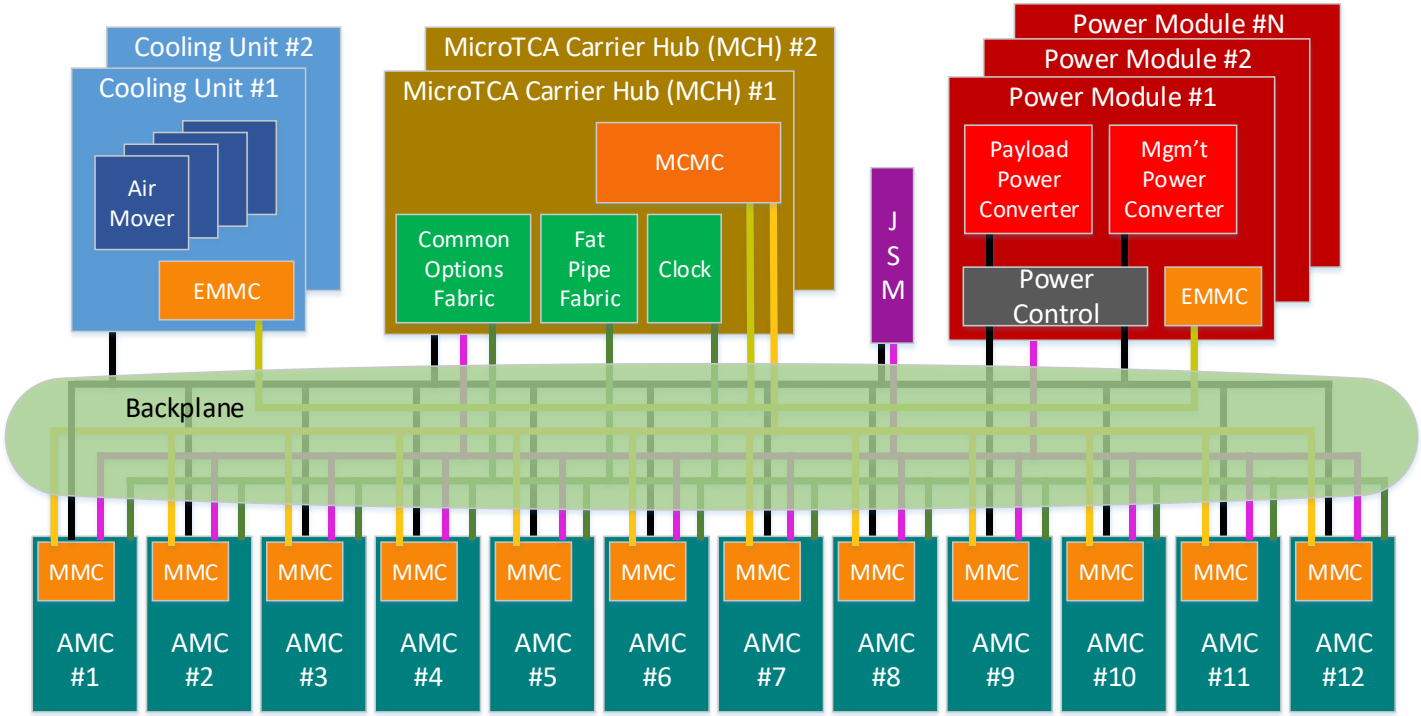
Main features:

- High availability
- Redundancy
- Manageability
- Serviceability

MicroTCA Overview (2)

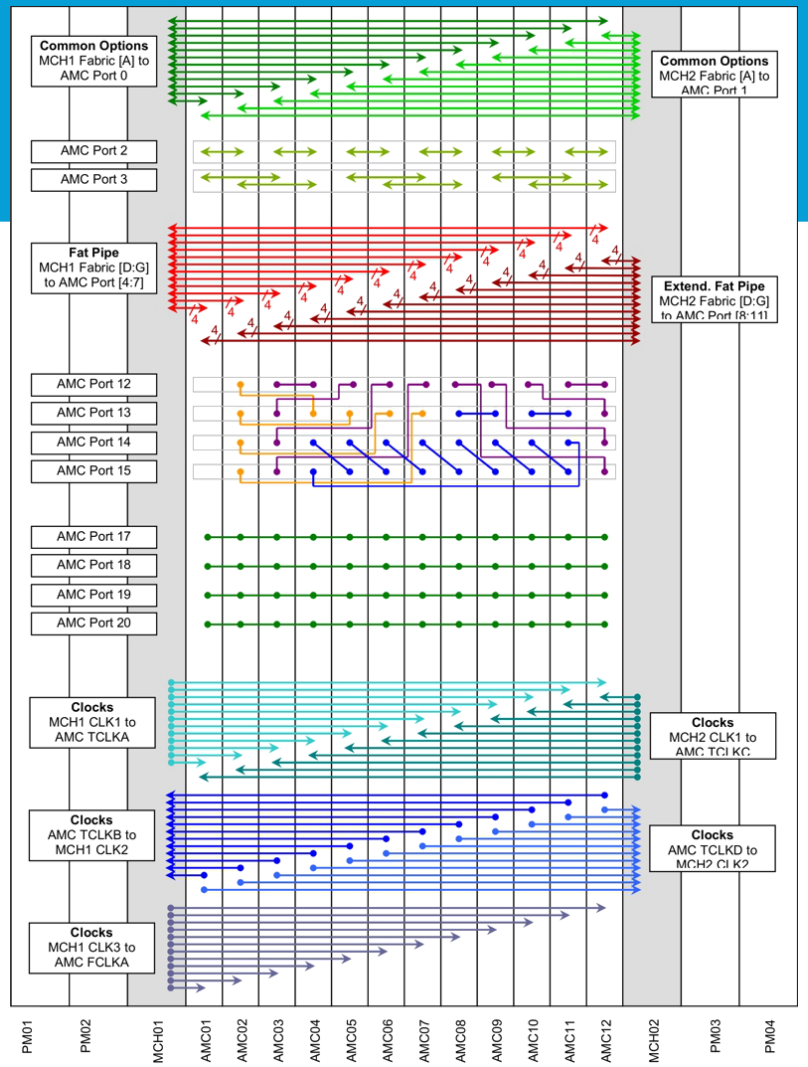


- IPMI management on IPMB bus
- Board presence detect and enable signals

MicroTCA Overview (3)

Common backplane interconnections:

- 2 GbE links, 1 towards each MCH (Common Options)
- 2 high speed AMC to AMC links
- redundant 4 lanes bus mediated by MCH for bulk data transfers (Fat Pipe and Extended Fat Pipe)
- 4x LVDS type AMC to AMC links
- 8x MLVDS lanes
- 4x AMC Clock I/O lines
- 1x FAT Pipe Reference CLK



ESS MicroTCA requirements

~500 MTCA systems to be deployed covering:

- Beam Diagnostics
- Machine Protection
- RF Systems
- Timing System

Systems availability greater than 95%

Use of standard COTS infrastructure equipment:

- MCH
- Power Modules
- Chassis
- CPU

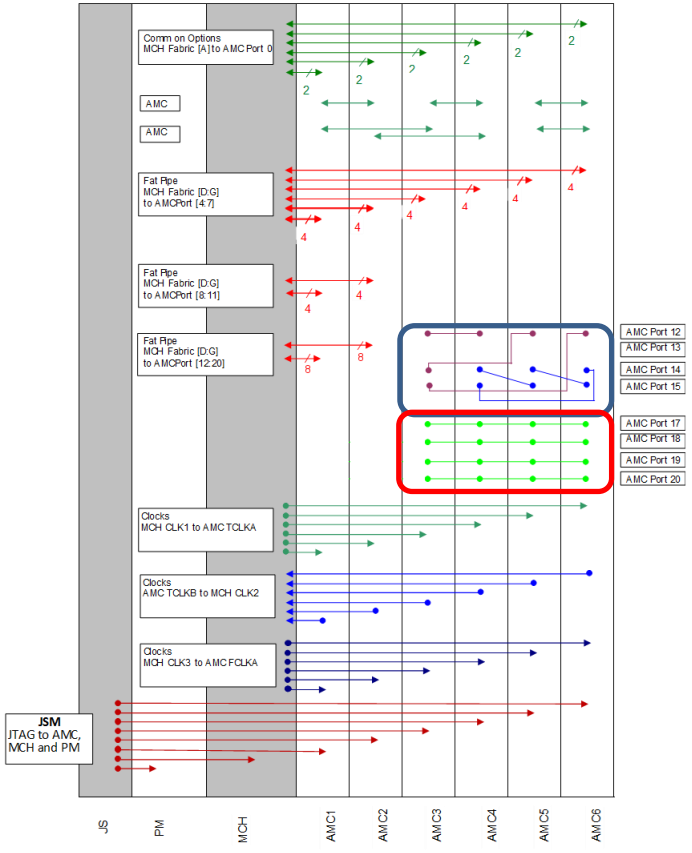
ESS specific COTS and In-Kind equipment:

- Event Receiver
- AMC Digitizers
- FMC carrier
- RTM cards

ESS MicroTCA Requirements (2)

3U backplane interconnections:

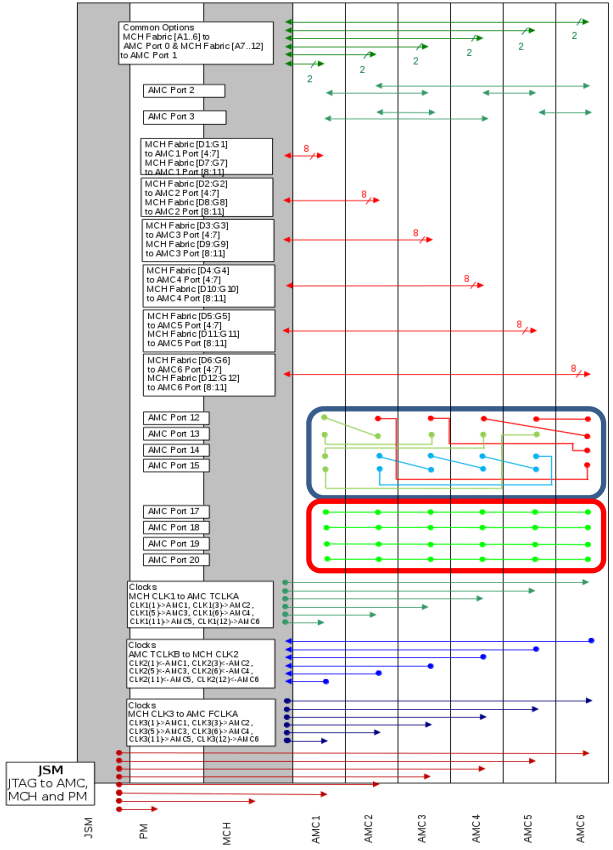
- 2 GbE links
- 2 high speed AMC to AMC links (BP specific)
- PCIe 16x and 4x
- 4x LVDS type AMC to AMC links
- 8x MLVDS lanes
- 2x AMC Clock lines
- 1x FAT Pipe Reference CLK



ESS MicroTCA Requirements (2)

ESS backplane design:

- 2 GbE links
- 2 high speed AMC to AMC links (BP specific)
- ~~PCIe 16x and 4x~~
- ~~4x LVDS type AMC to AMC links~~
- ~~8x MLVDS lanes~~
- 2x AMC Clock lines
- 1x FAT Pipe Reference CLK
- PCIe 8x to all AMCs
- 4x LVDS AMC to AMC provided to all slots
- 8x MLVDS lanes span all AMCs



Generic data acquisition platforms

- IFC1410

FMC Carrier:

- T2081 NXP PowerPC CPU architecture
- Xilinx Kintex Ultrascale Central FPGA

CPU section:

- 2GB DDR3L dedicated memory
- Directly connected to the GbE on the backplane
- PCIe connection to Central FPGA

Central FPGA section:

- 2 x 512MB DDR3L dedicated memory
- Directly connected to Fat Pipe region on the backplane (PCIe)
- MLVDS lines to Extended Options for triggers
- 2 HPC FMC cards connections
- Infrastructure for D1.4 compliant RTM

Generic data acquisition platforms

- IFC1420

Digitizer and FMC Carrier:

Based on same architecture of IFC1410

One HPC FMC slot occupied by custom daughter card with AD/DA converters

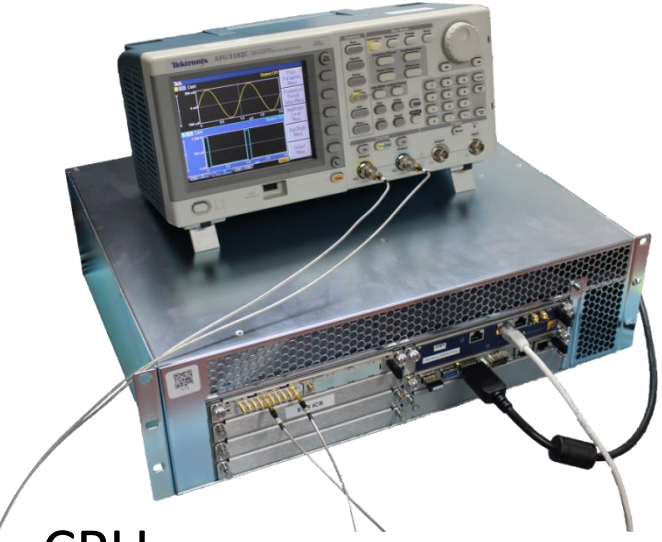
Analog connections from RTM compliant to DESY A1.1CO

Clock distribution scheme allows use of Backplane or RTM supplied clocks

DAQ 1430 features:

- 10ch 16-bit 250Msps ADC
- 4ch 16-bit 2.5Gsps DAC

IFC1410 system test stand



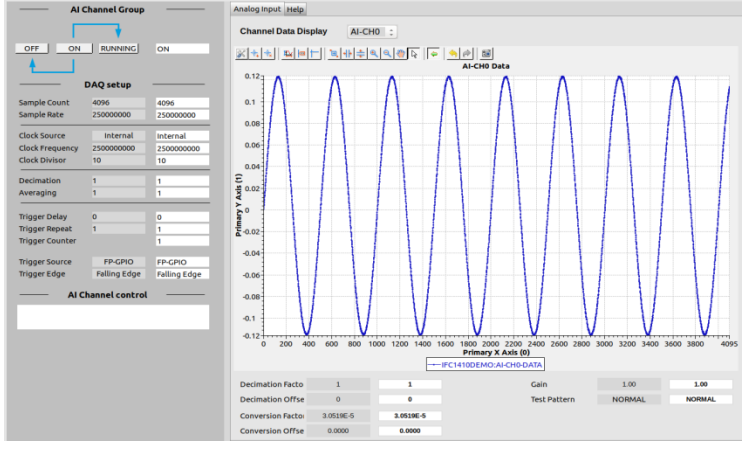
Timing:

Gets synchronization info from external device and provides:

1. clock to MCH
2. triggers to all AMCs
3. machine configuration settings

MCH:

Monitors AMCs, distributes clocks and provides interconnections



CPU:

Manages the EVR and runs the timing related IOC

IFC1410 with ADC3110 FMC:

FPGA collects and elaborates ADCs data;

PPC CPU controls FPGA workflow and runs the IOC.

LLRF system test stand

Timing:

Gets synchronization info from external device and provides:

1. clock to MCH
2. triggers to all AMCs
3. machine configuration settings

MCH:

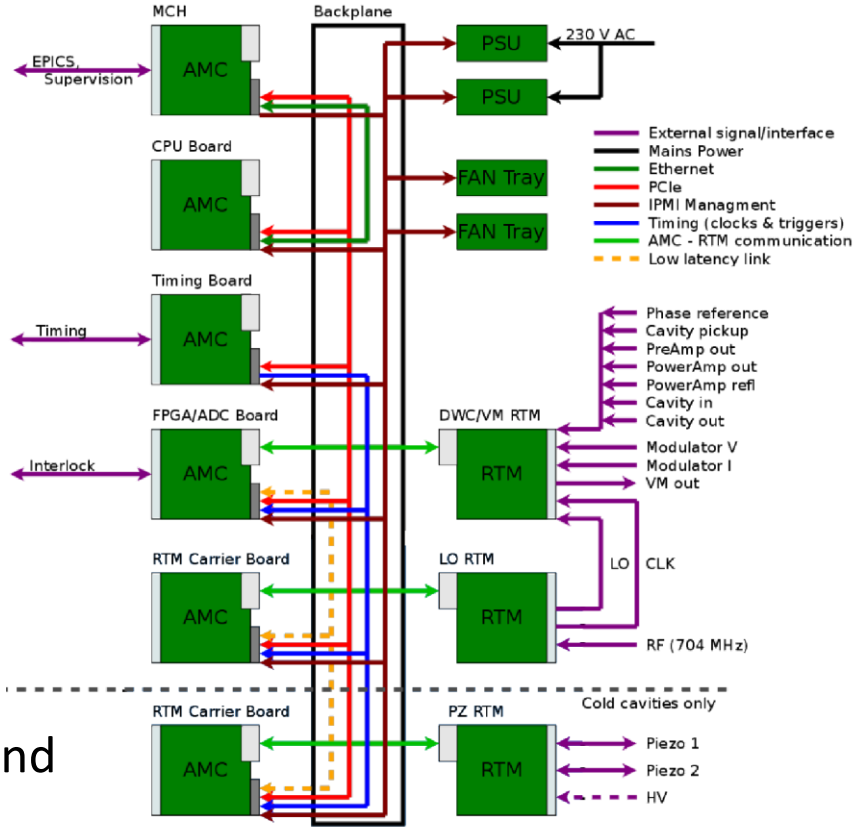
Monitors AMCs status, distributes clocks and provides interconnections

CPU:

Configures and collects data from AMCs, runs EPICS IOCs

AMC & RTM:

Application specific. May provide interlocks and information to MPS



Summary

- ESS uses standard infrastructure components
- Use of COTS AMCs and RTMs when possible
- Development of specialized AMCs and RTMs through In-Kind
- Effort to provide standard acquisition platforms