



| The European Synchrotron

High throughput DAQ for X-RAY DETECTORS

W. Mansour, N. Janvier and P. Fajardo



- **Introduction**
- **DAQ framework Concept**
- **Implementation**
- **Advanced prototype**
- **Experimental results**
- **Conclusions and future work**

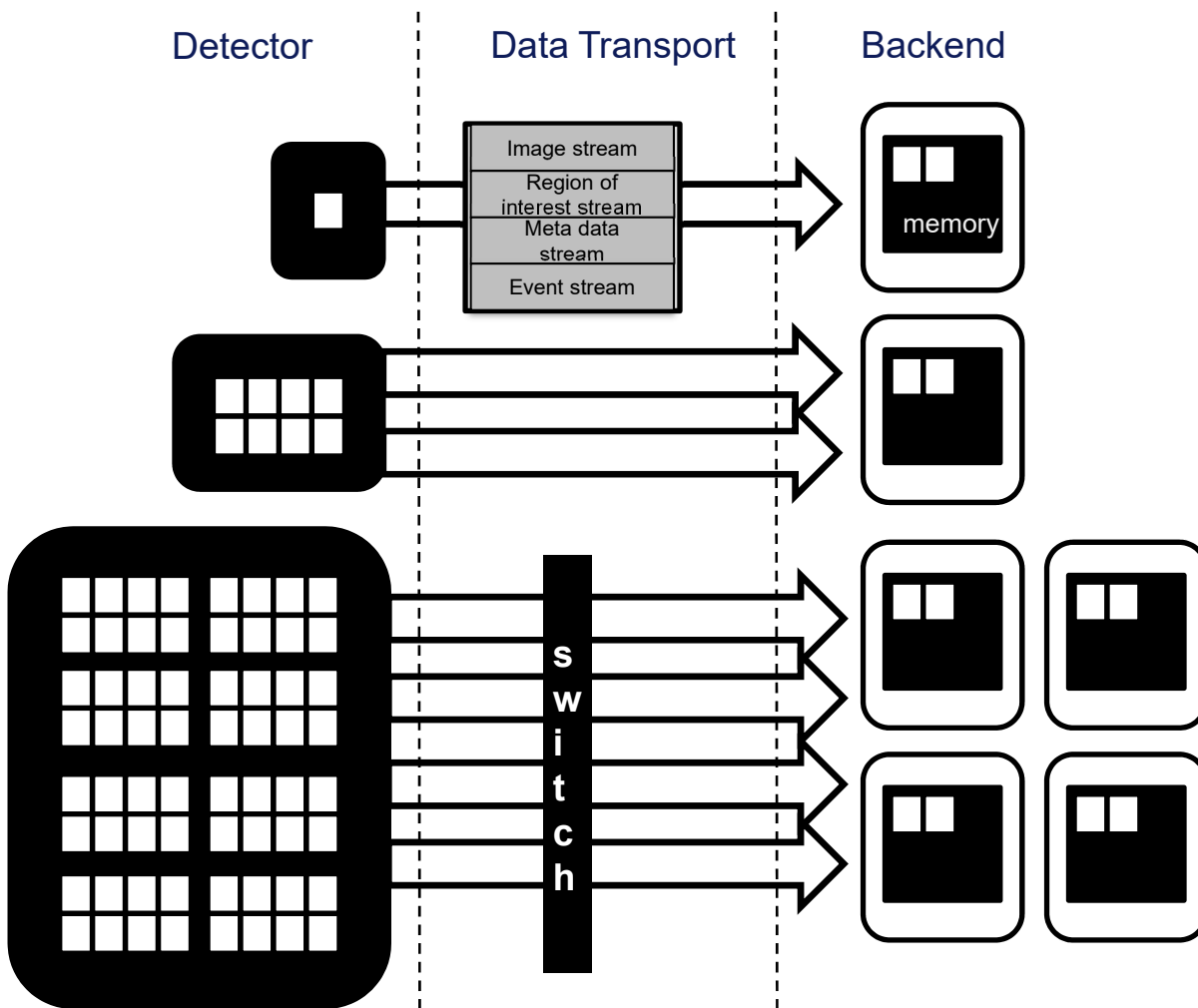
Motivations:

- Current and upcoming advanced detectors produce data throughput in 1-100 GB/s range
- Industrial DAQ protocols do not handle the required data throughput
- The need for a standard tool
- Reusable in a wide range of detectors

Objectives:

- RASHPA: RDMA-based Acquisition System for High Performance Applications
- Initiated in the frame of the European Project: CRISP
- Sufficiently generic and scalable
- Suitable for diversity of new high performance detectors

RASHPA CONCEPT



Scalability

- Support single or multiple sensors and workstations
- Adjustable bandwidth

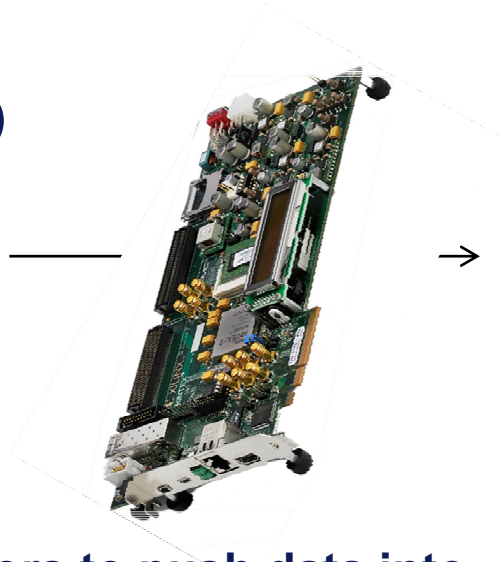
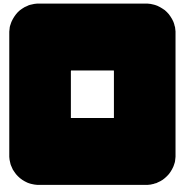
Flexibility

- Adapt to detector geometry (offset, stride, ...)
- Configurable data streams (image, ROI, event)
- Data transport layer (PCIe over Cable, 10 GbE)

High Performance

- RDMA to copy data from source to memory buffer
- Multiple and simultaneous data streams

Detector Module (DM)

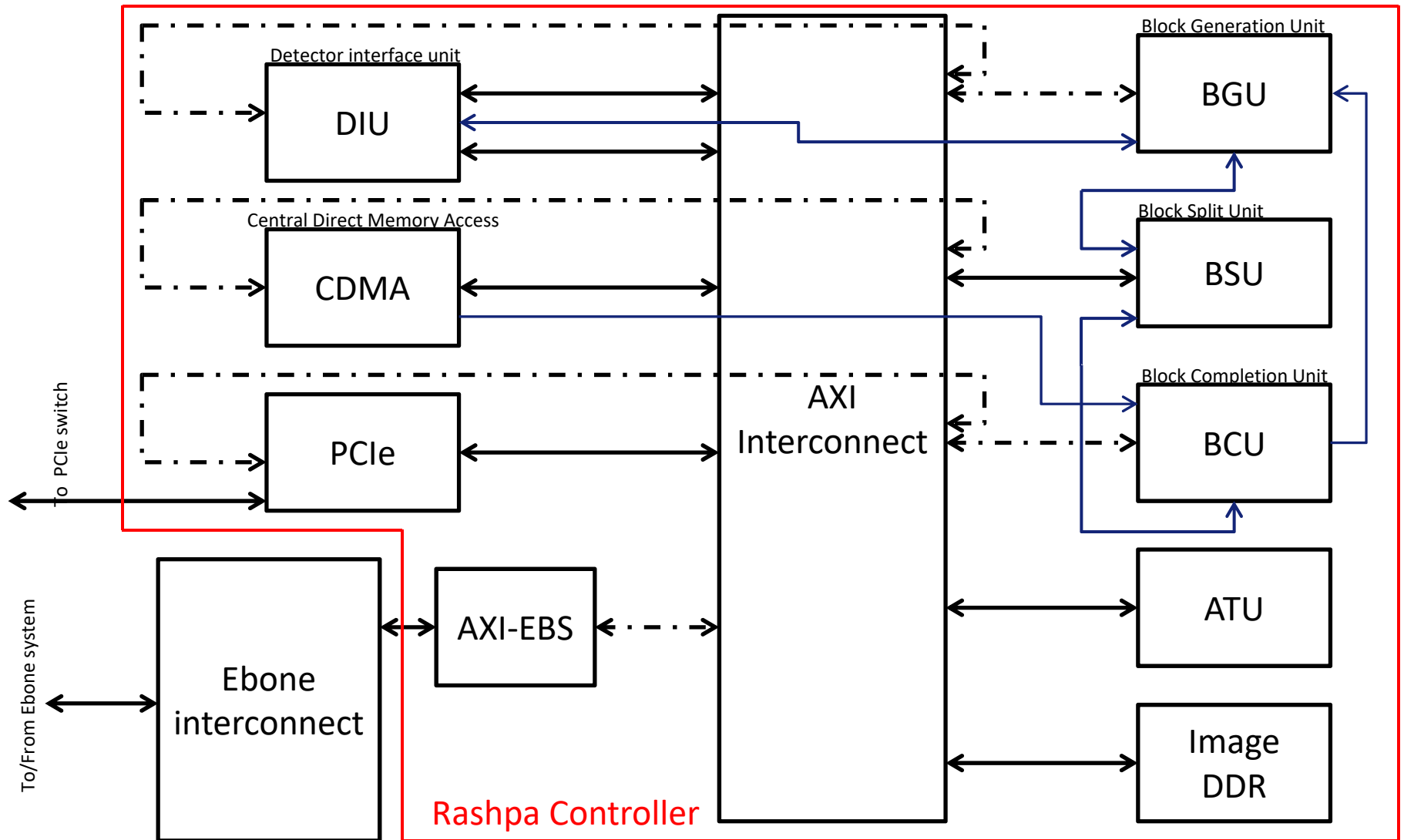


Backend Computer (BC)

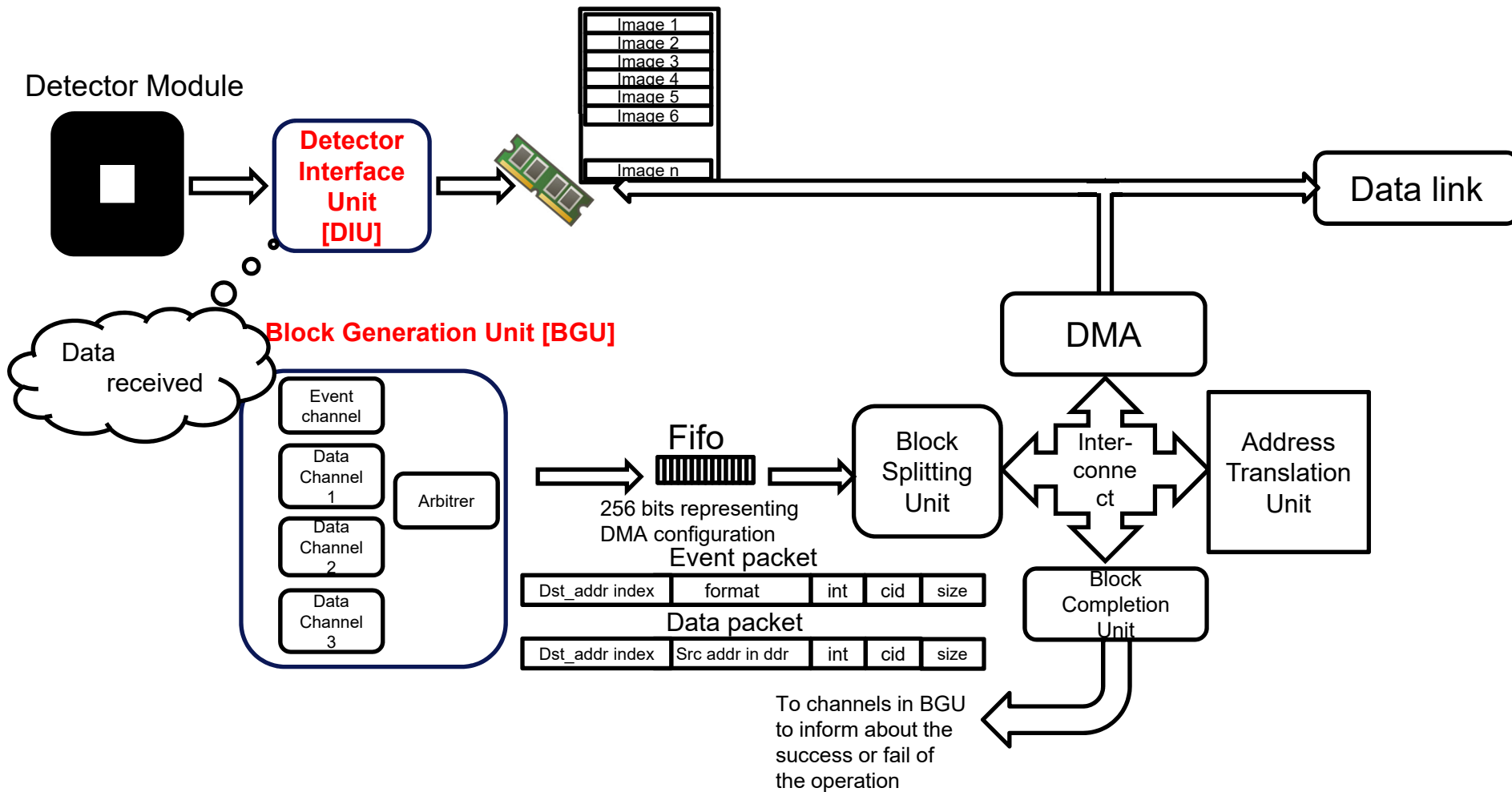


- **RASHPA allows detectors to push data into backend computers**
- **Usual destinations: Memory Buffers**
- **Other destinations: GPU, Coprocessors, disk controllers ...**
- **BCs receiving data from DM are called data receivers (DR)**
- **BC that configures and initializes RASHPA is called System Manager (SM).**

RASHPA IMPLEMENTATION

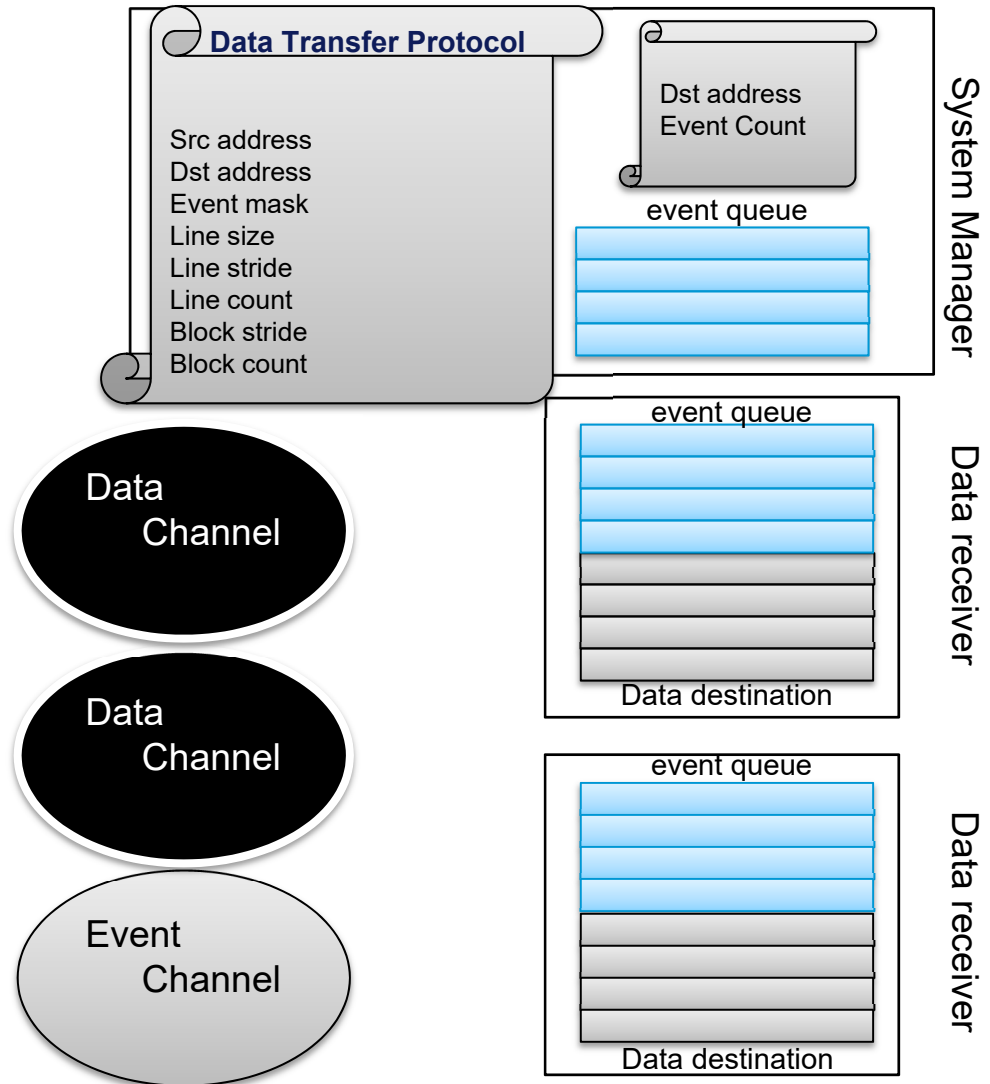
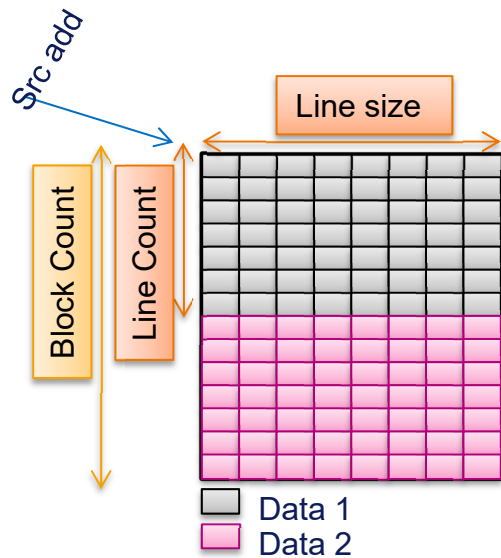


RASHPA IMPLEMENTATION



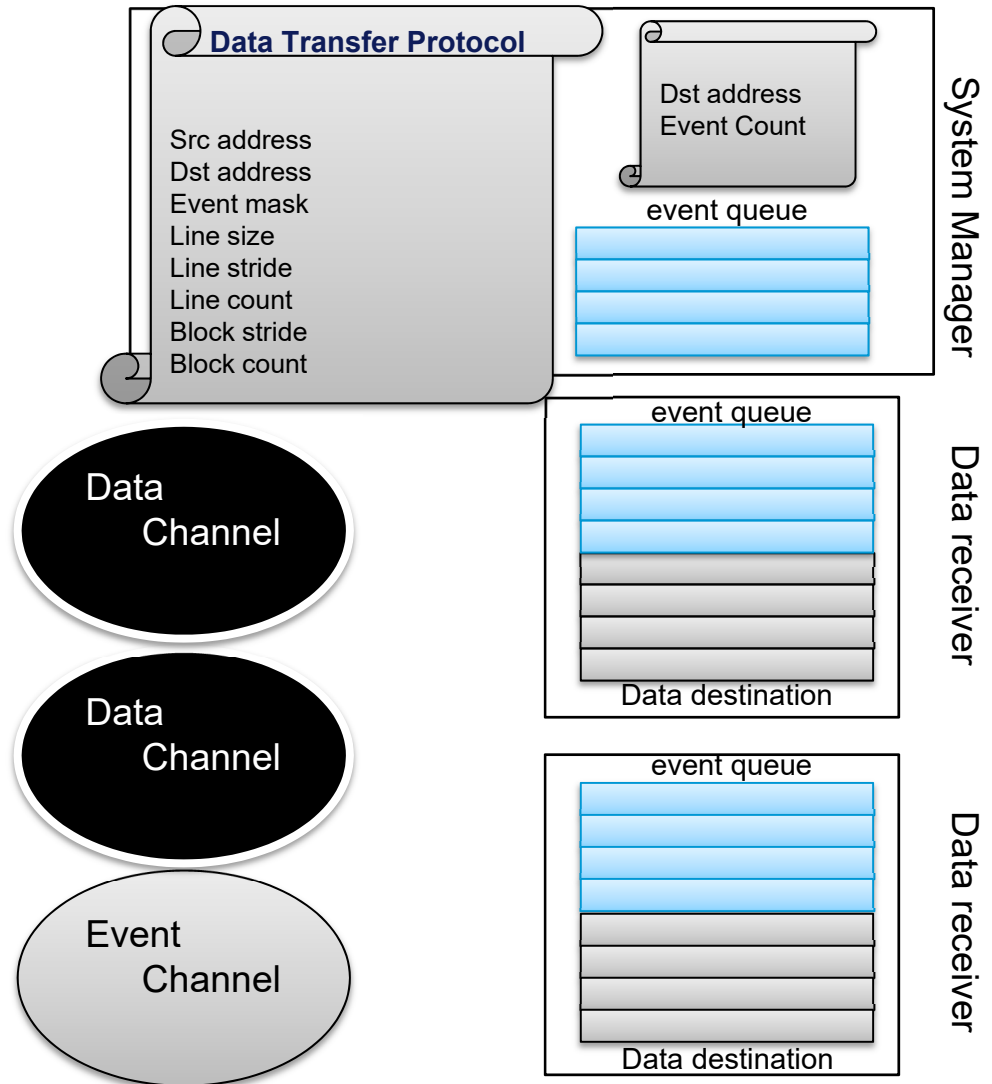
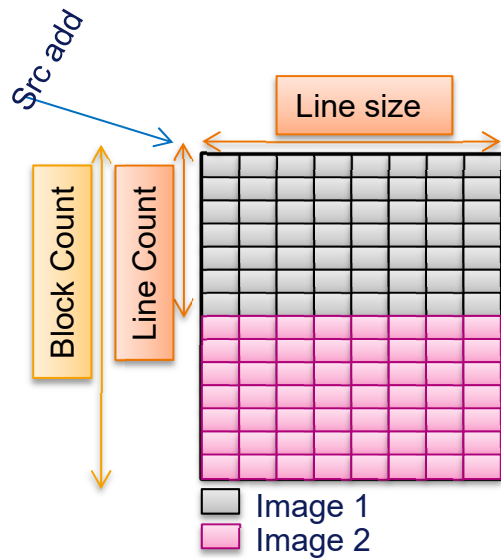
RASHPA IMPLEMENTATION

Data representation in RASHPA DDR



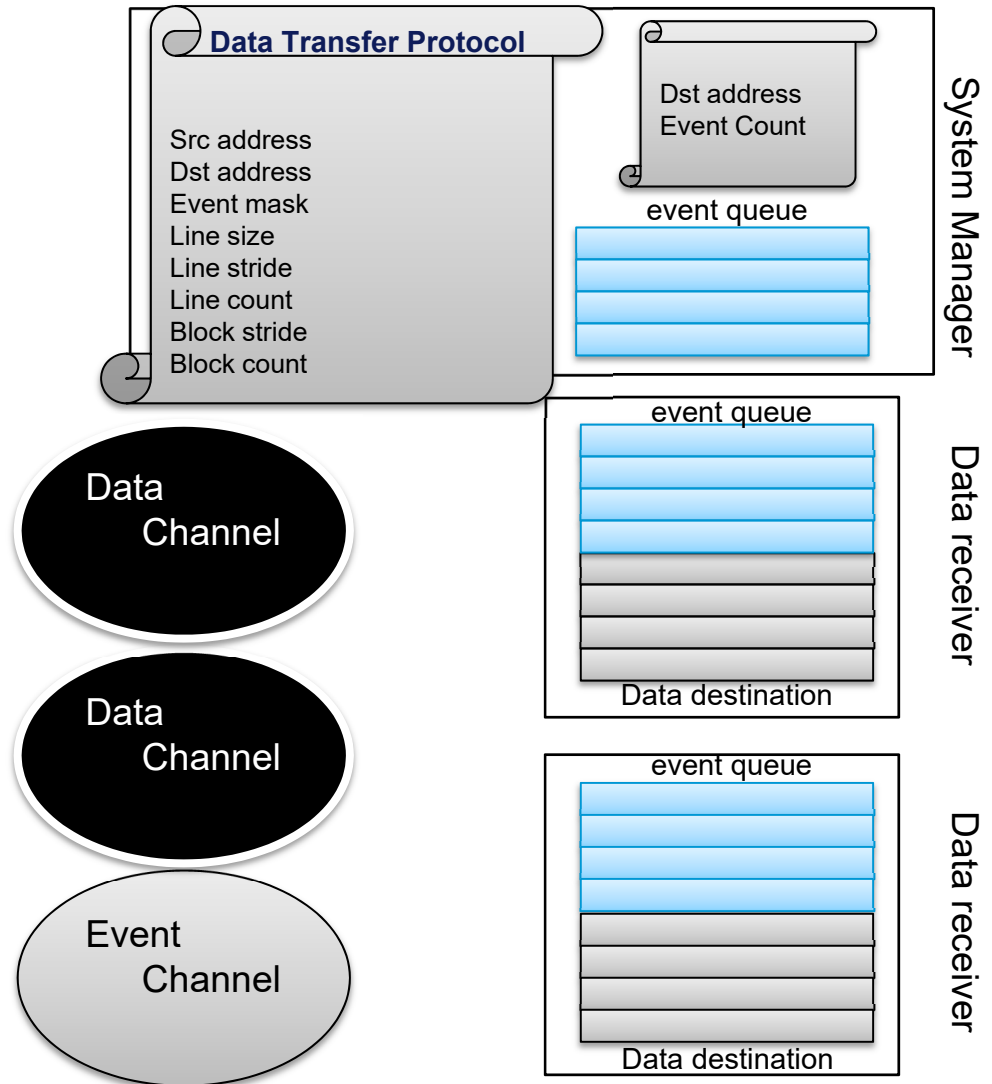
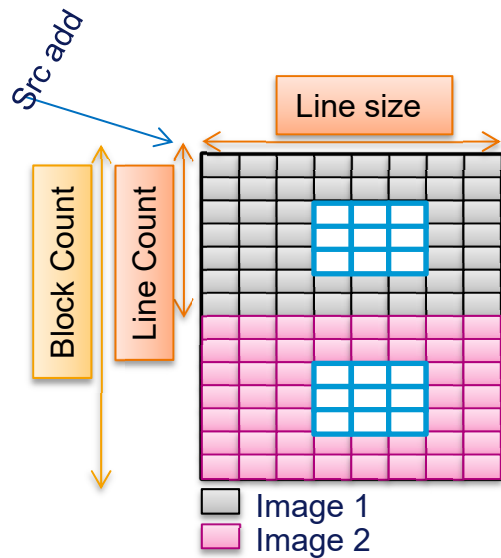
RASHPA IMPLEMENTATION

Data representation in RASHPA DDR



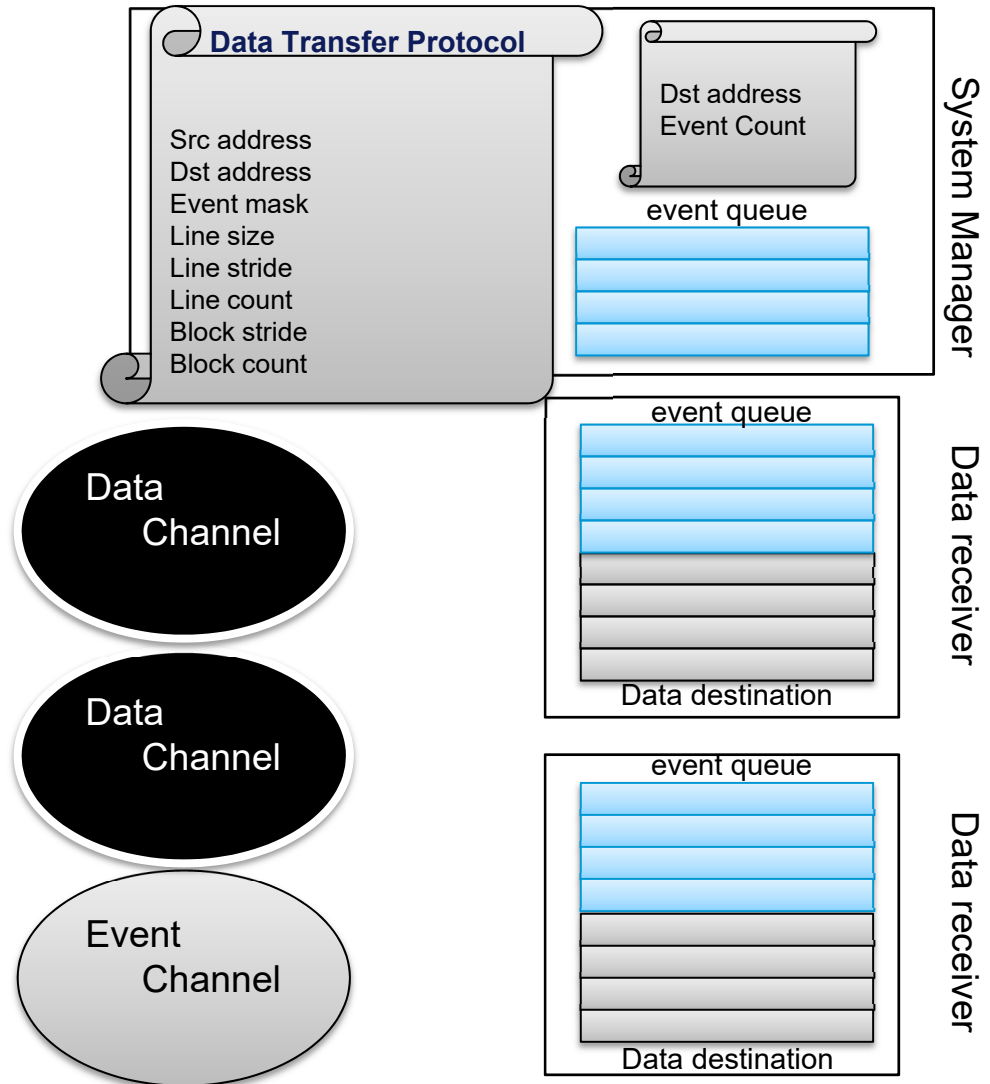
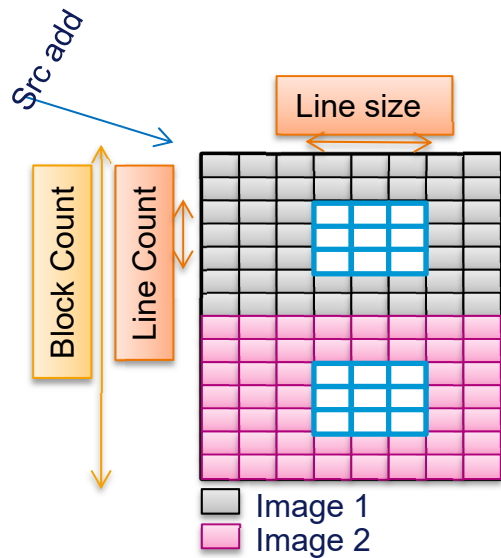
RASHPA IMPLEMENTATION

Data representation in RASHPA DDR



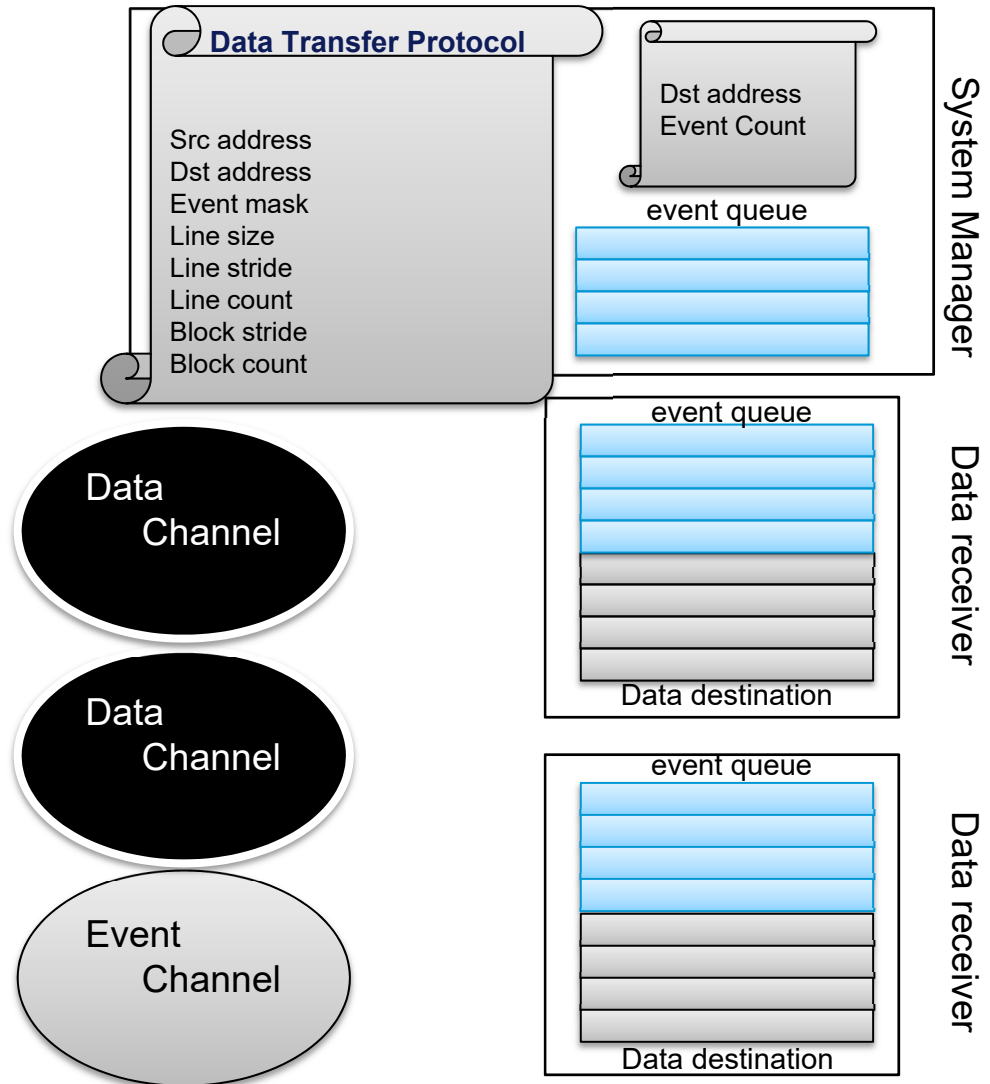
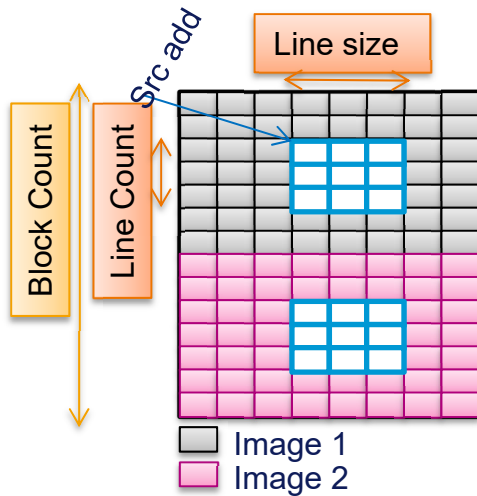
RASHPA IMPLEMENTATION

Data representation in RASHPA DDR



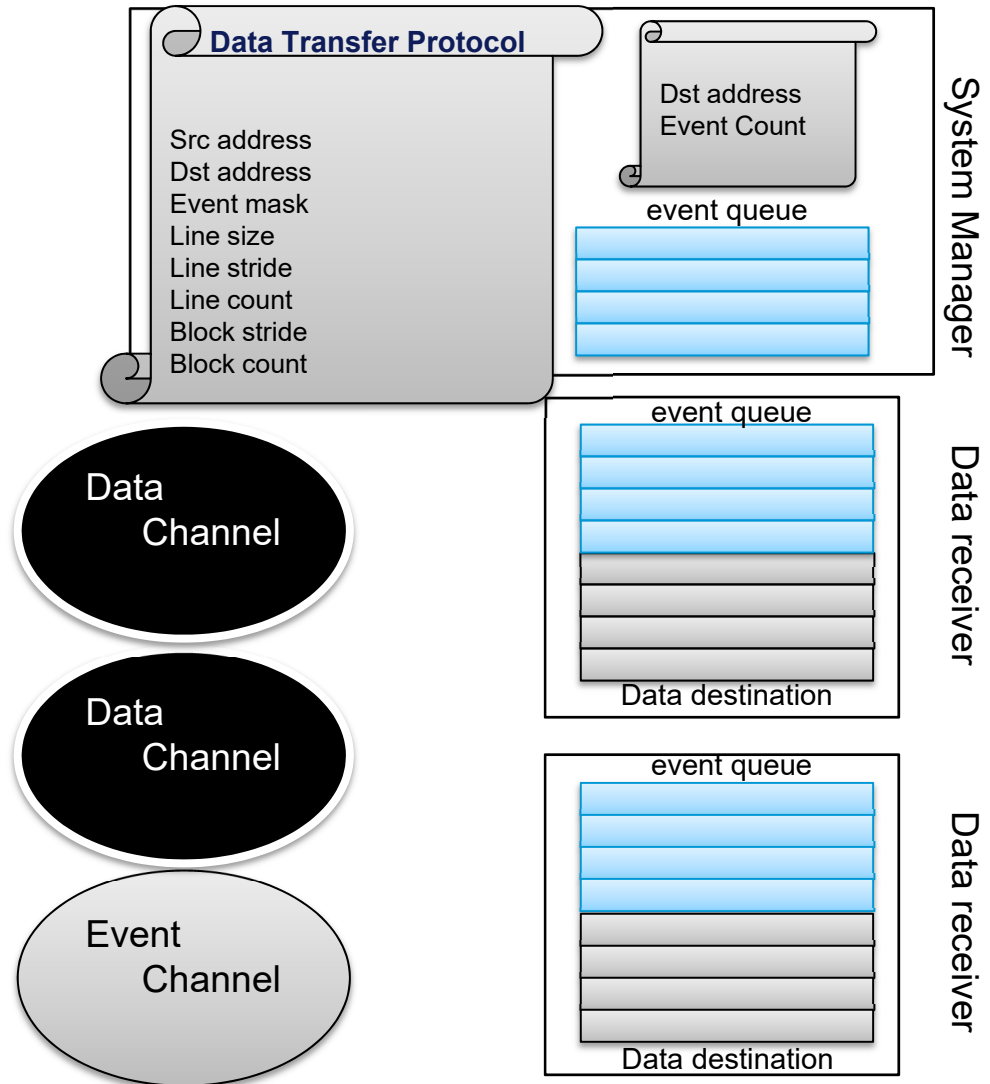
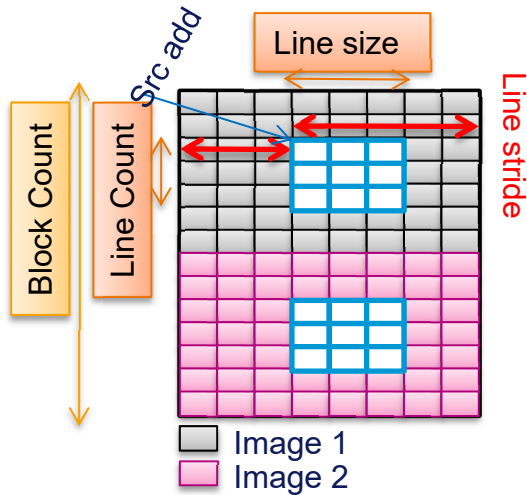
RASHPA IMPLEMENTATION

Data representation in RASHPA DDR



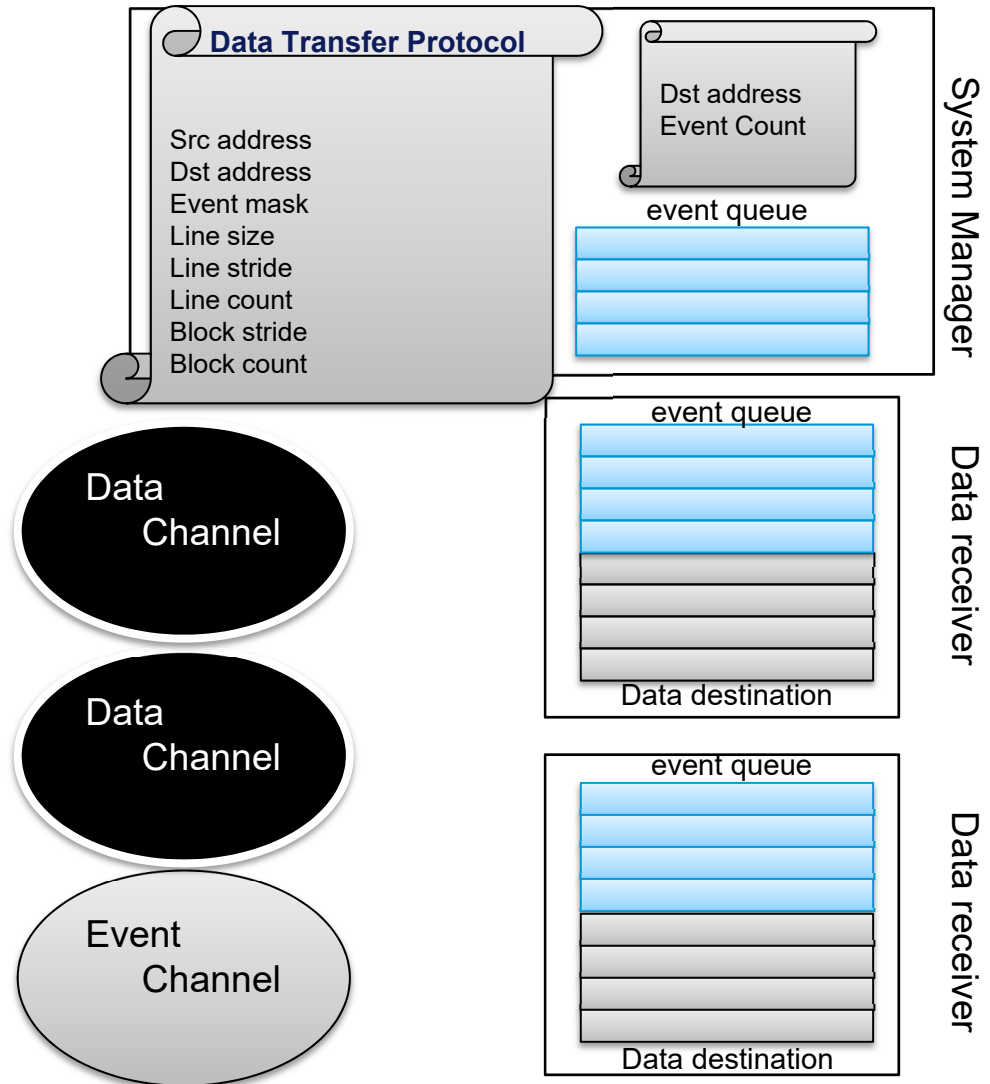
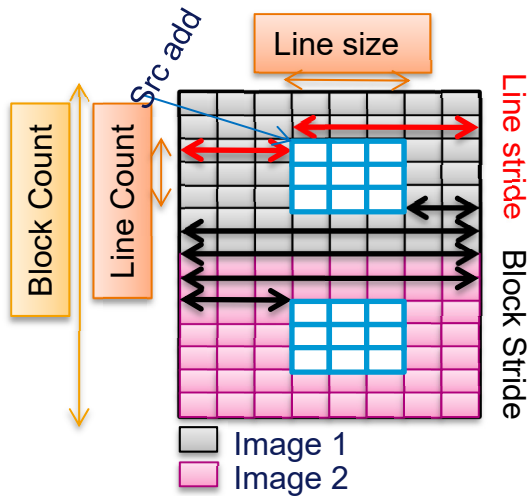
RASHPA IMPLEMENTATION

Data representation in RASHPA DDR

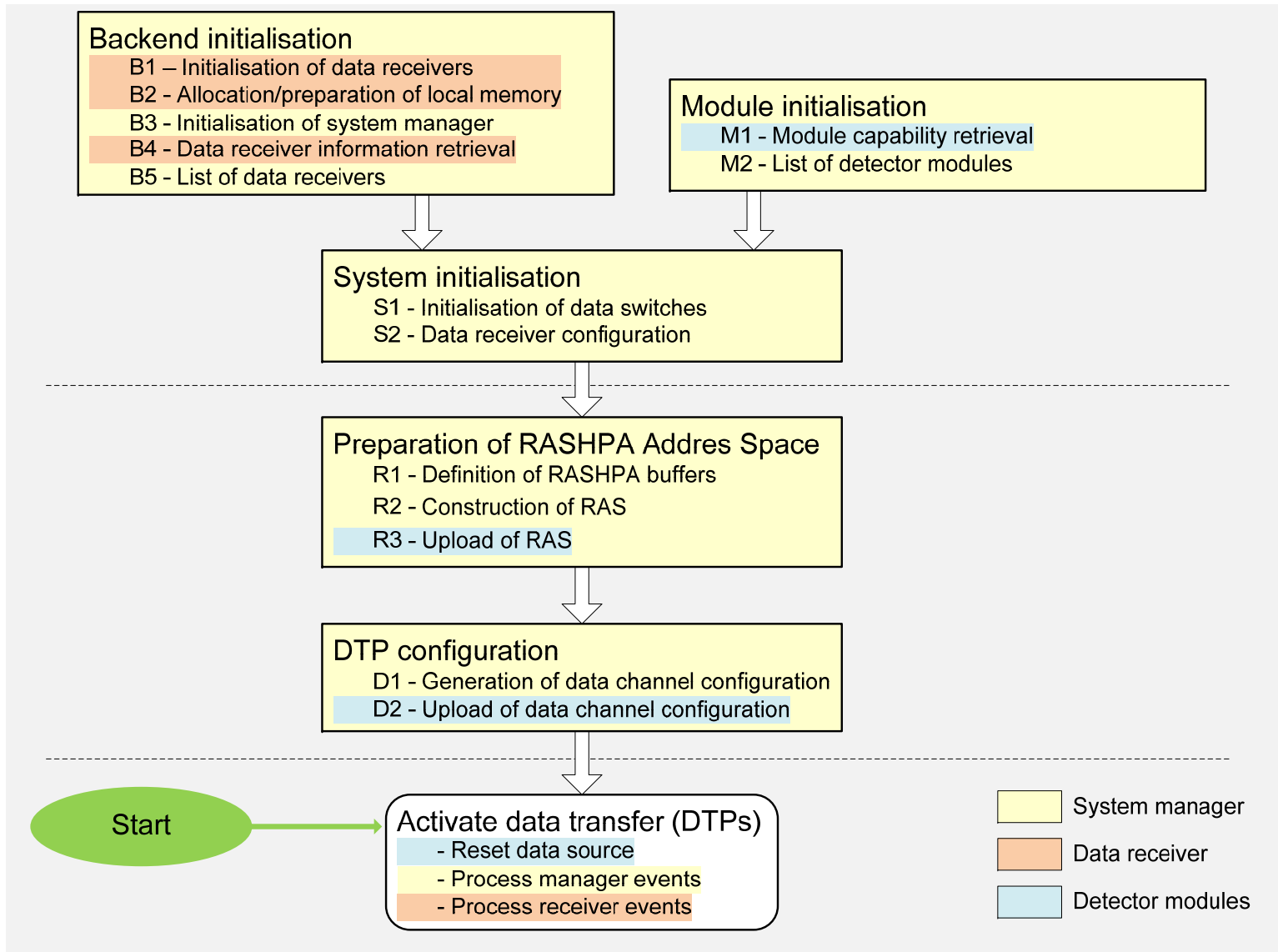


RASHPA IMPLEMENTATION

Data representation in RASHPA DDR



RASHPA IMPLEMENTATION - LIBRASHPA



RASHPA ADVANCED PROTOTYPE

Link Selection

- PCIe over cable was selected for data transfer
 - Native integration
 - RDMA Capable
 - Limited Capabilities
 - Lack of Standardization

One Stop Systems switch



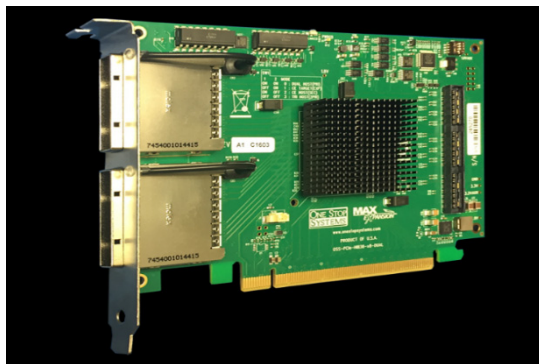
Dolphin IXS600



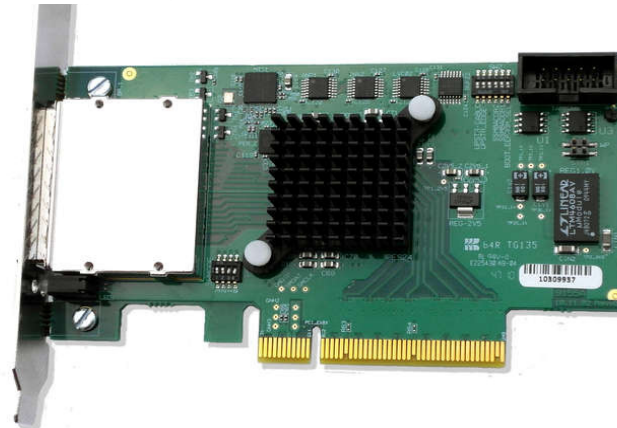
Supported link



One Stop Systems cable adapter



Dolphin PXH810



RASHPA ADVANCED PROTOTYPE

Detector PC as DR and SM



PXH810



RASHPA implemented on PFPKX7 commercial board from techway



Gen2x4

The system manager acts as a data receiver and implement the PCIe switching network.

An industrial PC is used as a second data receiver.

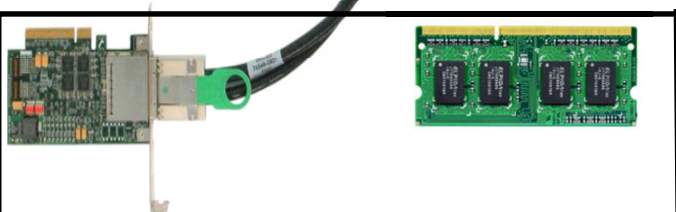
Smartpix detector is used as the XRAY detector for testing but replaced by an emulator to get significant data.

Linux based systems

PCIe IRQ driver

Physical memory driver

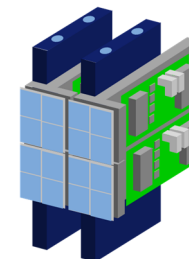
Gen1x1



Industrial PC as DR



PFPKX7



XRAY detector

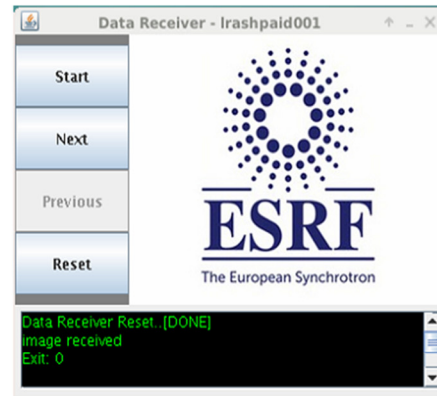
EXPERIMENTAL RESULTS

System Manager

GENERICS	Detector Emulated Data		Image Dimensions		
Event addr	0x79000000	Image Count	1	X-Size	280
Image Addr 1	0x79400000			Y-Size	216
Image Addr 2	0x79C00000				
		CHANNEL 1		CHANNEL 2	
PLX CONFIG		Pixel Size	32	Pixel Size	32
Event ADDR	0xFAC00000	Line Count	216	Line Count	108
Image ADDR	0xFA800000	Line Size	280	Line Size	100
		Start Line	0	Start Line	54
		Pixel Offset	0	Pixel Offset	90
		Block Count	1	Block Count	1

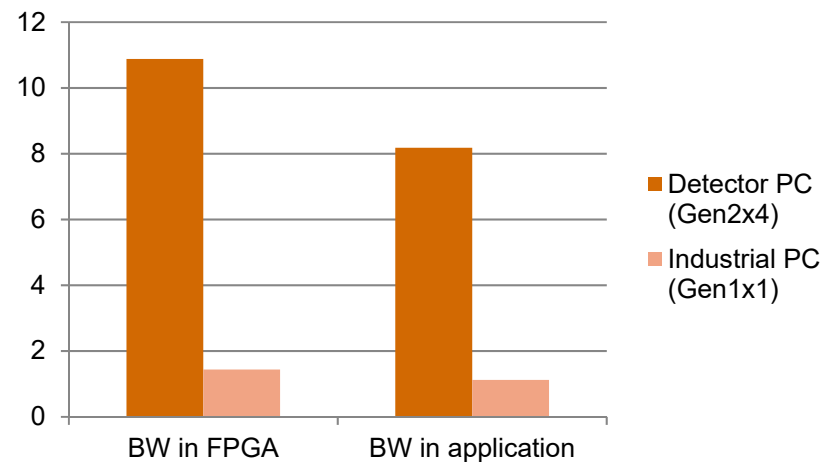
Buttons: reset Rashpa, run Rashpa, config Rashpa

Log: RASHPA reset DONE!!
Configuration Done!!
Running rashpa



Performance Tests

	Bandwidth within the FPGA	Bandwidth when data available to the application
Detector PC	10.88Gbps	8.18Gbps
Gen2x4	68%	51.15%
Industrial PC	1.44Gbps	1.12Gbps
Gen1x1	71.99%	56.28%



Conclusions:

- **Implementation of RASHPA Hardware**
- **Building routable RASHPA network based on PCIe over cable and PLX switches.**
- **Developing and testing the basic functionalities of librashpa for both system manager and data receiver.**
- **Integrating RASHPA with SMARTPIX detector**
- **Building an advanced RASHPA demonstrator.**

Perspectives:

- **Implementing RDMA based protocol over 100G Ethernet network**
- **Application of RDMA techniques in RASHPA to send data directly from the detector to GPUs in data receivers**



THANK YOU FOR YOUR
ATTENTION

Questions??

