LIA-20 Experiment Protection System

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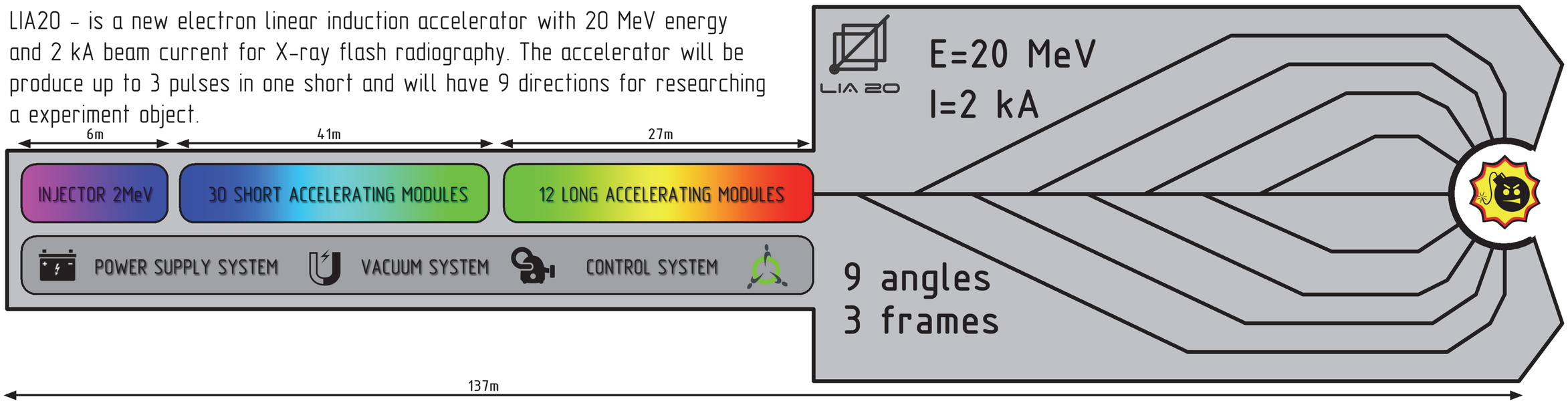
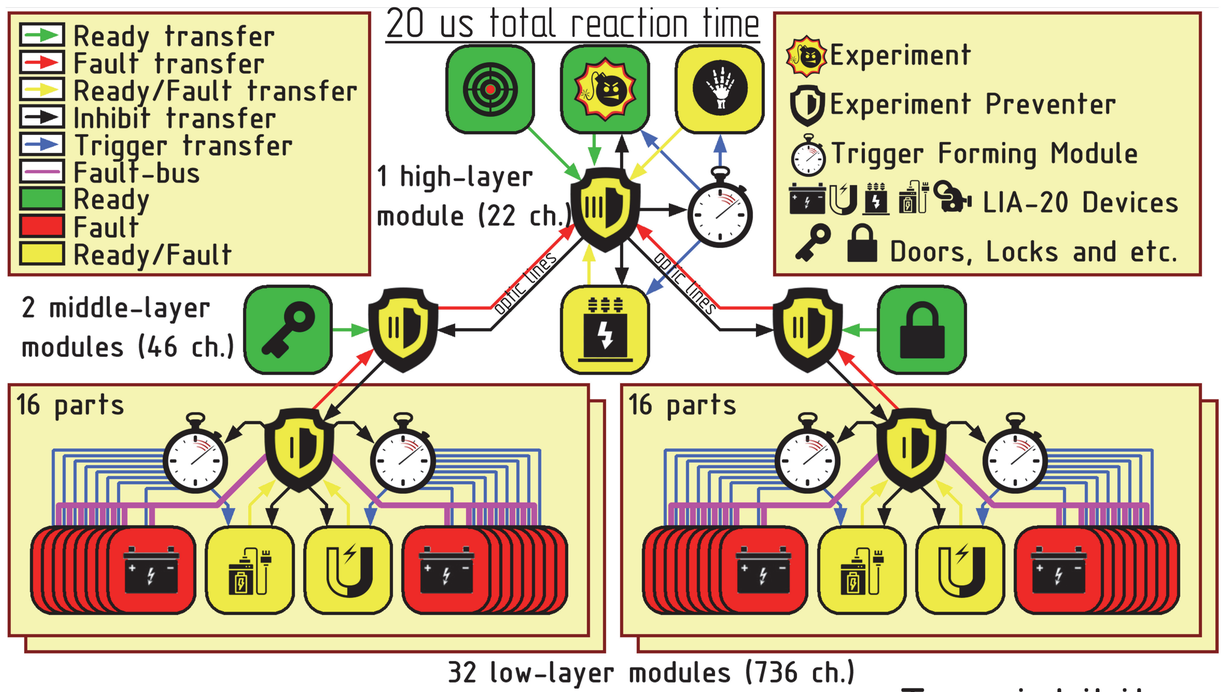
LIA20 – is a new electron linear induction accelerator with 20 MeV energy and 2 kA beam current for X-ray flash radiography. The accelerator will be produce up to 3 pulses in one short and will have 9 directions for researching a experiment object.

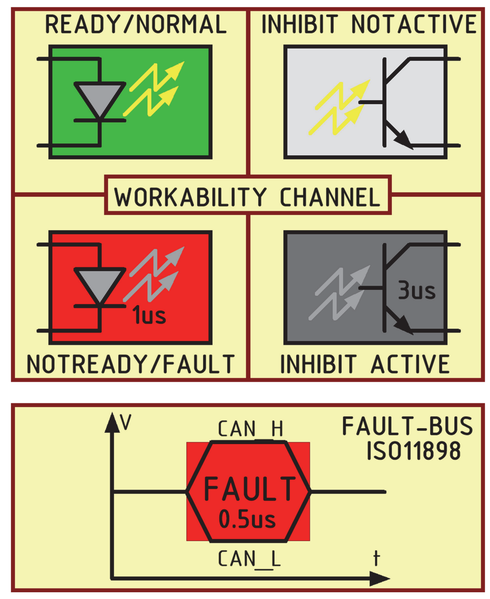


The experiment is very expensive therefore LIA20 needs in a special system that can inhibit the experiment when something wrong in accelerator. This Experiment Protection System based on special designed VME module – preventer. Also special modulator controller enter into this system.



Experiment Preventer

> 6U VME module based on FPGA,
> 8 «workability» channels on a front panel,
> up to 24 «workability» channels with rio module,
> 1 CAN channel,
> 1 «fault-bus» channel for connection modulator controllers,
> Reaction time ~ 3 us.



Two inhibit mechanisms

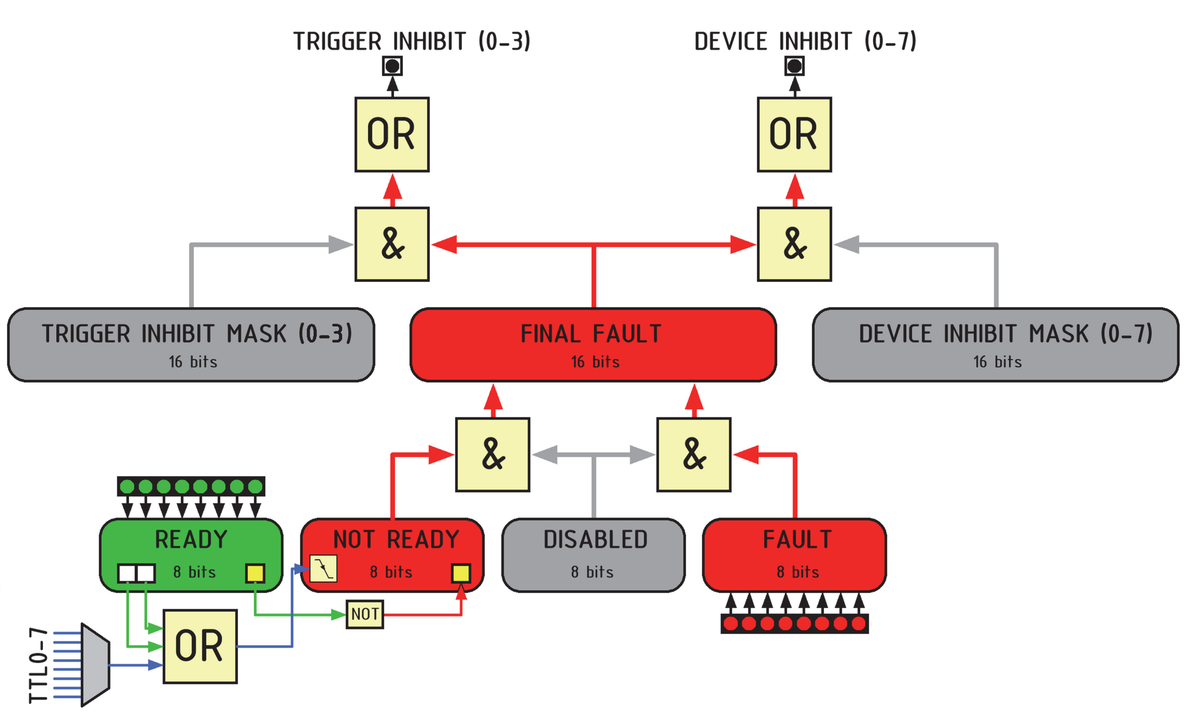
There are two inhibit mechanisms – a trigger inhibit and a device inhibit based on current latched value of a final «FAULT» register which collect values from two different sources:

- from primary «FAULT» signals,
- from processed «READY» signals.

The «READY» signal can be processed synchronously with one of the TTL signal* or with another «READY» signal. Any signal can be ignored by using a «DISABLED» mask. A «INHIBIT» signal appears after multiply the final «FAULT» with a corresponding mask by AND-scheme and summation together all bits in resulting value by OR-scheme.

*There are 8 TTL lines on a VME-BINP crate backplane. This lines are using for start different periods in a main accelerator cycle. LIA20 main cycle use 4 TTL periods. Each TLL period has 4 masks for the trigger inhibit scheme since Trigger Forming Module has 4 inhibit lines DZ0-3.

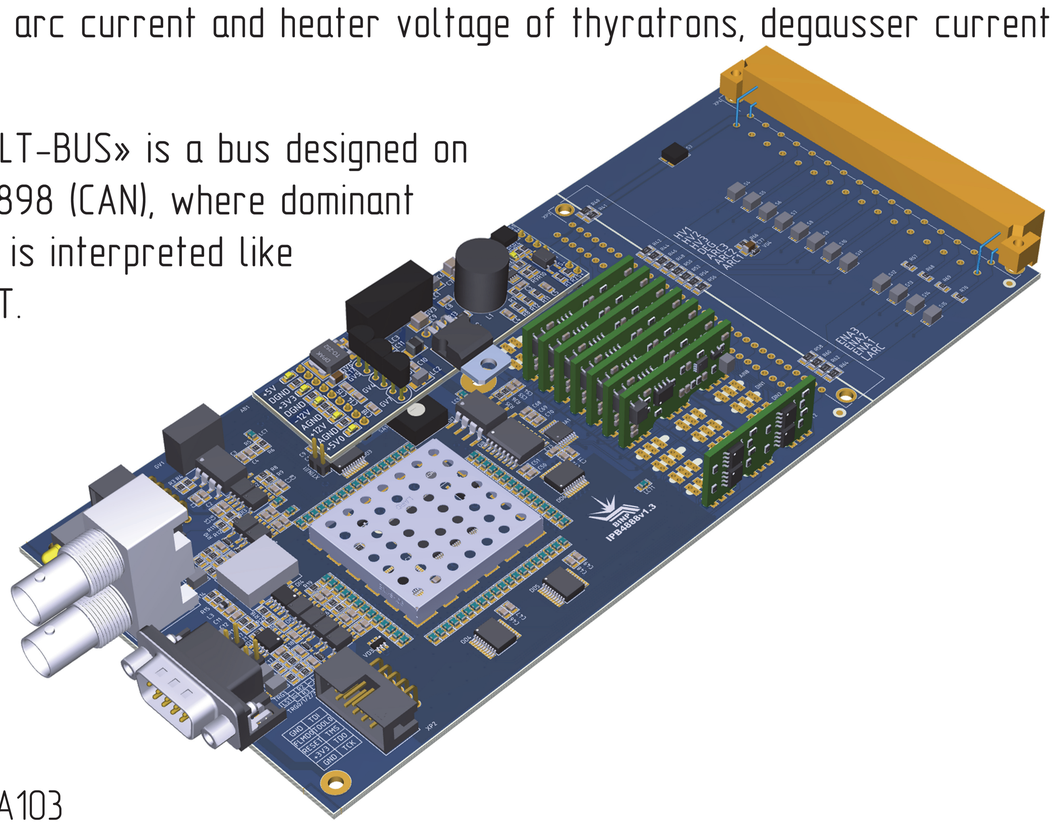
More detais about LIA-20 timing system on a THMPL10 poster.



IPB4888 (Interlock Processing Board)

A Interlock Processing Board is a base of the modulator controller (CoMoD) that one of the important unit in the experiment protection system. This board collect all information about modulator which is elementary unit of the pulsed power supply system. IPB get signals about voltage on forming lines, arc current and heater voltage of thyratrons, degausser current and provide fast reaction on a malfunction over the «fault-bus».

«FAULT-BUS» is a bus designed on ISO11898 (CAN), where dominant level is interpreted like FAULT.



TUPHA103

> 3U Eurocard formfactor,
> Based on Lattice LCMXO2-2000HC & Renesas UPD781035AGA,
> Worked under FreeRTOS,
> 14 replacement submodules:
  - 2 DAC modules (2 channels, 8-bit PWM, not used in CoMoD),
  - 8 Analog modules with comparators (160 kHz bandwidth),
  - 2 Digital input modules (4 isolated channels, can operate like trigger input, not used in CoMoD),
  - 2 Digital output modules (4 isolated channels, can operate like interlock output),
> 4 isolated front triggers,
> 1 front interlock output,
> 12-bit ADC 500 kHz with 128 kB SRAM,
> «FAULT-BUS» (CAN channel disabled),
> I2C, CAN