TiCkS: A Flexible White-Rabbit Based Time-Stamping Board

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ABSTRACT

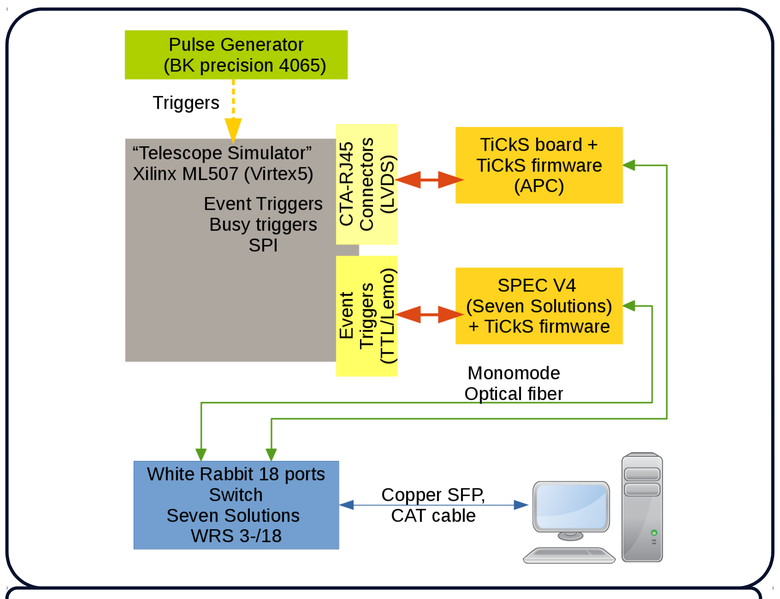
The TiCkS board (Time and Clock Stamping) is based on the White Rabbit (WR) SPEC node (Simple PCIe FMC carrier), to provide ns-precision time-stamps (TSs) of input signals and transmission of these TSs to a central collection point, developed as one of the candidate CTA TS nodes, with a small form-factor for use in any CTA camera.
The main firmware changes in the Spartan-6 FPGA are: the addition of: 1) a ns-precision TDC for the TSs; and 2) a UDP stack to send TSs and auxiliary information over the WR fibre, and to receive configuration & slow control commands over the same fibre. It also provides a PPS (Pulse Per Second) and other clock signals to the connected device, from which it can receive auxiliary event-type information over an SPI link (Serial Peripheral Interface).
A version of TiCkS will be made available in the WR Open Hardware repository, providing a cheap, flexible, and reliable solution for ns-precision time-stamping of trigger signals up to 400 kHz, for use in other experiments.

CTA, Cherenkov Telescope Array

CTA [1] will be a gamma-ray observatory in the very-high-energy range (VHE, > 30 GeV), with >120 imaging atmospheric Cherenkov telescopes distributed over two sites (La Palma, Spain & Atacama desert, Chile).
CTA's Software Array Trigger (SWAT) will detect coincident Cherenkov light-flashes (<100 ns window) from showers of particles induced in the atmosphere by Gamma-rays & Cosmic rays.
The SWAT needs accurate relative Time-Stamps (TSs) from each telescope's Camera Trigger Management electronics (CTM), which it can correct in software for the telescope pointing
→ Coincidence identification with a flexible logic

White Rabbit Technology for CTA

White Rabbit (WR) [2], adopted for time-stamping since it can achieve CTA's 2 ns rms relative accuracy requirement
WR for CTA:
- Distribute time from a central clock system to WR "nodes" in each telescope camera,
- Sent over hierarchical network of WR-compatible switches at array control centre
- WR-nodes time-stamp trigger signals from CTMs
  - both for "read-out" events and "busy" triggers
- Event & PPS counters in both camera's CTM and its WR-node for combining event data with TSs
- WR network itself may be used to collect TSs from all telescopes at a central point for SWAT
- Coincidence information sent to each camera's data-processing pipeline
  - → allows to drop non-coincident event data



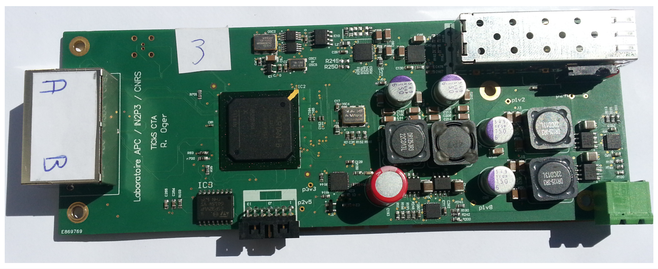
Test bench for TiCkS

TiCkS, CTA Time-Stamp node candidate

Hardware

TiCkS board (Time and Clock Stamping), based on WR-SPEC node [3] & WR-core [4]

Operation based on:
- "fine-TDC", 1ns:
  - Based on 8-bit I/O-SerDes @ 1 GHz (from PLL on WR-125 MHz clock)
  - As shift register for input trigger signal
  - Trigger signal in register detected on WR-clock tick,
    - → flag + #ns stored
- "Coarse-TDC", 8 ns:
  - Counter of the WR-clock, Zeroed by WR-PPS
  - Read-out if trigger signal detected
- PPS and Event counters
- SPI link (50 MHz) from OpenCores [5]
  - Allows some bits (16) from CTM → TiCkS
- FIFO from WR-core
  - To store/send event information
  - But "fix" of 2 FIFOs in ping-pong (by MUX), to avoid read-out dead-time
- UDP Stack from OpenCores [6]



TiCkS board with 2xRJ45 CTA-Connector

Test Bench for TiCkS

"Telescope Simulator" based on Xilinx ML507
- → mirrored simultaneous outputs to:
  - TiCkS (LVDS/RJ45)
  - SPEC-DIO with TiCkS firmware (TTL/Lemo)

Two modes:
- Fixed frequency, from Pulse generator
- Random Poisson generator
  - internal 100MHz linear-feedback shift register, 20 out of 32 bits
  - → minimum time & interval 210ns

Maximum Event Rate Tests

Fixed-Frequency

Histograms of ~10^8 inter-trigger time-stamps
- → no loss up to 320kHz,
- slight loss at 400kHZ, then worse

Random Triggers

Inter-trigger time-stamps well fitted by $Ne^{-\lambda T}$
Few missed events:
- i.e., counter increment with no TS
- No loss @ ≤ 9.5kHz, ~10 events/million @ 19 kHz
  - → equivalent dead-time below 1 ns

Data & Software

- Event data sent in "*bunches*"
  - ≤20 events (with bunch time-out)
- Close-packed into 12-byte words (LSB parts)
- "*Tailer*", 20 bytes (full LSB+MSB information)
- Bunch size ≤ 260 byte (≤ 302 bytes with overhead)
  - → Close to optimal for UDP network packets
  - Average event size of 13 bytes
    - 75% gain over unpacked events, given 42-byte overhead
- Decoding/unpacking library in "c"

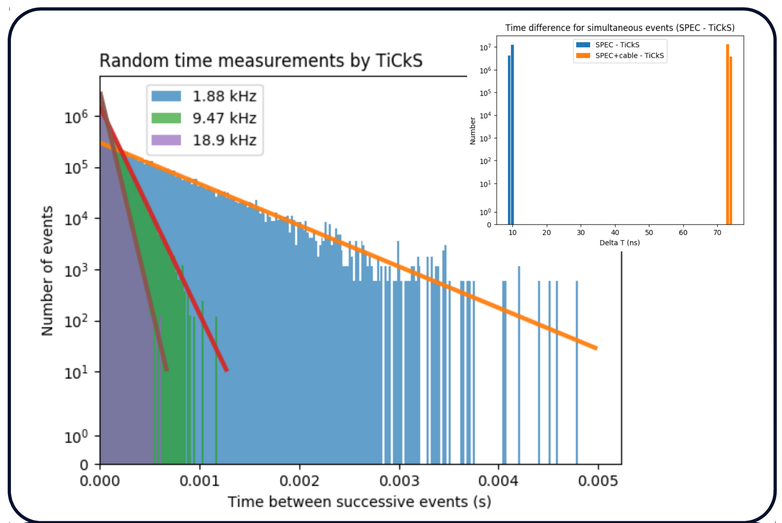
Firmware main characteristics:
- Spartan 6 xc6slx45t-3fgg484 version ISE 14.7
- Using 6735 slice registers (12%)
- 1/8 high-speed I/O buffers (BUFPLL)
- 4/4 Phase Locked Loops (PLL_ADVs)

Direction	Signal Name	Comment
Camera → TiCkS		
	Read-out Trigger	Required
	Busy Trigger	Optional (for cameras with dead.time)
	SPI clock, data, chip-select	Optional
TiCkS → Camera		
	PPS	Synchronized via WR
	x MHz clock	Aligned with PPS, x = 10 MHz here
	External Trigger	At defined TAI time

Signals exchanged between Camera Trigger Management (CTM) and TiCkS

Inter-board Time-Stamps

Tested to 400kHz (fixed freq.), 56kHz (random)
Distribution always within 2 adjacent ns bins
Addition of cable delay (63.2ns) → shift as expected



Inter-board trigger distributions for random Poisson inputs (*inset*: TiCkS intra-board distributions, with/without cable delay)

References

[1] CTA, **www.cta-observatory.org**
[2] White Rabbit Open Hardware, **www.ohwr.org/projects/white-rabbit**
[3] SPEC WR Open Hardware project, **www.ohwr.org/projects/spec**
[4] WR Core v4.0, **www.ohwr.org/projects/wr-cores/Wiki/Wrpc_release-v40**
[5] SPI Master/Slave Interface, **www.opencores.org/project,spi_master_slave**
[6] 1G eth UDP / IP Stack, **https://www.opencores.org/project,udp_ip_stack**

Conclusions

TiCkS hardware and firmware built and tested:
- well-capable of time-stamping trigger signals
  - Tested for fixed & random time distribution
  - Little or no loss at CTA rates
- Soon to be made available in OpenHardware

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