THE TIMING SYSTEM OF HIRFL-CSR*

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This article gives a brief description of the timing system for Heavy Ion Research Facility in Lanzhou- Cooler Storage Ring (HIRFL-CSR). It introduces in detail mainly of the timing system architecture, hardware and software. We use standard event system architecture. The system is mainly composed of the events generator (EVG), the events receiver (EVR) and the events fan-out module. The system is the standard three-layer structure. OPI layer realizes generated and monitoring for the events. The intermediate layer is the events transmission and fan out. Device control layer performs the interpretation of the events. We adopt our R&D EVG to generate the events of virtual accelerator. At the same time, we have used our own design events fan-out module and realize distributed on the events. In equipment control layer, we use EVR design based on FPGA to interpret the events of different equipment and achieve an orderly work. The timing system realizes the ion beam injection, acceleration and extraction.

INTRODUCTION

The CSR is a synchrotron system, and the injection, acceleration, accumulation and derivation of the cluster must be precisely synchronized to achieve a successful operation cycle. CSRm infuses the CSRe with a beam once every other cycle, and CSRe can use the storage (or deceleration) of the beam to continuously target the target experiment. This precise synchronization is performed by the timing system and the magnetic field power control system. The time of the cluster in the CSR main ring is approximately 0.5us ~ 3us.

Fig. 1 shows the structure of the CSR synchronization control system. The synchronous control system connects all parts with Ethernet as the transmission medium: synchronous server, database, front-end server, front-end controller. The database system and synchronous server is the information and control centre of the whole system. The main function of the synchronization server is to organize the synchronization data of the CSR tuning bundles to all related devices, including the distribution of synchronous data and the generation and broadcast of timing. The synchronous database is one of the subsystems, which mainly stores the synchronous data of the equipment that is well organized. I/O controller and the DSP implementation parts perform specific operations role, they can finish and synchronous communication between the server and a controller is responsible for one to four control device object. The front-end server completes the collection of the output information of the controlled device object and the data exchange with the database system, and also provides the man-machine interface. Synchronous fan out is mainly used to distribute a synchronous instance in the timing sequence.

HIRFL - CSR current way is composed of a piece of the story card (FPGA card PXI bus) based on virtual accelerator software is responsible for time series output to meet the requirements of optical signal pulse sequence, is converted to electrical signals through the light to electric switch, via the twisted-pair distributed to each control station control system. In each station control system is converted to light pulse signal through electrical signal to optical signal converter, and then fan out through light and the optical fiber distributed the light pulse signal to the control system of workstation front controller (DSP). In the front-end controller, it is interpreted and compared with the pre-deposited cases to determine whether the waveform output is carried out. The structure is shown in the Fig .2.

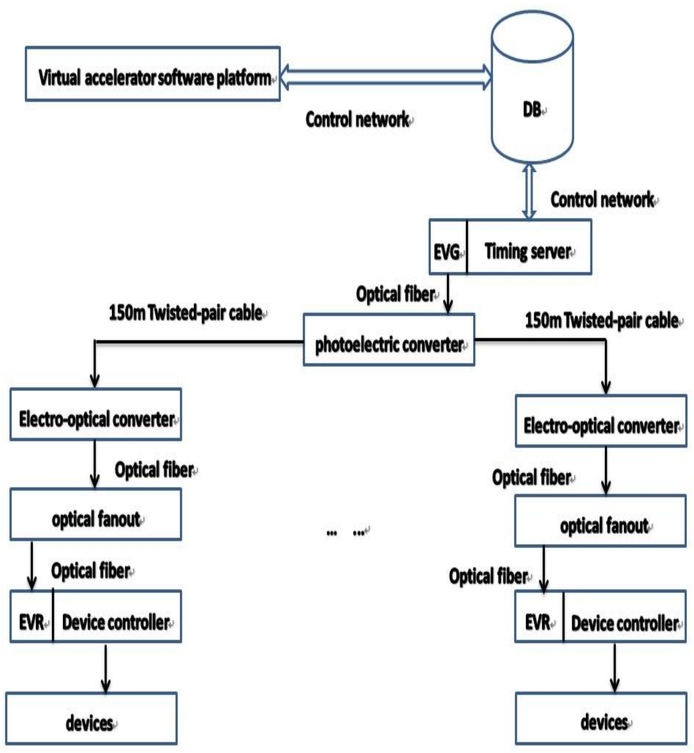

Fig2: The structure of the hardware

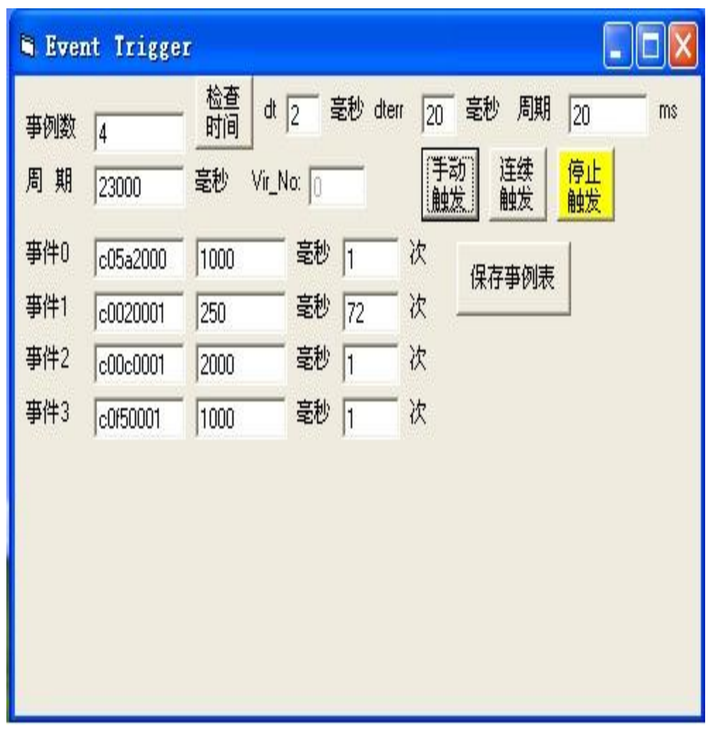

Fig5: the event cycle sequence organizing GUI

For physical events the GUI (Graphical User Interface) is used to write the event sequence cycle to the RAM on the EVG, read the event sequence cycle from RAM and start the event cycle. Moreover, the GUI can exchange data with the Oracle database. Fig. 5 shows the event cycle sequence organizing GUI. The event cycle story structure is shown in Fig. 6.

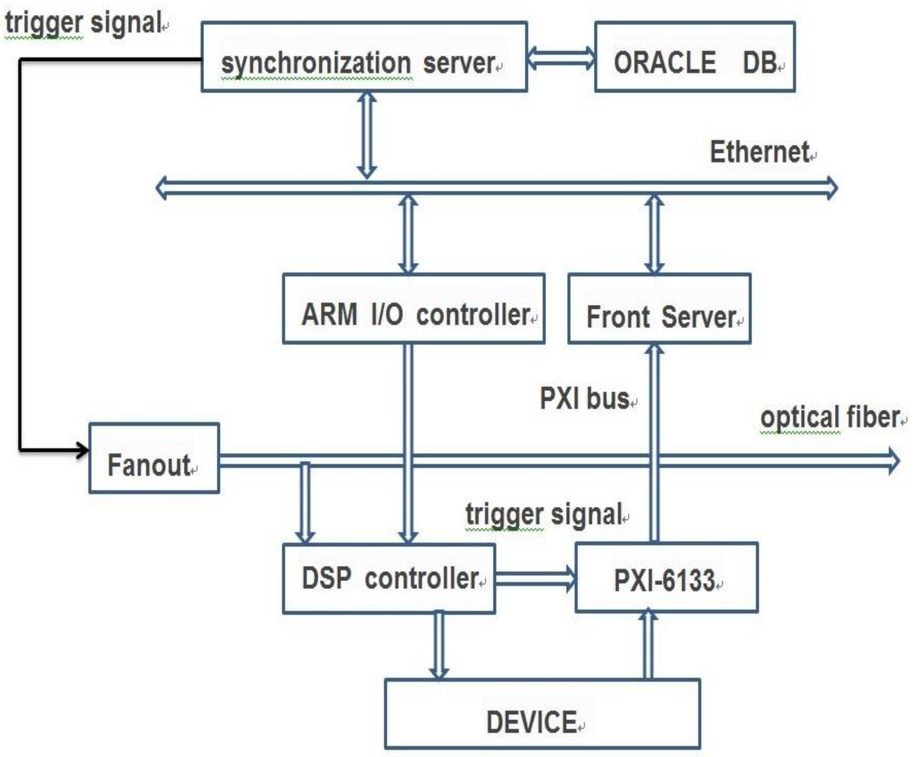

Fig1: The structure of the CSR synchronization control system

The event table type description: Event code is a binary array and the length is 32 bits. The data file structure of the event table is shown in Fig. 3. The event story structure is shown in Fig. 4.

the number of event ID in the table
event ID1
Event ID delay time (unit is 20 ns)
event ID2
Event ID2 Delay time value
.....
Event IDn
Event IDn Delay time value
Trigger the output pulse width (unit is 40 ns)

Fig 3: The structure of the event table.

bits	31	30	29--25	24	23--16	15--8	7--0
value	1	1					
instruction	head of the code		reserve	mode	Event no.	Function code	virtual accelerator no.

Fig 4: The event story structure .

the number of events
length of the string
event ID
delay time
repeat times

Fig 6: The event cycle story structure .

The timing system has been applied to the actual operation in 2008 and passed the acceptance of the CSR expert group. It implements the requirements of the synchronization for the CSR project. The timing system has been stable operation of the nine-and-a-half years, and ensures the normal conduct of the experiment.