MicroTCA based Beam Position Monitoring System at Cryring@ESR

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Motivation

At FAIR the commissioning of the re-assembled CRYRING accelerator, formerly hosted by Manne Siegbahn Laboratory Stockholm, is currently in progress. This compact low energy heavy ion synchrotron and experimental storage ring will be the main instrument for an extensive research programme as well as a testing platform for the future beam instrumentation and control system concepts decided on for FAIR. Besides many other measurement systems CRYRING is equipped with 18 beam position monitors (BPM), for which a new data acquisition system (DAQ) was developed. Based on the upcoming MicroTCA form factor in combination with FPGA mezzanine card (FMC) technology the DAQ system was designed to be state-of-the-art, reliable, modular and of high performance. Testing „Open Hardware“, here the ADC FMCs and FMC carrier boards, was another intention of that concept.

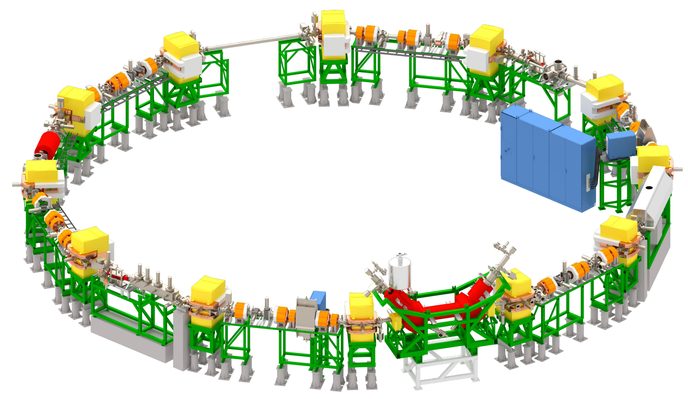


Figure: Cryring **E**xperimental **S**torage **R**ing visualisation

DAQ and Signal Processing System

- MicroTCA.4 based system
  - 1 frontent controler CPU.
  - 2 MCHs
  - 5 AFCv2 FMC carriers
  - 9 ADC 250M 16b 4ch FMC
  - 36 Channels
- AMC FMC Carrier (AFC)
  - Artix7 200t FPGA.
  - 2GB/32bit DDR3 memmry.
  - 2 FMC HPC slots.
- Matpex PCI express breakout board
- Exploder, a White Rabbit receiver node

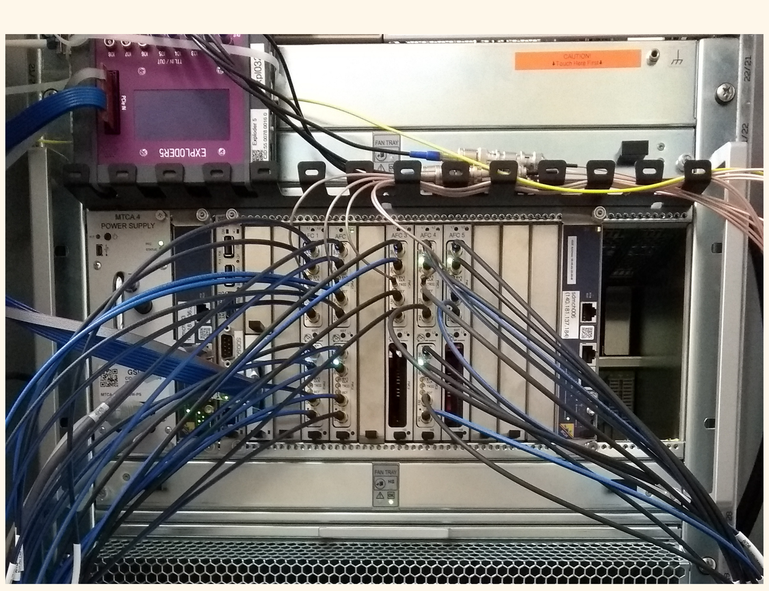


Figure: Cryring BPM DAQ system in MicroTCA form factor

AFCv2 MMC (Cortex M3) and MATPEX1a (AVR XMEGA) uses common IPMI implementation developed at GSI. It was tested with N.A.T. and Vadatech MCH.

In HDL DAQ Infrastructure

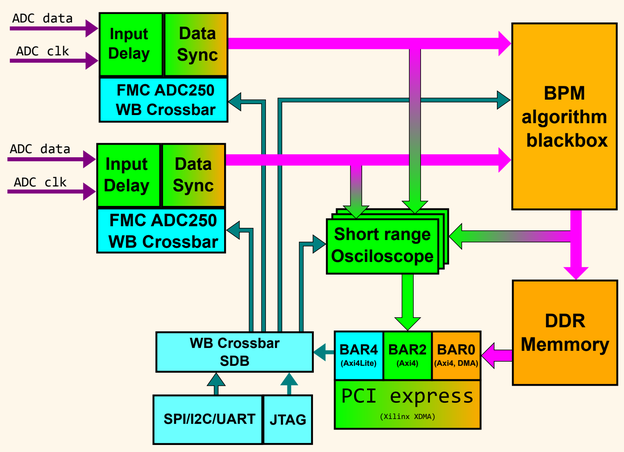


Figure: HDL bitstream

- Mainly writen in VHDL
- Control network based on Wishbone + Self Describing Bus extension
- AXI4Lite to Wishbone and Wishbone to AXI4Lite translation
- Algorithm is a black box with well defined input and output interface (Axi4-Stream)

Graphical User Interface

The following figures show the ADC raw data, the calculated positions and the closed orbit for a stored 300 keV/u H_2^+ beam with a beam current in the order of 10 μA.

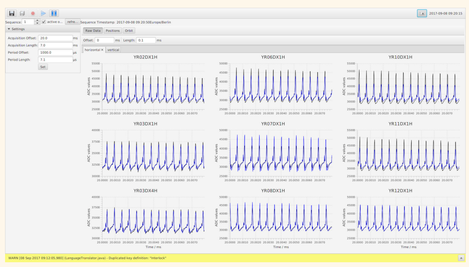


Figure: RAW data for 9 horizontal BPMs

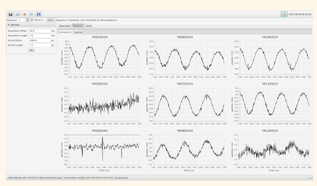


Figure: Beam positions for 9 horizontal BPMs

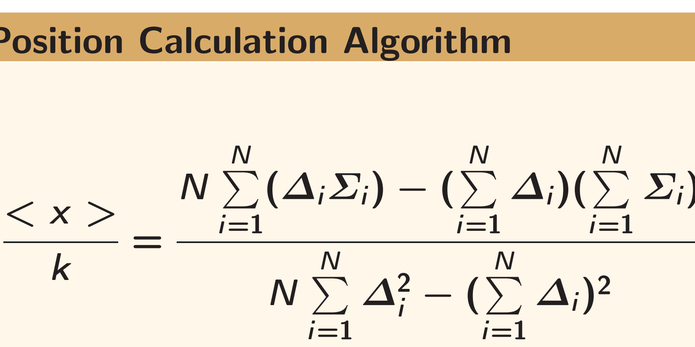
Figure: Orbits

Position Calculation Algorithm

$$\frac{< x >}{k} = \frac{N\sum_{i=1}^{N}(\Delta_i \Sigma_i) - (\sum_{i=1}^{N}\Delta_i)(\sum_{i=1}^{N}\Sigma_i)}{N\sum_{i=1}^{N}\Delta_i^2 - (\sum_{i=1}^{N}\Delta_i)^2}$$

Figure: A Least-Square Fit of Difference signal to Sum signal is used to estimate the position of the beam.

In FPGA implementation of the algorithm is realised in multi stage pipelined architecture. In a first part of it dividend and divisor are created while in a second stage estimator is created using the High Radix division algorithm. The algorithm was implemented and tested in FPGA. The result values were matching to the ones computed in PC.



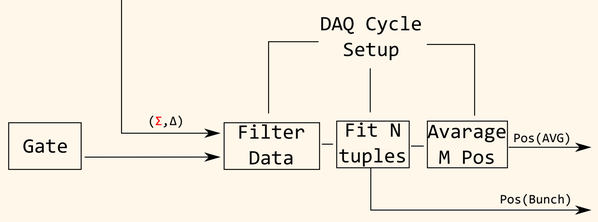


Figure: simplified BPM signal flow during the digital processing in the FPGA

Future Steps

- More stabilisation and bugs hunting
- Complete characterization of the system
  - amplifier and ADC gains
  - noise sources
  - data paths delays
- Implementation of RF synchronisation for turn-by-turn measurements (tune)
- Further integration into the control system (FESA)
- Integration with WhiteRabbit FAIR timing receiver node

Modular FMC VHDL Abstraction Layer

- Written in VHDL
- No external scripts required
- Carrier/Board compatibility checks
- Automate pin assigments
- Helps with verification
- Easy FMC instantiation

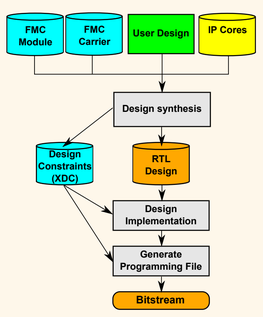


Figure: FMC HAL flow

Boards supported:

- OHWR FMC ADC 250Msps 16b
- OHWR FMC DIO 5ch ttla
- OHWR FMC DIO 32ch ttla

Contact Information

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