Parallel processing for the high frame rate upgrade of the LHC synchrotron radiation telescope

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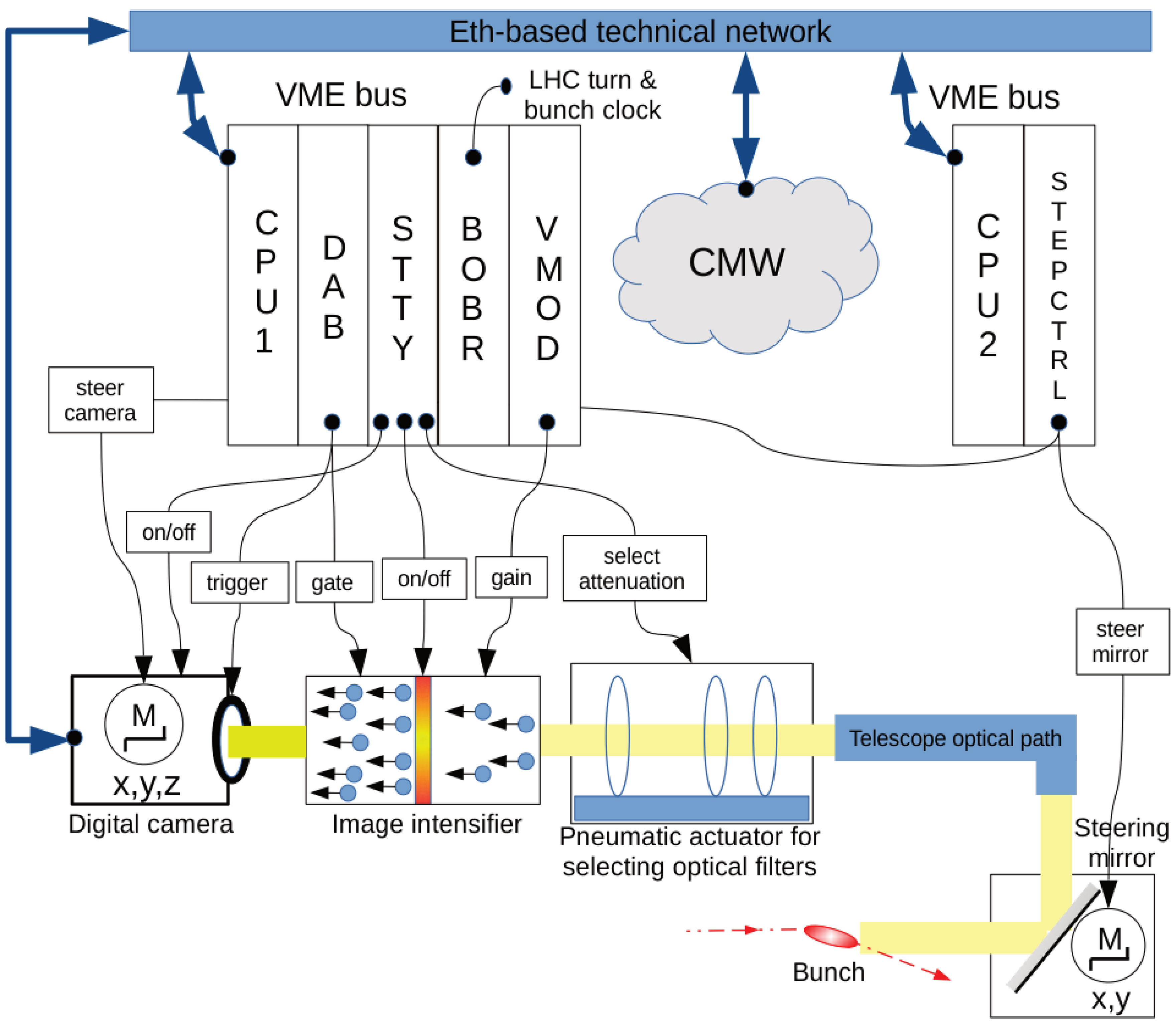
Abstract

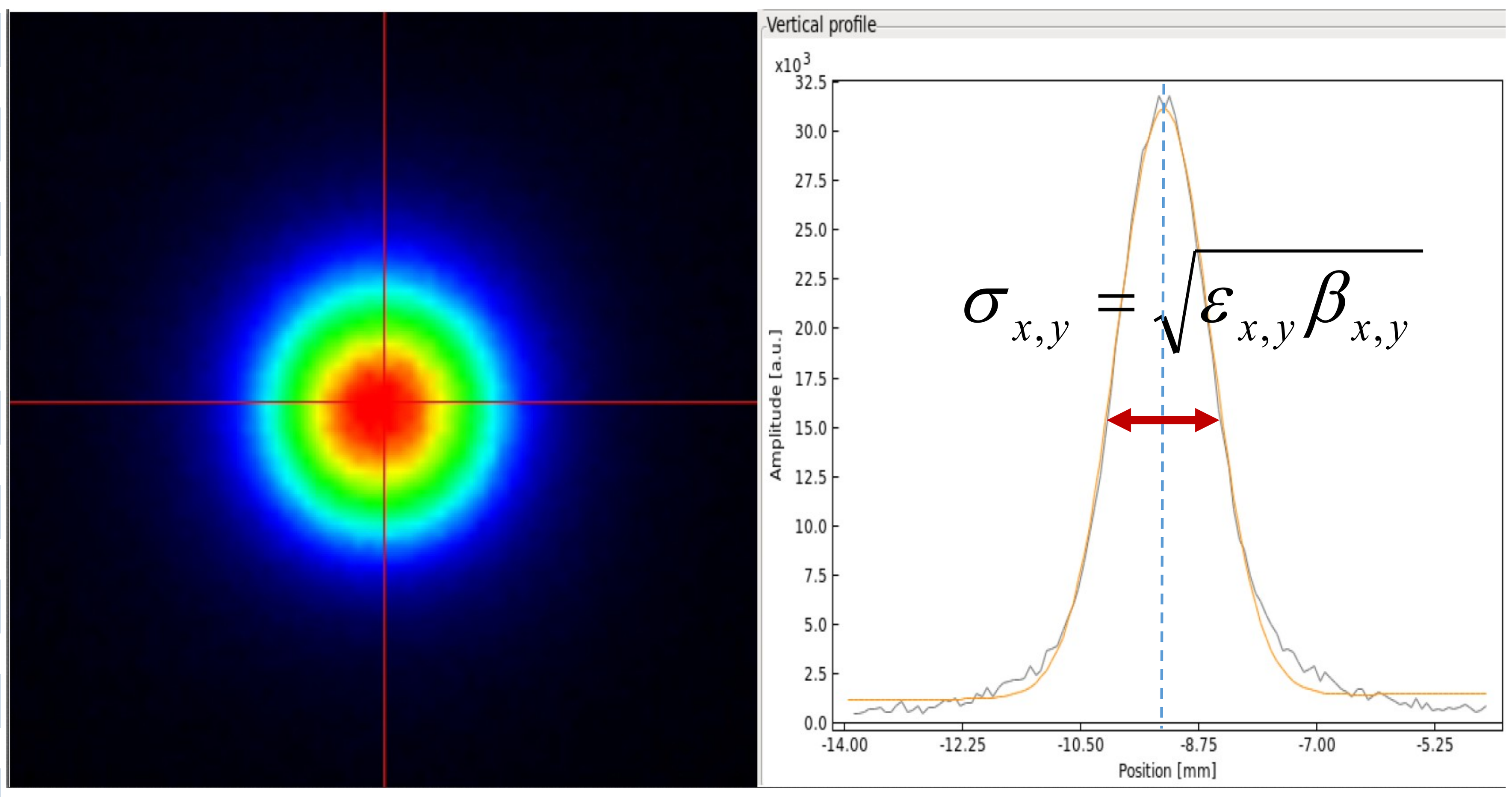
The Beam Synchrotron Radiation Telescope (BSRT) is routinely used for estimating the LHC's beam size, profile and emittance; quantities playing a crucial role in the optimization of the luminosity levels required by the experiments. During the LHC's 2017 run, the intensified analog cameras have been replaced by GigE digital cameras coupled to image intensifiers. **Preliminary tests revealed that the typically used sub-image rectangles of 128x128 pixels can be acquired at rates of up to 400 frames per second, more than 10 times faster than the previous acquisition rate**. To address the increase in CPU workload for the image processing, new VME CPU cards (Intel 4 core/2.5GHz/8GB RAM) are envisaged to be installed (replacing the previous Intel Core 2 Duo/1.5GHz/1GB RAM). This paper focuses on the software changes proposed in order to take advantage of the new CPU's multi-core capabilities for parallel computations. It will describe how beam profile calculations can be pipe-lined through a pool of threads while ensuring that the CPU keeps up with the increased data rate. To conclude, an analysis of the system performance will be presented.

Hardware setup overview

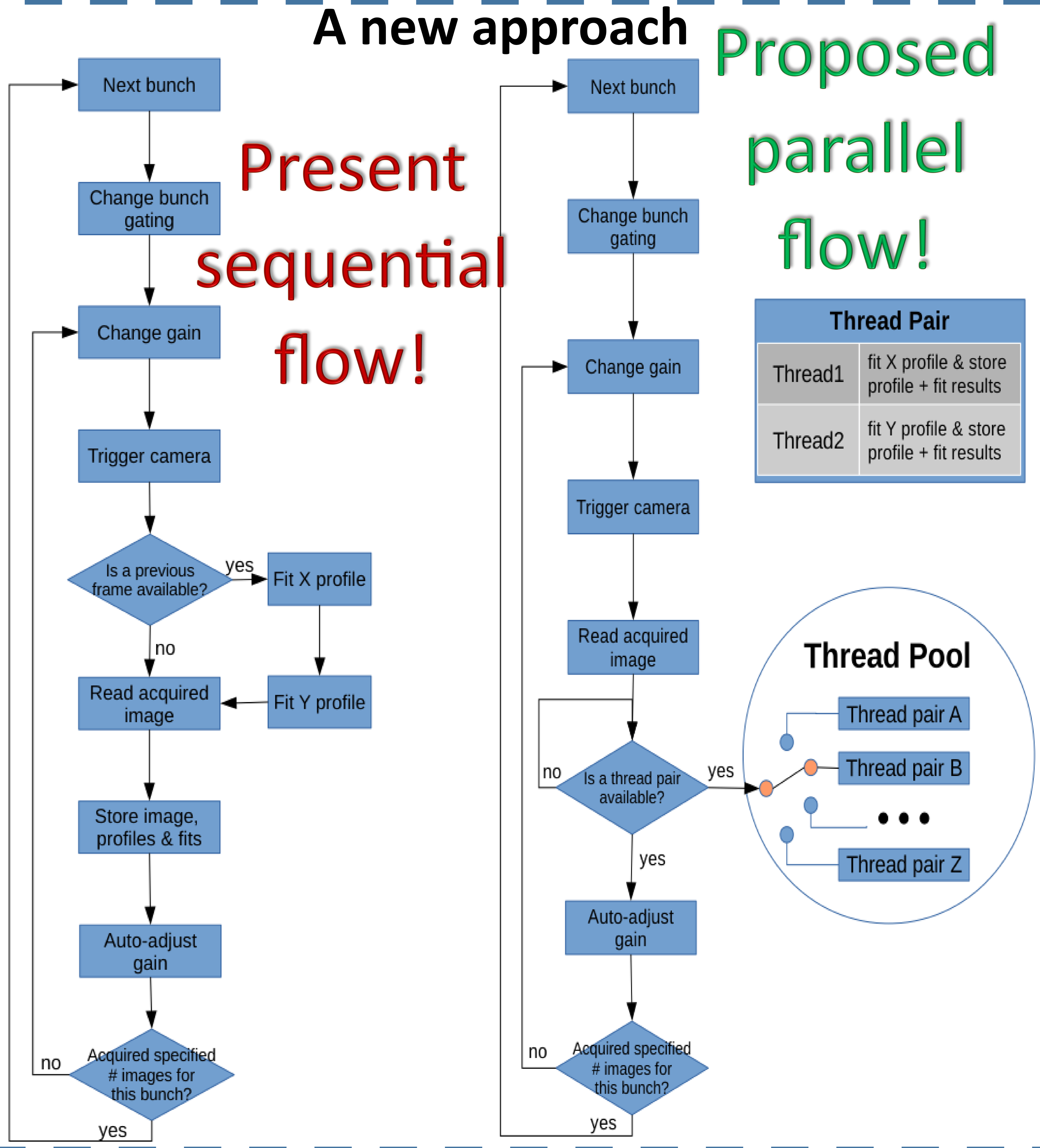


Transverse emittance calculation

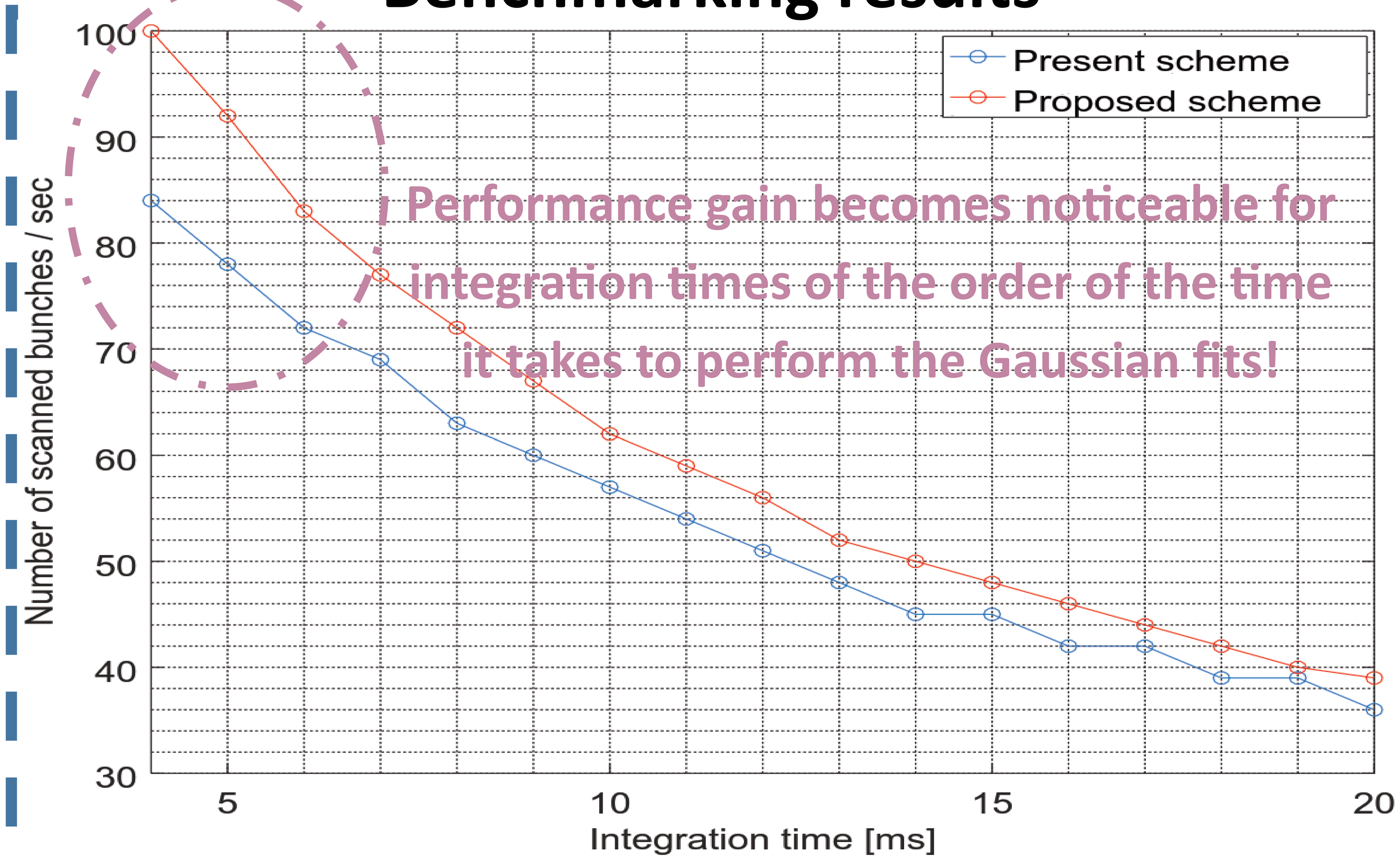
- Project image intensity in x & y transverse axis
- Gaussian fit of projections in x & y transverse axis
- Calculate transverse emittances from beam sizes



A new approach



Benchmarking results



Conclusions

With this work we have demonstrated that the bunch scanning speed when using parallel processing to provide average transverse bunch sizes and emittances should be superior to the currently used technique. It can be seen for example, that **for an integration time of 5ms there is an 18% (i.e. 14 bunch/sec) gain in terms of scanning speed** by using the proposed parallel scheme. Although already quite relevant for current LHC operation, **the main goal of this work is not to demonstrate that a performance gain could be achieved but to devise a scheme that would remain valid and scalable with the number of available cores**. The extrapolation of the results of this test for the future MEN-A25 4 core processor card (using 2 Thread Pairs) is not straightforward since processor idiosyncrasies affecting performance are not simple to anticipate. However, from this test one expects that **the gain in bunch scanning speed will only be evident for short integration times**. Although short integration times mean less light hence a poorer signal-to-noise ratio, preliminary tests indicate that with the new digital cameras, and even for integration times of only a few milliseconds, the signal-to-noise ratio is good enough to perform the Gaussian fits and extract the transverse beam sizes.