The Implementation of KSTAR Fast Interlock System using compact-RIO

•Myungkyu Kim, Taehyun Tak, Jaesic Hong, NFRI, Deajeon, Korea

In the tokamak using superconducting magnet that can operate in long pulse with high temperature and density plasma, the interlock system is becoming more and more important to protect the device itself. Korean Super-conducting Tokamak Advanced Research (KSTAR) achieved high-confinement mode (H-mode) operation for 70 seconds in 2016. In this case, it is necessary to have precise and fast operation protection device to protect Plasma Facing Component (PFC) from high energy and long pulse plasma. The higher the energy of the plasma, the faster the protection is required, and the protection logic should be implemented to process the signals from the various devices as quickly as possible. To meet these requirements, KSTAR implemented the Fast Interlock System (FIS) using NI's Compact Reconfigurable Input Output (c-RIO). The c-RIO is a device using FPGA (Field Programmable Gate Array), its form is similar to PLC (Programmable Logic Controller) and is easy to expand I/O. The implemented protection logic is performed in the FPGA, so input and output can be processed quickly and much. The EPICS IOC performs communication with peripheral devices (PCS, CCS, SIS, heating devices) and operation of c-RIO.

History of KSTAR Fast Interlock System

- 1st Version, 2009

Central Control System (CCS) activates heating stop from Plasma Control System (PCS) using RFM within 200ms.

- 2nd Version, 2012

Fast interlock interface activates heating stop from plasma current (Ip) signal using Timing Synchronization System (TSS).

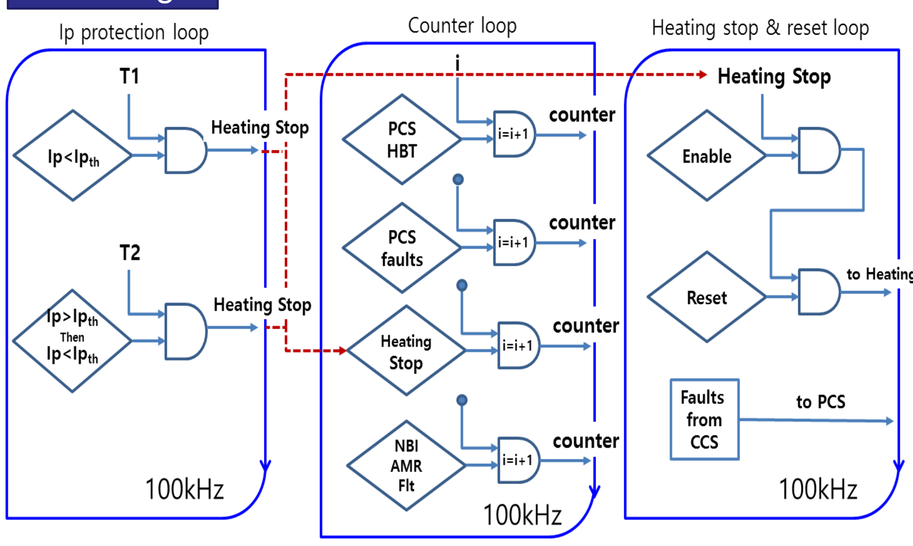
- 3rd Version, 2014

2nd Version plus
Plasma Facing Component (PFC) fault, NB armor fault, CCS to PCS using RFM

c-RIO module description

Modules	Description	No.
NI 9159	14-slot chassis, LX110 FPGA, MXIe	1
NI 9402	4-ch, 55ns, DIO, BNC	4
NI 9401	8-ch, 100ns, DIO, 25pin D-SUB	2
NI 9426	32-ch, 7㎲, DI, 37pin D-SUB	2
NI 9477	32-ch, 8㎲, DO, 37pin D-SUB	2
NI 9215	4-ch, 100kS/s/ch, 16 bit AI, BNC	2

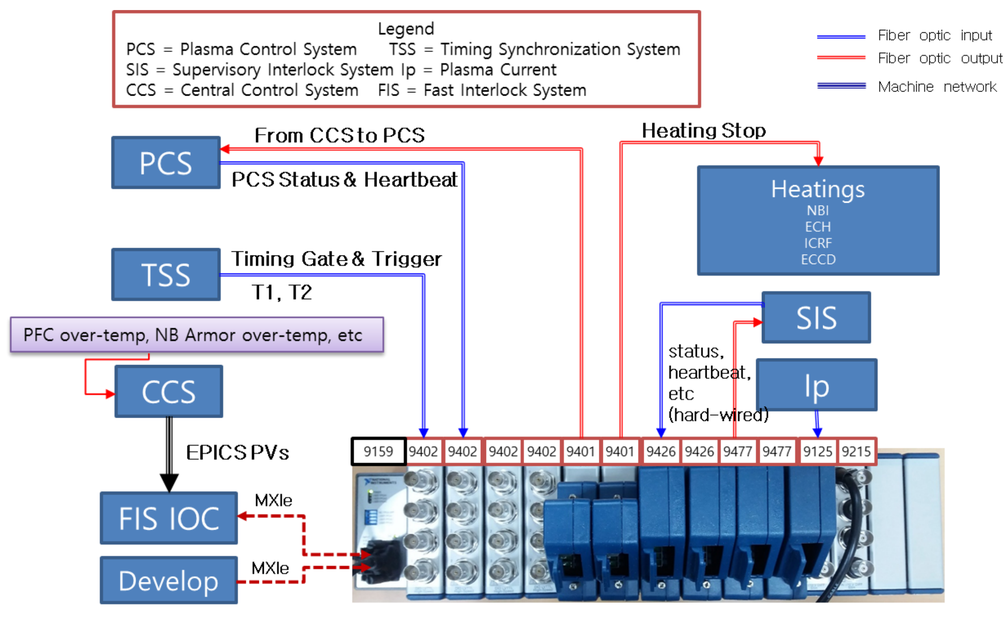
FPGA Logic



Why c-RIO?

- Fast response time, fast processing time
- Proven device, platform, high reliability
- Easily implement and modify logic using FPGA and LabVIEW
- Fast system development
- Communication with EPICS using IRIO is possible.

Configuration of KSTAR fast Interlock System



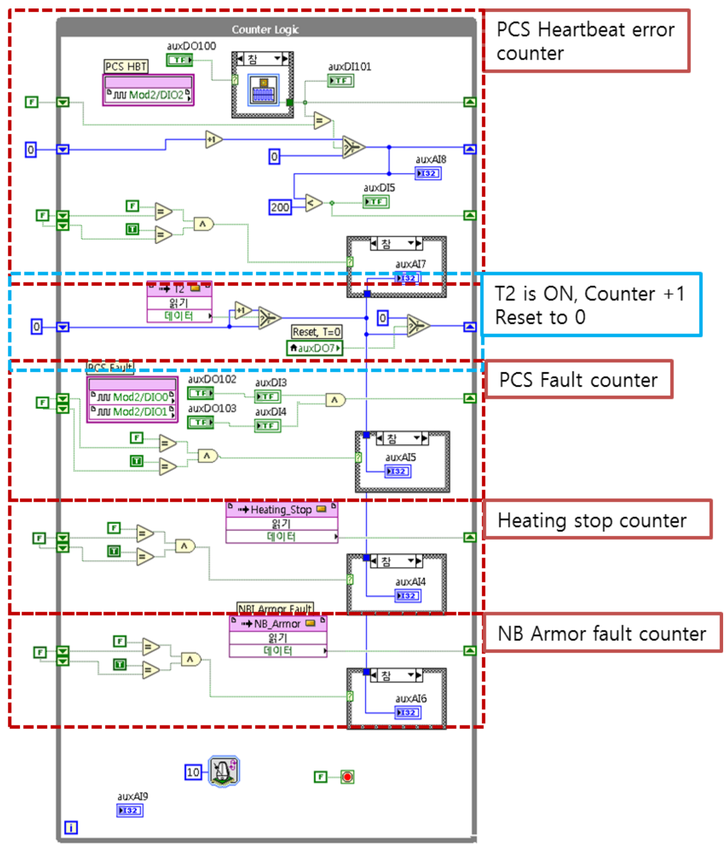
Conditions for fast Interlock

- While T1 ON, $Ip<Ip_{th}$
- While T2 ON, $Ip>Ip_{th}$ then $Ip<Ip_{th}$
- PCS fault
- NBI armour over-temperature fault via EPICS
- PFC over-temperature fault via EPICS

LabVIEW FPGA code for the Counter loop

Counter Loop(Logic)
Event recording after T2 ON
Increase counter 1 by 10㎲ cycle

auxAI4 : Heating stop counter
auxAI5 : PCS fault counter
auxAI6 : NBI Armor fault counter
auxAI7 : PCS Heartbeat error(1kHz) counter



Test result for the Counter loop(heartbeat error)

PCS Heartbeat(HBT) error forced generation

auxDO105 : T2, True = ON
auxDO7 : reset, True = ON
auxDO100 : HBT error, False=ON

T2 ON, HBT error
=>2.111698 sec
Counter = 2.11369 sec
Δt = 0.001992s

T2 ON, HBT error
=>1.565027 sec
Counter = 1.56702 sec
Δt = 0.001993s

- HBT fault occurs when the same value exceeds 200 times during 1 kHz HBT at 10 ㎲ clock.
- Theoretically, 1st detection is possible only after 2ms!

Conclusion & Future works

- **4th version The KSTAR Fast Interlock System was installed hardware and software for 2017 operation.**
- **However, due to the early termination of the unexpected campaign, commissioning on actual equipment had to be delayed until 2018.**
- **FPGA programming is preparing for more features and a variety of situations, and will be applied in 2018.**
- **Also, in the long term, Fast Interlock Server will share information with PCS and RFM Gate-way using Synchronous Databus Network (SDN) of ITER.**