RAPID CONTROL PROTOTYPING TOOL FOR THE SIRIUS HIGH-DYNAMIC DCM CONTROL SYSTEM

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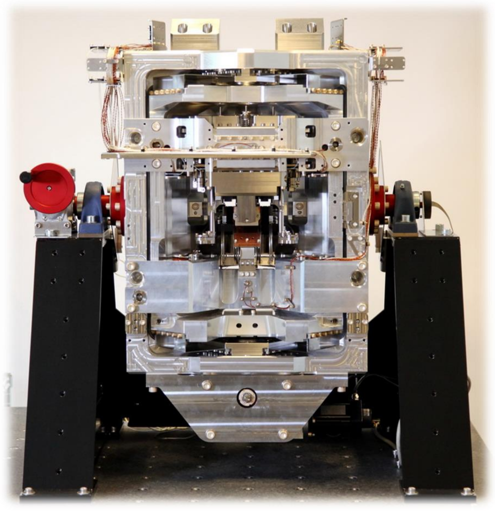
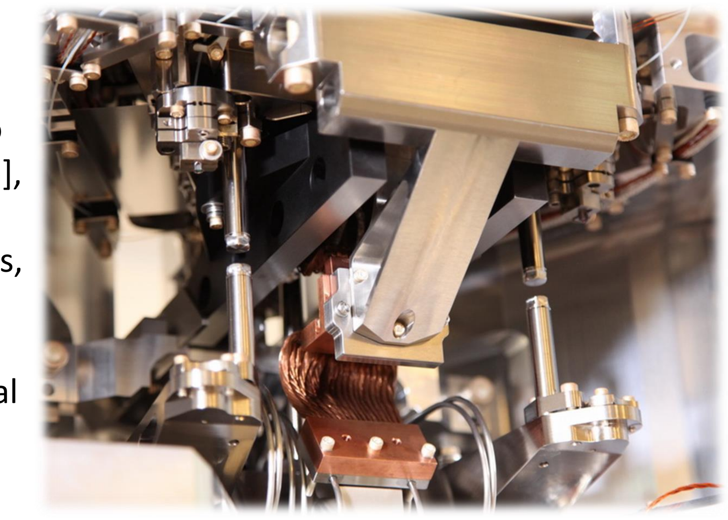


Abstract

The monochromator is known to be one of the most critical optical elements of a synchrotron beamline. It directly affects the beam quality with respect to energy and position, demanding high stability performance, and fine position control. The new high-dynamic double-crystal monochromator (HD-DCM) [1-5], prototyped at the Brazilian Synchrotron Light Laboratory (LNLS), was designed for the future X-Ray undulator and superbend beamlines of Sirius, the new Brazilian 4th generation synchrotron [6-8]. At this kind of machine, the demand for stability is even higher and conflicts with factors such as high power loads, power load variation, and vibration sources. To identify and ensure sufficient control of the dynamic behavior of all subcomponents in the prototype, an implementation in MATLAB / Simulink Real-Time environment in a Speedgoat Real-Time Performance Machine [9] was developed. This approach enables rapid prototyping, by allowing a shared environment for system modeling and testing. The tool was developed in a modular architecture aiming at a practical model iteration and platform migration to beamline controllers, which can prove portability and scalability features.



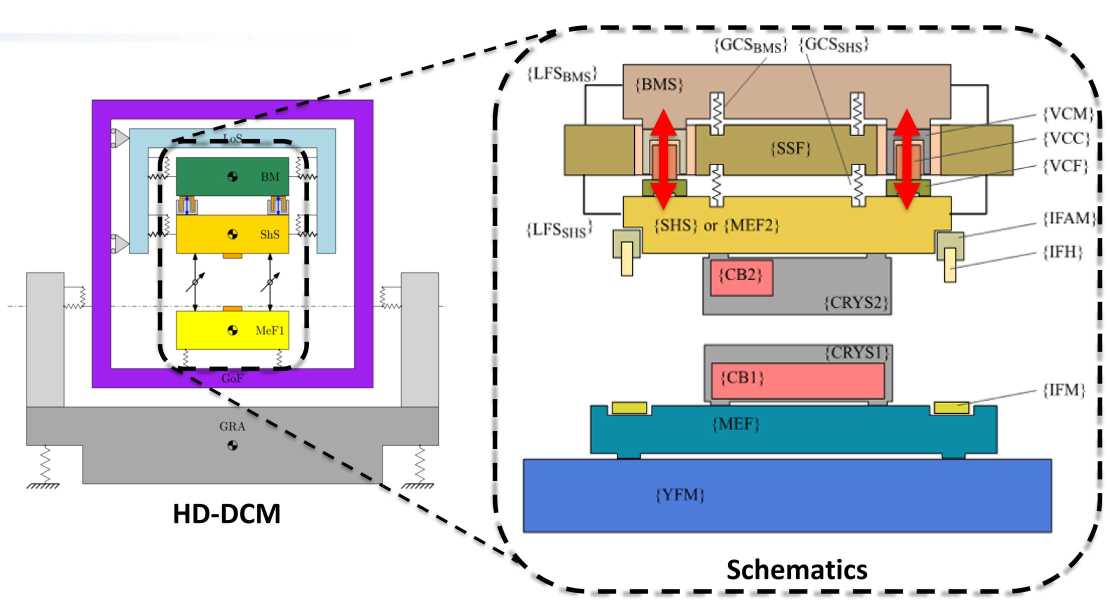
Introduction

This work presents a Rapid Control Prototyping (RCP) tool, used for designing and testing the new High-Dynamic Double-Crystal Monochromator. This tool was implemented with the objective of speeding up control design and testing phases, considering the upcoming high demand for designing and commissioning multiple high-end systems in a short time for Sirius. Its architecture and parametrization focuses on a smooth migration to a standard control platform, chosen for advanced applications at Sirius beamlines [10].

High-Dynamic DCM Concept

- ❑ Completely reviewed version of usual DCM Design
- ✓ Control-Oriented Mechanical Design
- ✓ Balance-Mass Concept
- ✓ Contactless Actuators
- ✓ Leaf-Springs
- ✓ Thermal Control

- ❑ High-Dynamic Core Tests (performed mid 2017)
- ✓ 9.2nrad rel. pitch/roll error*
- ✓ 0.9 nm rel. gap error*
- ✓ in-vacuum cryocooled system expected by the end of 2017.

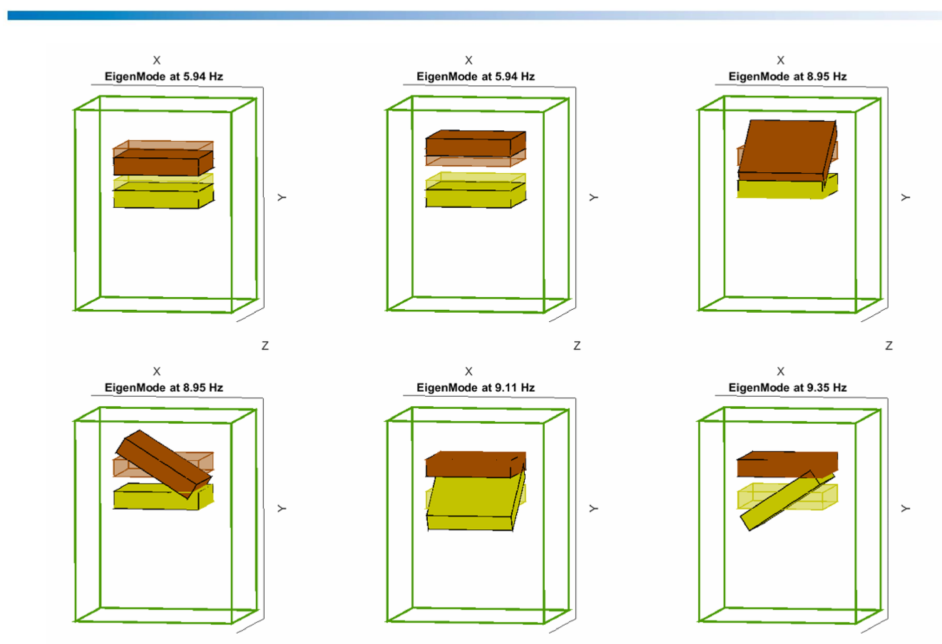


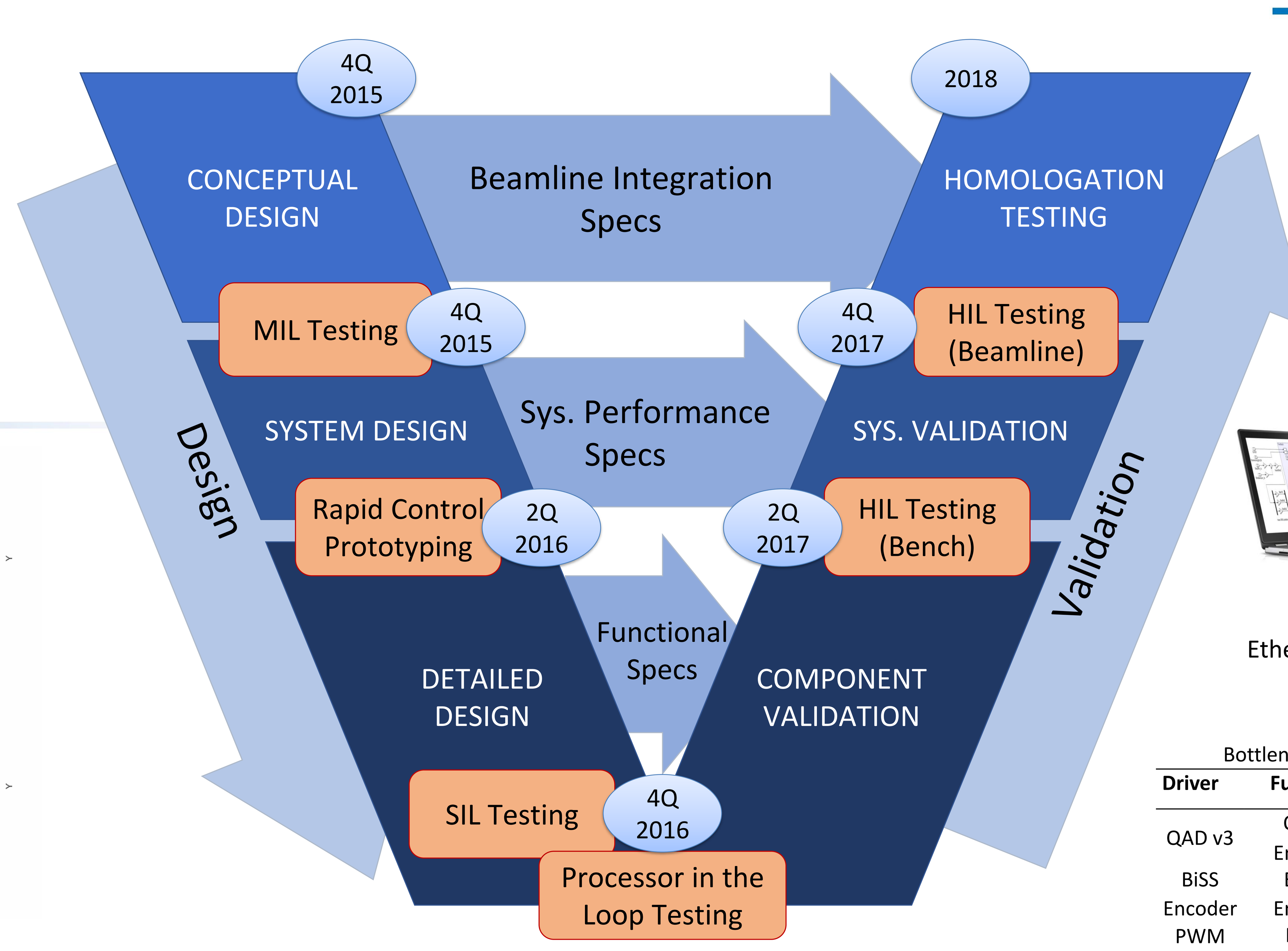
HD-DCM Main Control Specifications

	Bragg Angle	Long Stroke	Short Stroke	Thermal Control
Actuator Type	Torque Motor	Stepper or Servo	Voice-Coils	Foil Heaters
Sensor Type	Rot. Incr. Encoder	Lin. Abs. Encoder	IFM	RTDs
Feedback Resolution	50nrad	5nm	0.1nm/ 1nrad	<10mK
Stability target*	<0.8µrad	N/A	<10nrad	<50mK
Closed-Loop BW	35 Hz	20 Hz	>250 Hz	0.1 Hz
Feedback Sampling	10 kHz	10 kHz	20 kHz	20 Hz

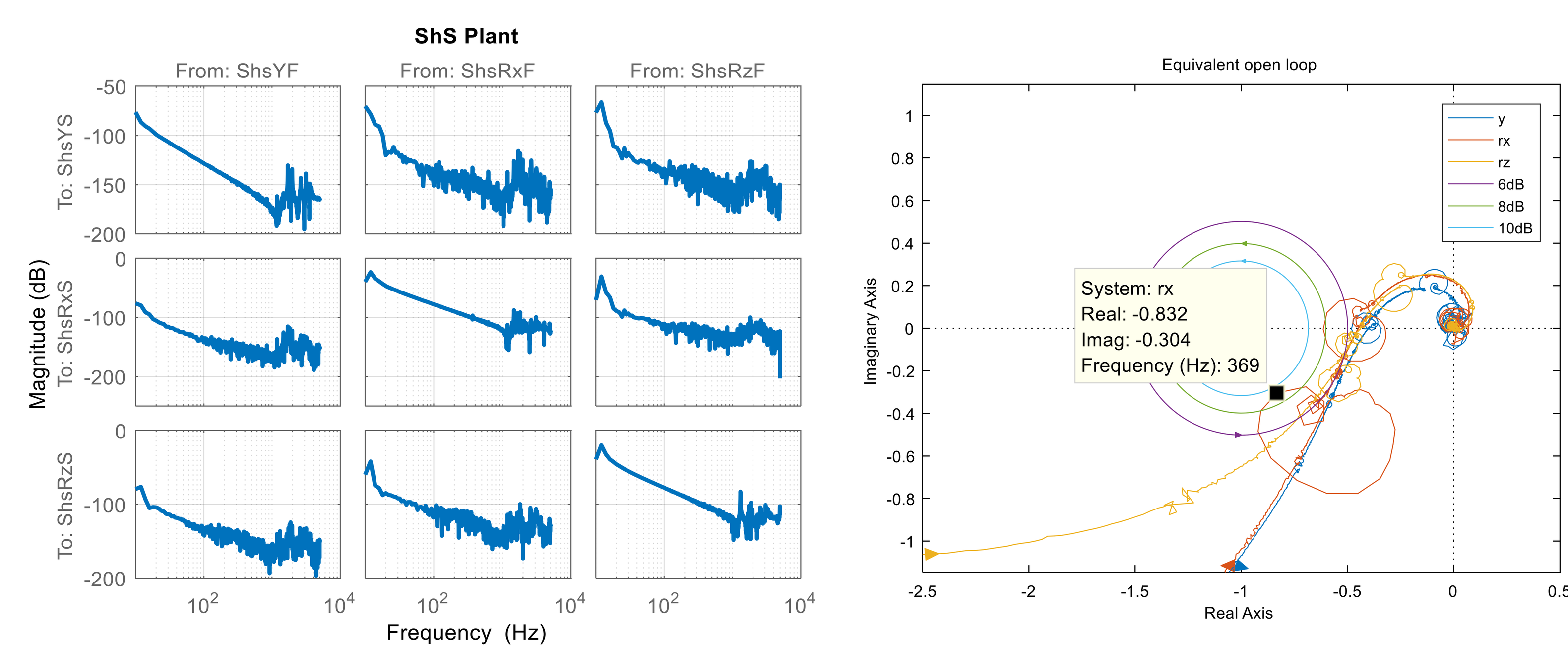
*In-position stability, RMS values integrated up to 2500 Hz.

Model Based Design





System Validation



MIMO plant identification, using step sine (left), and Nyquist plots for the Identified HD-DCM plant.

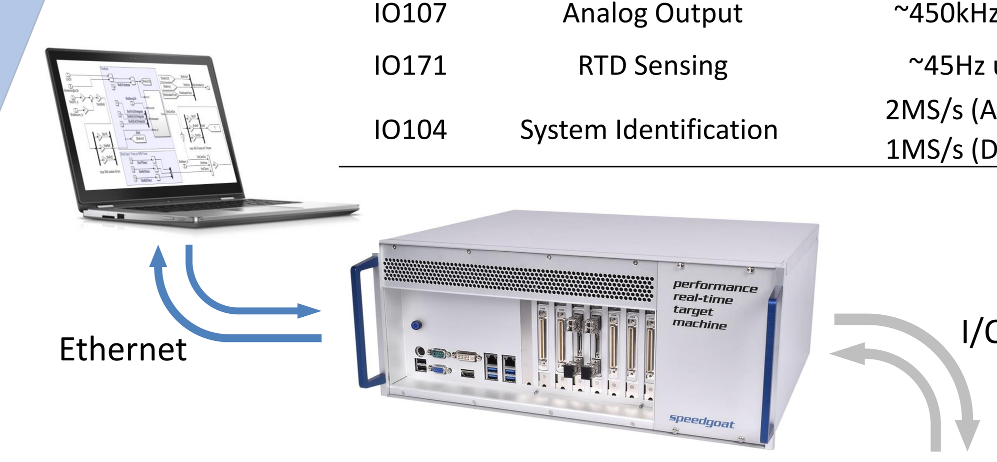
RCP Hardware Performance

Performance Real-Time Target Machine:

- ✓ Intel Core i7 3,5GHz CPU;
- ✓ 4GB RAM
- ✓ 250GB SSD (540MB/s)
- ✓ Custom FPGA Implementation
- ✓ Speedgoat Library for MATLAB
- ✓ 2x Gigabit Ethernet ports
- ✓ 1x COM port
- ✓ 5x USB ports
- ✓ 3PCI + 4PCIe (Expandable)

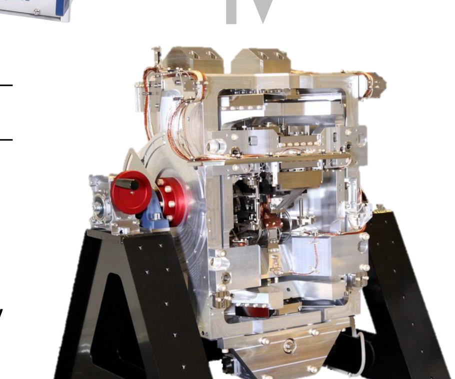
Speedgoat Performance Real-Time Machine Boards

Hardware	Function	Maximum Rates
IO333	Digital I/O (with FPGA)	Applic. Dependent (75MHz Clock)
IO107	Analog Output	~450kHz update
IO171	RTD Sensing	~45Hz update
IO104	System Identification	2MS/s (AD+DMA) 1MS/s (DA+DMA)



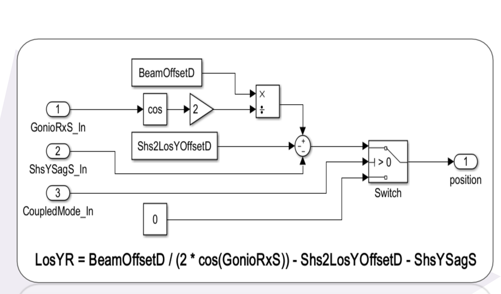
Bottlenecks for Performance IO333 FPGA Drivers

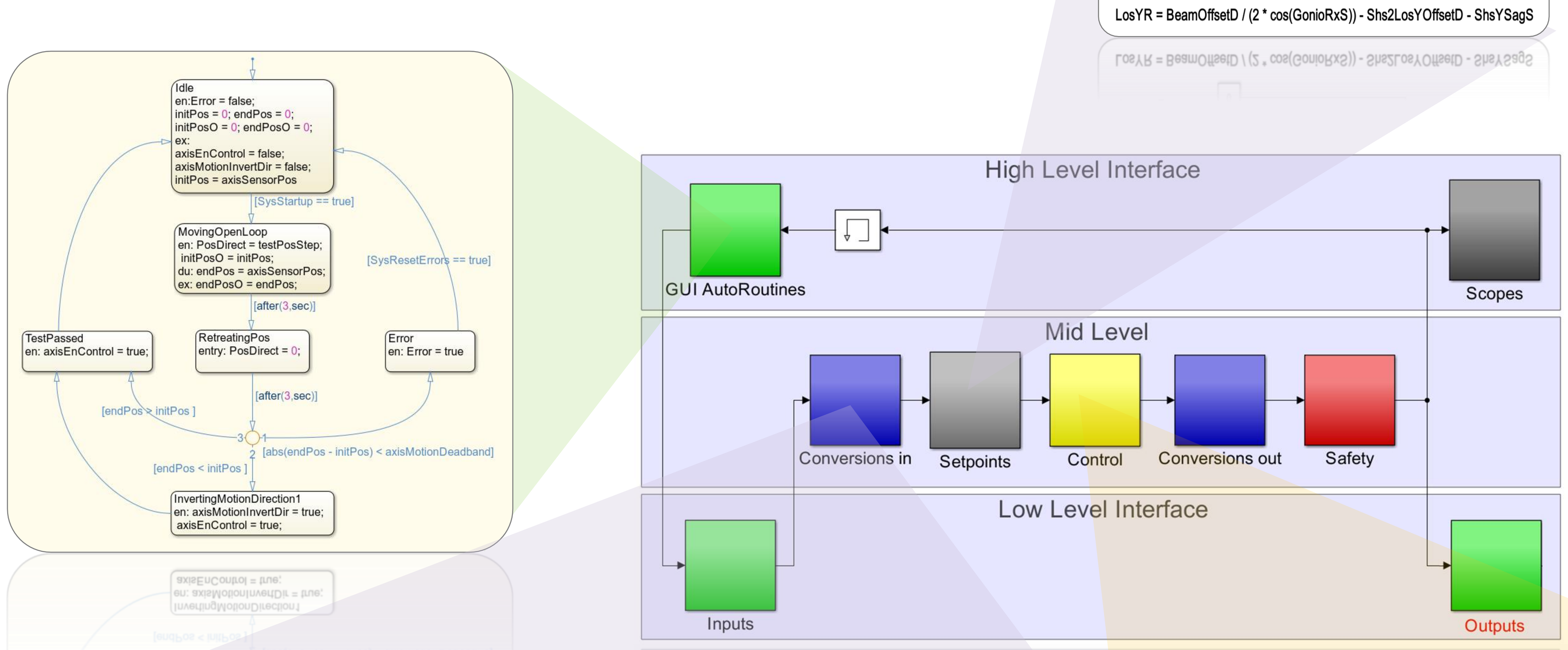
Driver	Function	Bottleneck
QAD v3	Quad. Encoder	Decoding Limited to 75MHz clock (4x res. not possible at 20MHz)
BiSS Encoder	Biss-C Encoder	Minimum latency of 80µs (12.5 kHz maximum feedback rate)
PWM Gen	PWM Output	Latency of a full PWM period to apply parameter changes
Dig. I/O	Trigger Output	13.3ns latency specification (75MHz FPGA Clock)

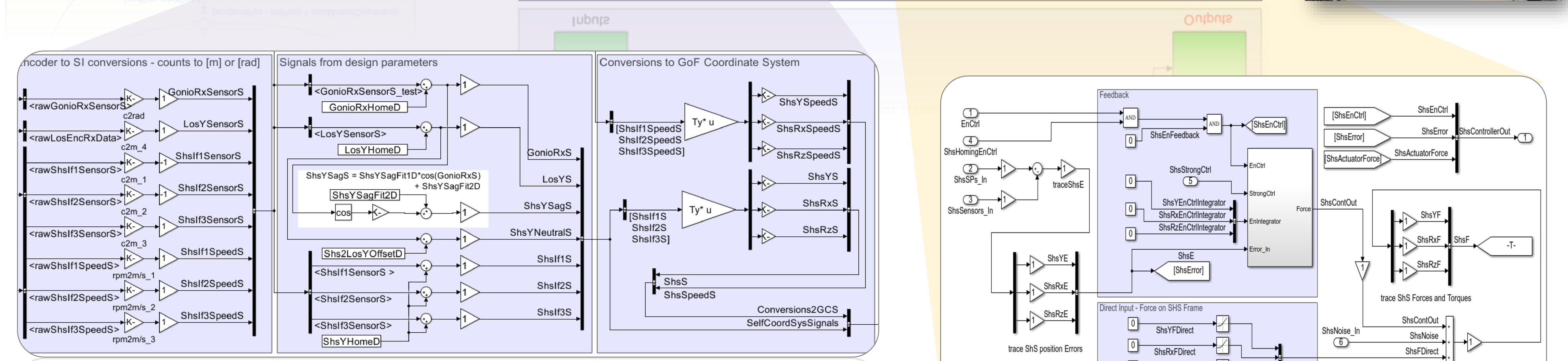


RCP Tool Architecture

The demand for quickly testing the HD-DCM system and future projects has put modularity and flexibility as key factors when structuring the RCP tool. This way, the software architecture for its implementation in Simulink Real-Time was made in blocks, and organized in preliminary layers, namely: low-level interface, mid-level, and high-level interface.







Conclusion

The RCP tool implemented in Speedgoat's xPC target accelerated the design and testing phases, permitting the model and hardware tests to coexist in the same platform. The proposed architecture modularity and flexibility, allows parameters and even complete structures to be directly exported from the Simulink model to the standard beamline control platform, which has a more advantageous cost-benefit relation. Indeed, once the development of the HD-DCM is finished, its final control plat-form will take over and the RCP tool will be modified for a new system.

Acknowledgement

The authors would like to gratefully acknowledge the funding by the Brazilian Ministry of Science, Technology, Innovation and Communication and the contribution of the LNLS team, the MI-Partners team and those of the synchrotron community who directly or indirectly built the path to this development.

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