Introducing Fast Interlocks in the UNICOS-CPC framework

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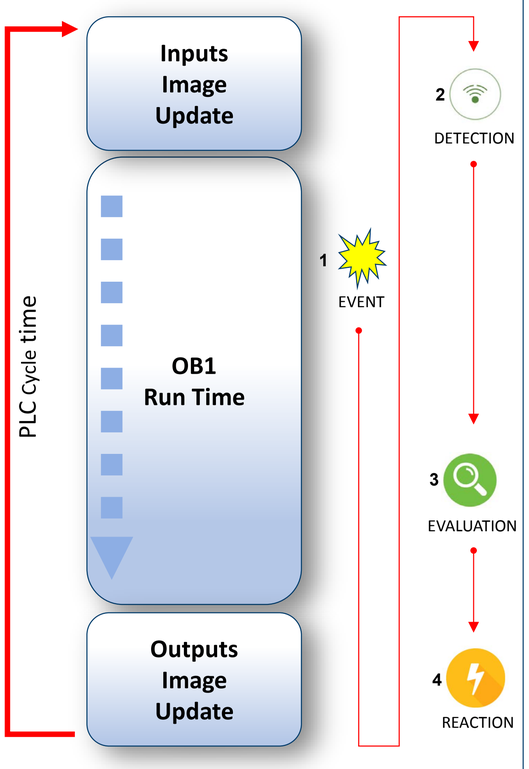
THPHA150

The CERN UNified Industrial COntrol System framework (**UNICOS**) with its Continuous Control Package (**UNICOS- CPC**) is the CERN standard solution for the design and implementation of continuous industrial process control applications. Reacting as fast as possible to an interlock situation is a new requirement which has been introduced in UNICOS-CPC. This poster presents the challenges, design and test results of the seamless integration of fast interlocks capabilities in the current UNICOS-CPC package based on SIEMENS PLCs.

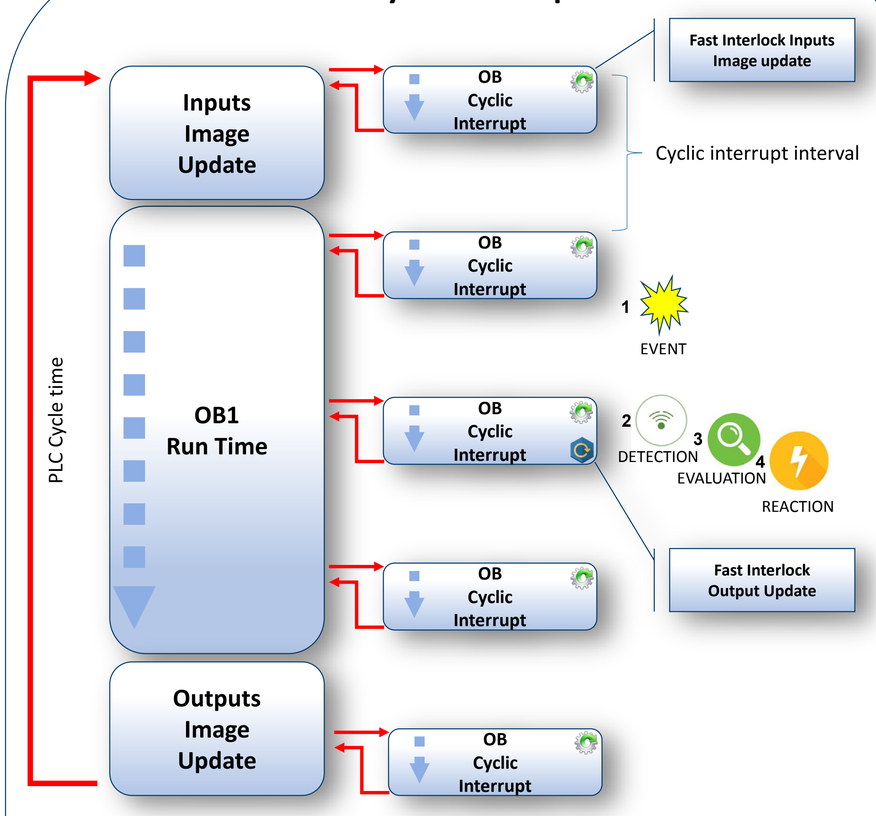
INTERLOCK TREATMENT SOLUTIONS

Standard



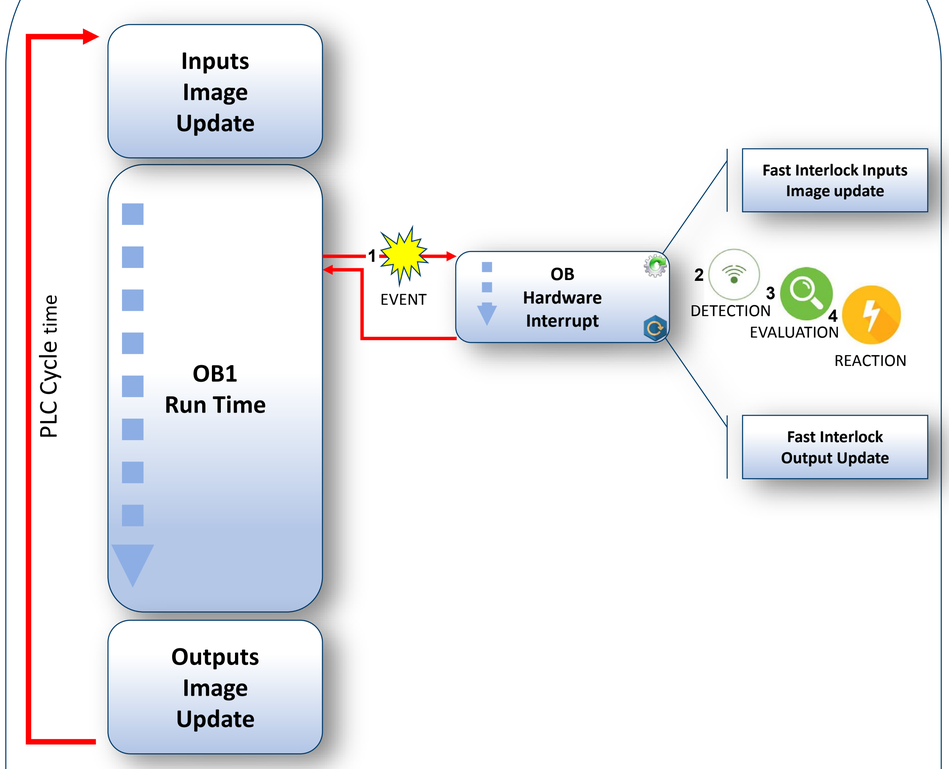
- ✓ **Standard reaction time**
- ✓ Runtime cycle time dependant
- ✓ Low level of determinism

Cyclic Interrupts



- ✓ **Medium-fast reaction time**
- ✓ Cyclic interrupt interval dependant
- ✓ Medium level of determinism
- ✓ No specific hardware needed

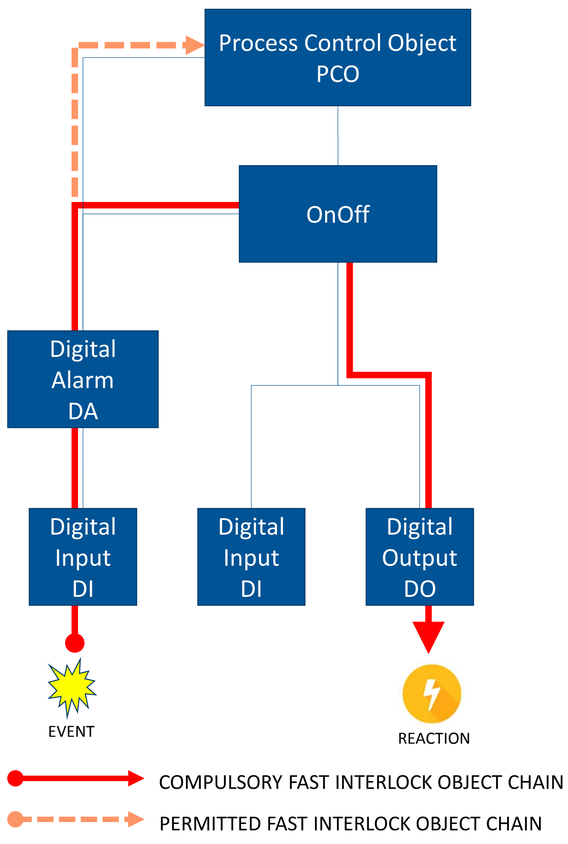
Hardware Interrupts



- ✓ **Fast reaction time**
- ✓ Runtime cycle independent
- ✓ High level of determinism
- ✓ Specific hardware needed

UNICOS-CPC INTEGRATION

UNICOS CPC objects interaction in the Fast Interlock chain



The UNICOS-CPC objects conforming the fast interlock chain are excluded from the main (OB1) runtime and executed in the interrupt OB (Cyclic or Hardware)

ISSUES

- ✓ Concurrency
  Shared resources executed during interrupt
- ✓ Consistency
  Digital inputs updated during interrupt

SOLUTIONS

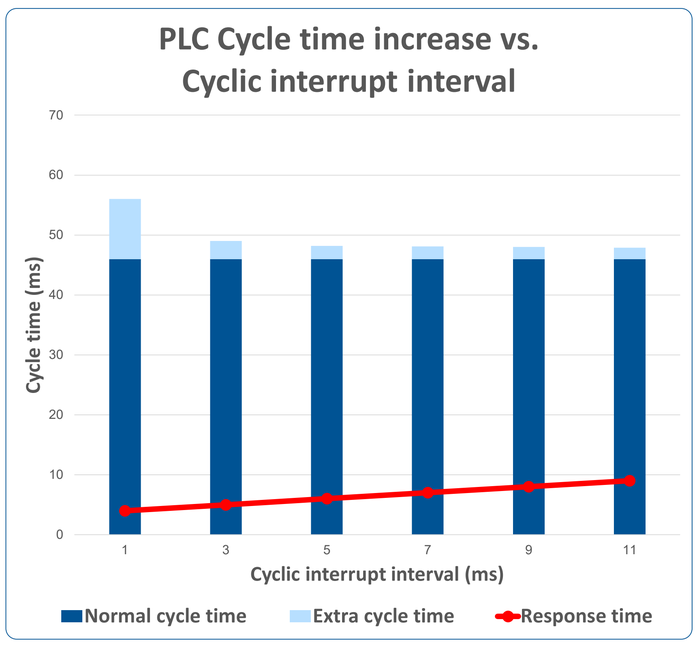
Interrupts are disabled during the execution of shared resources:
- ✓ SFC 41 "DIS_AIRT“
- ✓ SFC 42 "EN_AIRT"

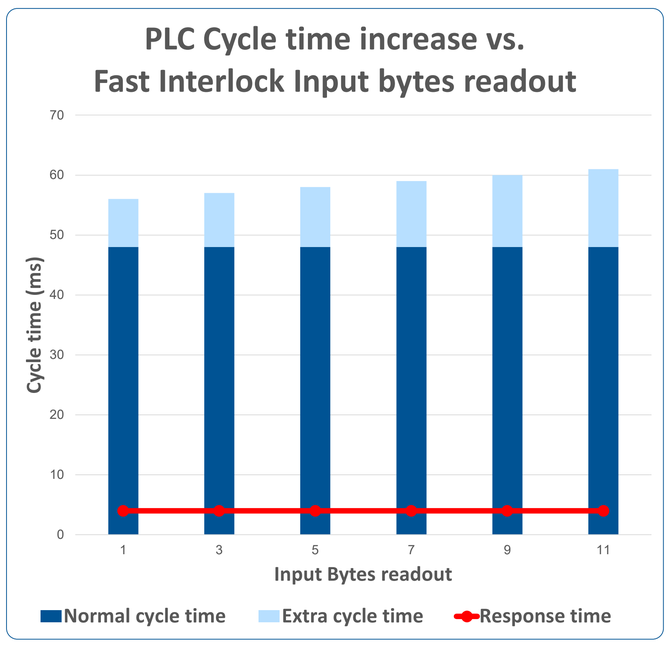
Only input bits of fast interlocks are updated

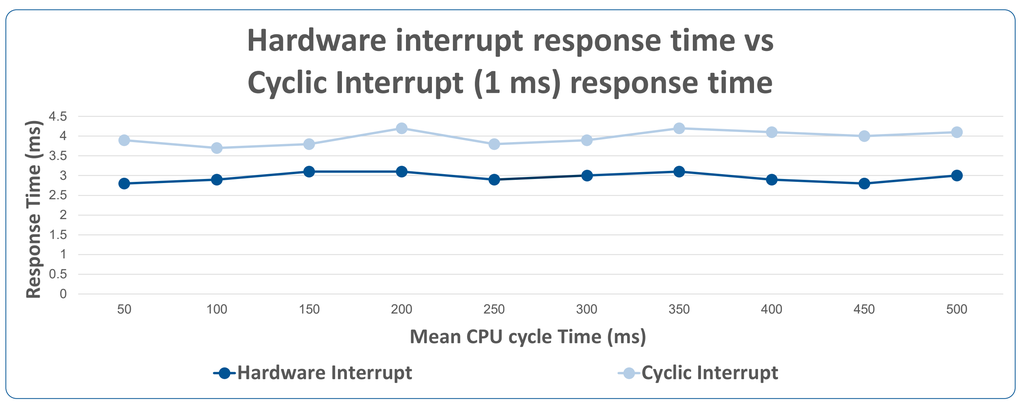
Input image byte		Peripheral input byte	New input image byte
00**101**001		10**100**001	
AND		AND	
11**000**111		00**111**000	
⇩		⇩	
00**000**001	OR	00**100**000	⇨ 00**100**001

Peripheral input bits

TEST RESULTS







- Two solutions: HW and cyclic interrupts.
- Reaction times ~ 3 ms for Hardware interrupts.
- Reaction times ~ 4 ms for Cyclic interrupts of 1 ms interval.
- Reaction times not depending on PLC cycle time.

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